S-Parameter Correlation

of typical PCB interconnect structures

As the use of S-Parameters to characterize and model typical Multi-GHz (MGH) PCB structures increases, a careful examination of both tools and methods is needed. This paper examines the S-Parameter correlation of Allegro PCB SI 630 against hardware measurement while offering practical advice for a new generation of hardware engineers now deploying S-Parameter techniques in the context of mainstream digital design.

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Revision 1.0

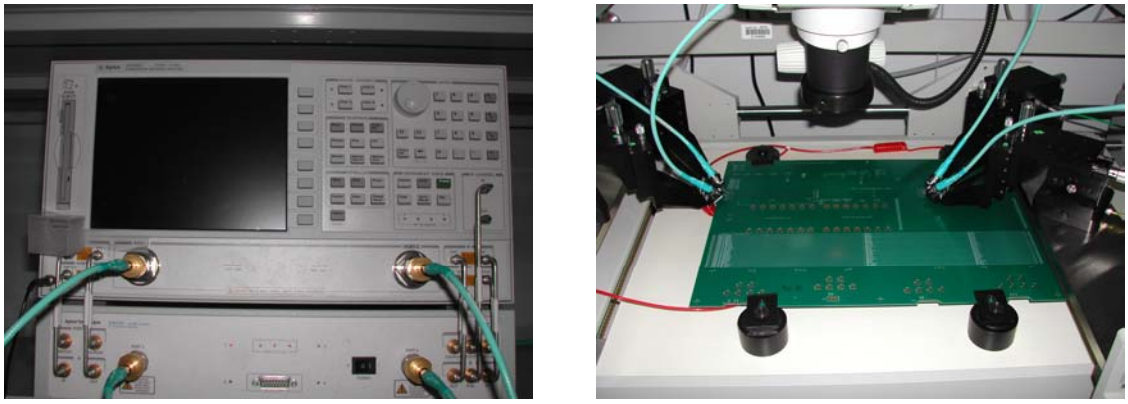
1. Introduction

This paper details the process used to correlate S-Parameters generated by Cadence Allegro PCB SI 630 with measured S-Parameters of the same physical PCB interconnect structures. Instead of simply showing the final correlation overlays, we will detail the steps taken to arrive at them. In this way, the common pitfalls will be illustrated with hopes that the reader can avoid them. To quickly overview the quality of the correlation, please refer to the various diagrams in sections 3 through 6.

2. Correlation Environment

All simulations were performed using version 15.2 of Allegro PCB SI 630 that includes complete support for S-Parameter generation and analysis.

Measurements were performed using an Agilent 8720ES 50MHz to 20 GHz S-Parameter (Vector) Network Analyzer (VNA) with picoprobes as shown in Figures 2.1.



Figures 2.1: Correlation Measurement Equipment

The 8-layer PCB testboard used in this exercise provides example traces in a variety of configurations, as well as convenient probe pads to aid in the measurement process. The testboard was designed by Intel, and then built with FR4 dielectrics using a typical volume printed circuit board fabrication process. The testboard was designed and built, in part, by engineers responsible for the original PCI Express Specification in order to empirically test and validate some of the assumptions and simulations made in deriving the specification.

This paper will provide an in-depth look at the correlation for three types of differential routing with varying lengths: 7” microstrip, 15” stripline, and 10” microstrip with layer changes.

A photo of the testboard is provided in Figure 2.2.

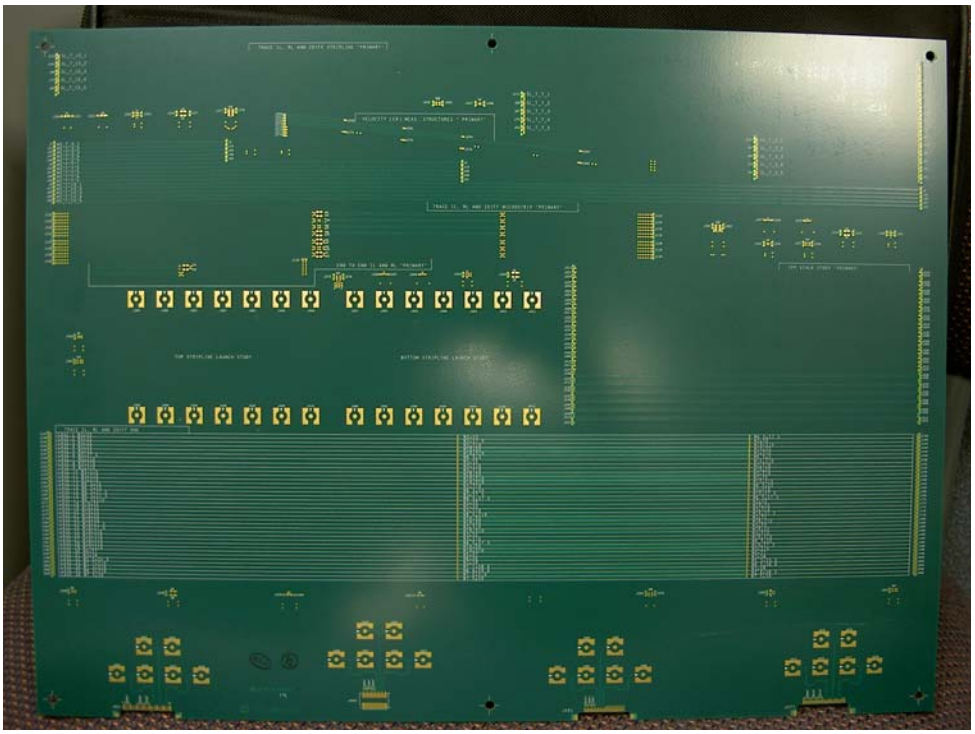


Figure 2.2: Correlation Testboard

And a screenshot of the design database is given in Figure 2.3.

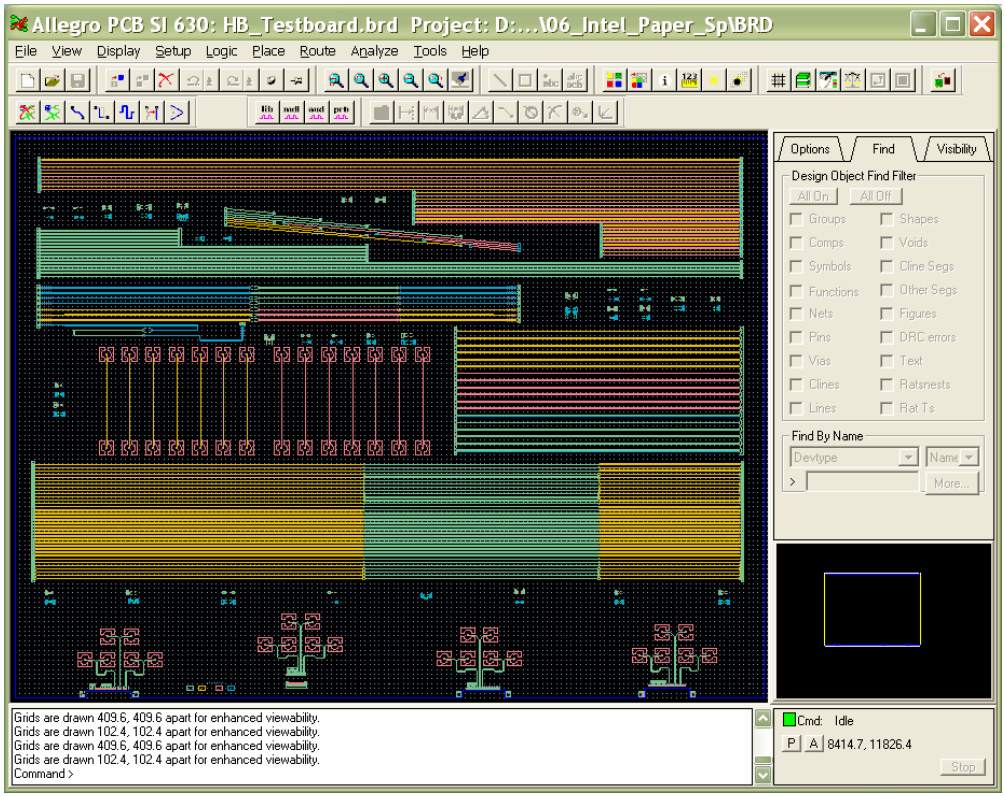


Figure 2.3: Testboard Database shown in Allegro PCB SI 630

Terminology Used

PCB Parameters

To examine S-Parameter correlation for the trace configurations, it is important to define terms related to the accuracy of the physical trace parameters. Examples of physical trace parameters are trace width and spacing. With fabrication adjustments and tolerances, it is common to find that what you designed is not what is built (and hence measured). As such:

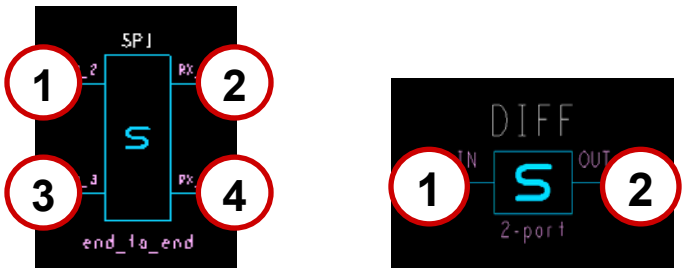
DESIGNED = data in the Allegro layout database, and sent to the PCB fab vendor (ie, what the engineer expected to be built)
BUILT = what the PCB fab vendor attempted to build (ie, what the fab vendor tried to build). Note: fab vendors often change thickness/widths/etc based on impedance targets and materials on hand.
ACTUAL = what was actually measured on the board (ie, what was actually built). Note: typically, the only way to get these values is to slice open a physical PCB and carefully measure the trace parameters under a microscope.

For example, when we show results related to the BUILT trace parameters the results may still not match what was measured on the ACTUAL circuit board.

Since engineers often do not have access to the latter types of data, the plots should help you grasp the level of accuracy you can expect given the quality of your trace parameters.

Differential Trace Node (Port) Numbers

Differential traces will be numbered throughout as shown in Figures 2.4 for the two common configurations: single-ended (at left), and differential (at right). When driven, we assume a transmitter (Tx) on the left and a receiver (Rx) on the right.



Figures 2.4: S-Parameter Node (Port) Numbers

Furthermore, some diagrams in this paper will plot differential S-Parameters for the trace, commonly referred to as “differential in, differential out” or “Sdd” similar to the configuration shown on the right.

Overall, if you are not familiar with S-Parameter concepts and terminology we highly recommend you view the following 1-hour “webinar” before continuing.

http://www.cadence.com/webinars/webinars.aspx?xml=sparam

Frequency Range of Plots

At the time of this writing, engineers working with PCB characteristics are primarily interested in studying correlation up to 10 GHz. As such, many plots will be focused on this range. However, since data rates will undoubtedly continue to increase, we will also show many plots up to 20 GHz in order to illustrate not only the correlation in that range, but also to highlight the parameters that must be well-characterized to achieve correlation in the 10 to 20 GHz range.

Common Mistakes

As will be illustrated, there are numerous mistakes that can be made when measuring, generating, and using S-Parameters that can lead you to the conclusion that the tools do not work correctly. Throughout this paper, common mistakes will be offset with *red italic type* for easy reference.

One example of a common mistake made when using Allegro PCB SI 630 to generate S-Parameters is to include only DC loss. To ensure that high-frequency AC (e.g., skin effect, dielectric loss) losses are included, be sure to set a non-zero "Cutoff Frequency" in the Analysis Preferences form shown in Figure 2.5.

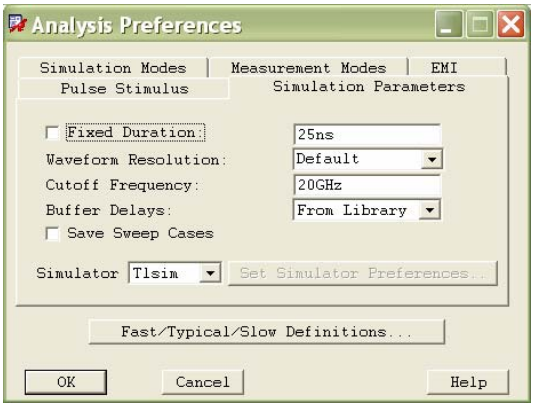


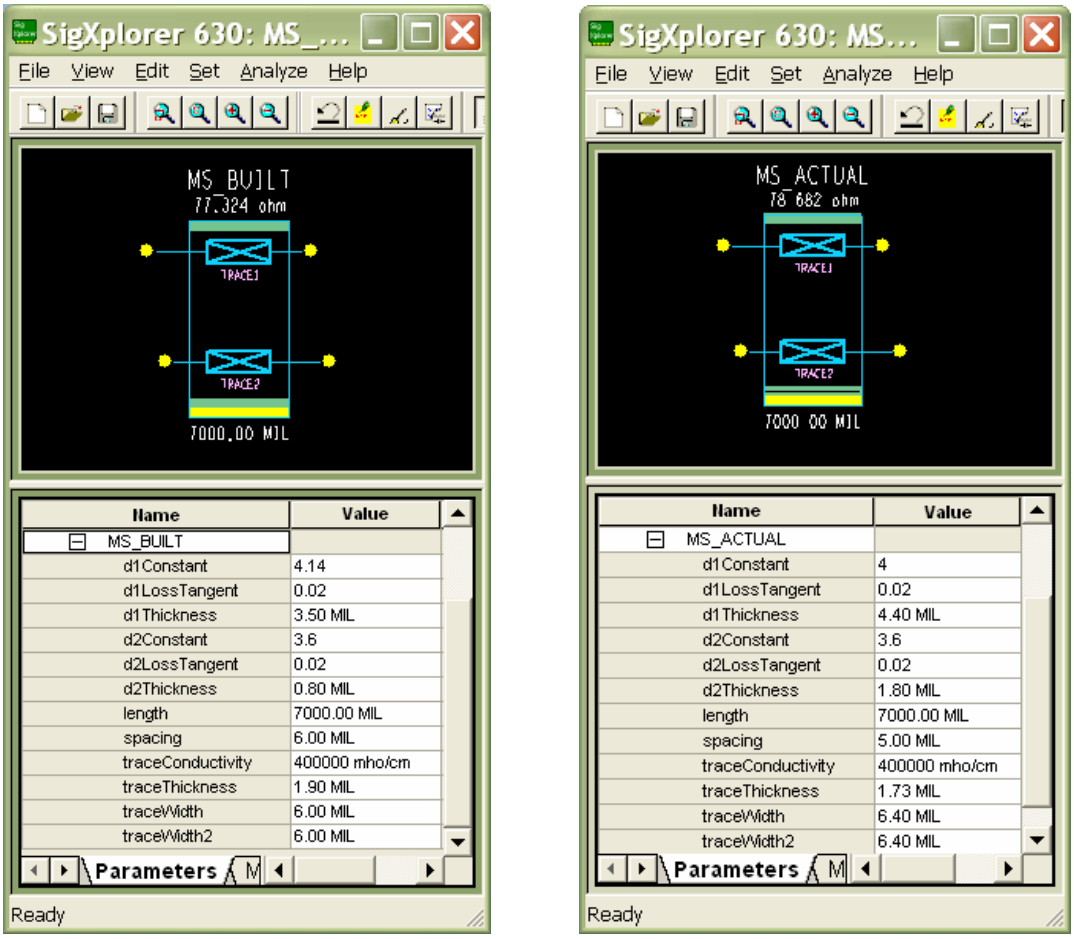
Figure 2.5: Analysis Preference Form

Engineers commonly set the Cutoff Frequency high enough to include the 5th harmonic of the fundamental frequency of your interface. For Multi-GHz analysis, this will typically place the value in the 7 to 20 GHz range. Note that *you must set this value* or the tool will use 0 GHz as a default and ignore AC losses. If you neglect to set the value, all of your S-Parameter plots will show very little loss over frequency.

Common Mistake: Be sure to specify your desired frequency range by entering a value for the Cutoff Frequency in the Analysis Preferences form before generating S-Parameters.

3. Case 1: 7” Microstrip Differential Trace Correlation

To begin the process of correlating measured and simulated S-Parameters we chose a simple 7-inch microstrip trace segment. The BUILT and ACTUAL parameters associated with the trace are shown in Figures 3.1.



Figures 3.1: BUILT and ACTUAL Microstrip Trace Parameters

This data shows that, while there was some variation in dielectric thickness, the overall differential impedance (shown at the top) stayed within 2% (less than 1.5 Ohms). Note that only the physical parameters in the tables above can be corrected using a cross-section measurement, whereas quantities like *dielectric constant* and *loss tangent* are more complex and must be determined by other means.

A photograph of the ACTUAL cross-section is shown in Figure 3.2.

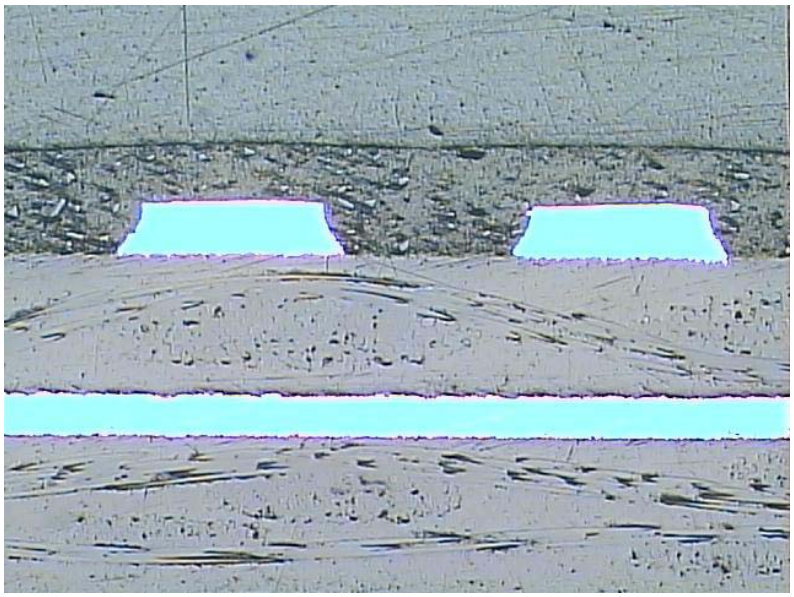


Figure 3.2: Microscope Photograph of Microstrip Trace Cross-section

Various items can be seen in the cross-section photograph:

- The "weave" of the fiberglass can be seen (this will become important later)
- The trace is actually not rectangular. (In this case, it was actually trapezoidal with 7.1 mils at bottom and 5.7 mils at the top. It is approximated to 6.4 mils in the form above. Note that in Allegro PCB SI 630, it is possible to have the integrated field solvers model the trapezoidal effect by using the environment variable "TrapeZoidal_Angle_in_Degree". For a complete discussion on using this and other variables, please see: http://www.allegrosi.com/downloads/App_Note_Env_Variables.pdf .)
- The solder mask turned out thicker than expected, roughly equal to the thickness of the trace.
- The variation in material property/content between the solder mask and lamination dielectrics.

Making the VNA Measurement

Pico-probes were used in acquiring the VNA measurement of the microstrip trace. Initially, the measured data was incorrect because of inadequate positioning of the probes.

The following Figure 3.3 shows how visual inspection of this first measurement reveals the problematic data.

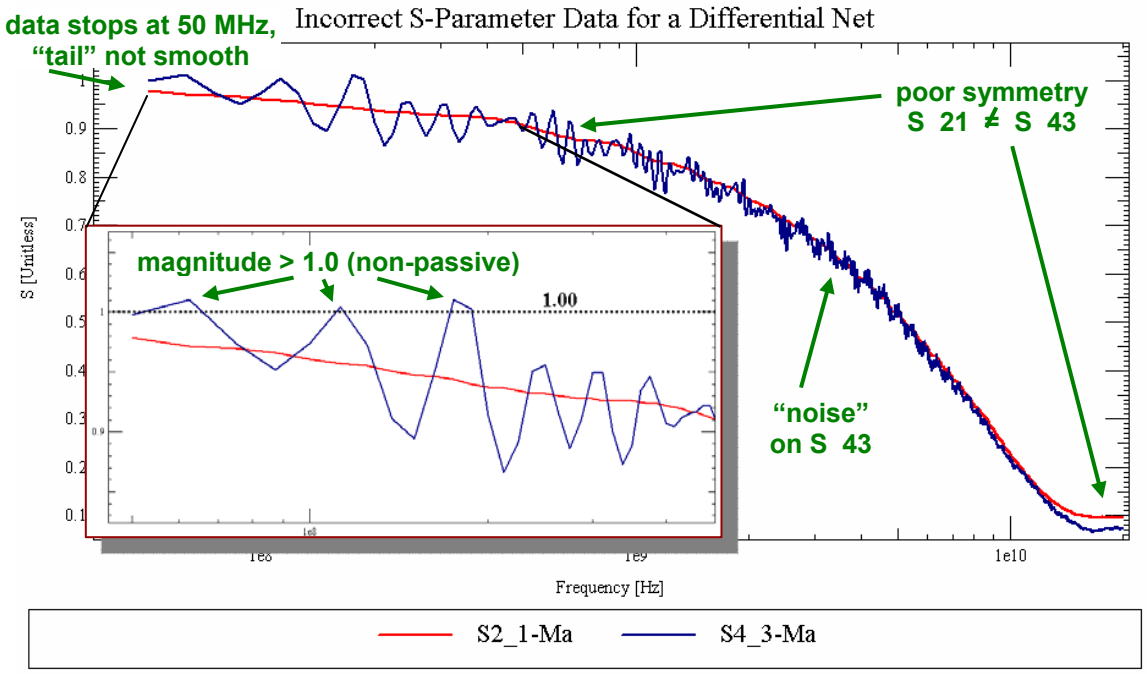


Figure 3.3: Common Problems in S-Parameter Data

Examining Figure 3.3, the experienced eye can notice a number of problems with the measurement (that would result in another attempt):

1. Though this is a symmetric differential configuration, we can see that S_21 does not match S_43 as expected.
2. The magnitude on S_43 goes above 1.0 at three points, showing the data to be not *passive* as would be required for a simple piece of interconnect.
3. The "tail" on the left side of the data is not smooth. This combined with the fact that there is no data below 50 MHz will make it very difficult for any tool using this data to determine this interconnect's DC behavior.
4. In general, S_43 is "noisy" and should be measured again (a curve similar to S_21 is expected).

In our case, inaccuracy of the data was detected by attempting time domain simulation with the measured data/model instead of visual inspection. This simulation revealed unexpected and incorrect initial DC voltage levels, suggesting that the data in the measured model was incorrect. Regardless of how the problem was detected, a more careful measurement had to be (and was) made before proceeding.

Common Mistake: Ensure proper/adequate connections when probing physical systems. Also note that if the differential data is not symmetric, there may be calibration issues as well. Settle on a methodology for examining or testing the measured data before expecting it to correlate.

Microstrip Trace Correlation

Once consistent measurements were obtained, we overlayed them with the S-Parameters generated by Allegro PCB SI 630 as shown in Figure 3.4. Five adjacent 7" microstrip traces were measured (shown in black), with each trace having the exact same DESIGNED and BUILT parameters. The plot confirms what might not be intuitive, that there are significant the loss plot variations for equivalent traces on a single PCB.

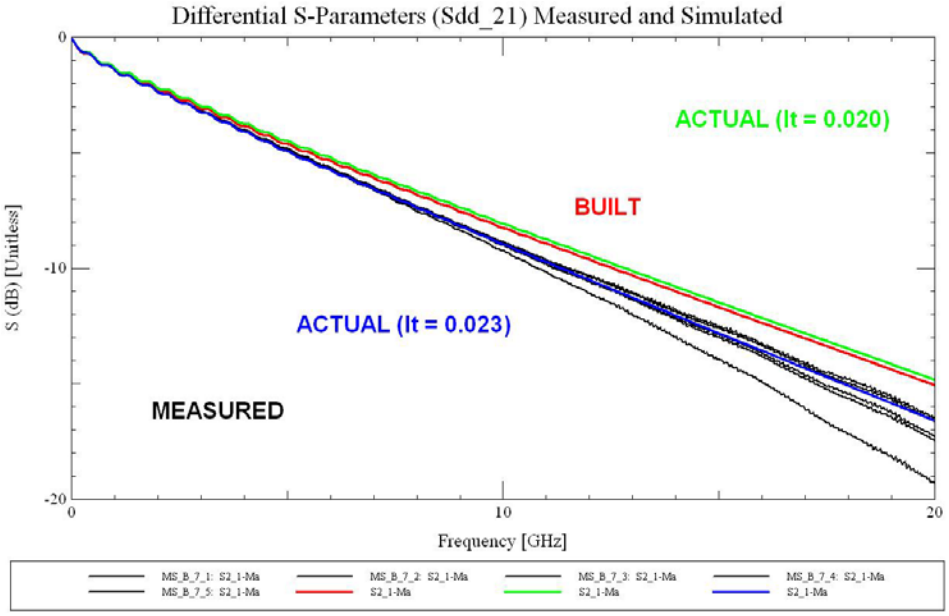


Figure 3.4: Microstrip Trace Correlation

Qualitatively, we see good correlation in all data up to 5 GHz. From 5 to 20 GHz the plots separate more with the BUILT tracking MEASURED better than ACTUAL. Recall that an ACTUAL value for the *loss tangent* (lt) could not be determined by examining the cross-section, so a couple expected values (0.020 and 0.023) are plotted here. Interestingly, lt=0.023 seems to track much better over the entire frequency range. Zoomed in correlation plots can be found in Appendix A.

Quantitatively, the variation from measurement versus frequency is given in the following Table 3.1. By "variation from measurement" we mean the largest delta (in dB) from any of the 5 measurements at the given frequency. As such, the "MEASURED" row lists the variations in all measurements at that frequency.

	3 GHz	5 GHz	10 GHz	15 GHz
BUILT	0.15	0.26	1.0	2.2
ACTUAL (lt=0.020)	0.24	0.41	1.2	2.45
ACTUAL (lt=0.023)	0.05	0.11	0.3	1.1
MEASURED	0.04	0.07	0.4	1.4

Table 3.1. Variation from Measured Sdd_21 for Generated BUILT and ACTUAL for a 7" microstrip trace (in dB).

From Table 3.1, the following observations can be made about the 7-inch microstrip traces measured in this section:

1. MEASURED S-Parameters for equivalent traces on the same PCB varied by 0.5 dB around 10 GHz. Interestingly, there's enough variation within a single PCB (sometimes attributed to the fiberglass weave/resin makeup) to cause measurements to not agree with each other from trace to trace. This suggests that it will be difficult to correlate closer than a half a dB on this typical FR4 PCB (at 10 GHz). It may be possible to yield more consistent traces and measurements if a tighter weave in the fiberglass is used.
2. In achieving correlation, knowing the correct loss tangent (lt) value is more valuable than obtaining ACTUAL cross-section data. In fact, assuming the expected lt of 0.020 caused BUILT to correlate better than ACTUAL. Very good correlation can be obtained by knowing the correct loss tangent, which in this case we assume to be 0.023.
3. BUILT S-Parameters varied by 1 dB from MEASURED at 10 GHz. However, knowing the correct loss tangent value decreased this value to 0.3 dB.
4. All methods (MEASURED, BUILT, ACTUAL) show good correlation (within about a half a dB) up through 5 or 6 GHz. In this frequency range, the simulation environment proved to be an accurate analysis tool in predicting the performance of the FR4 PCB, regardless of the availability of ACTUAL or exact loss tangent data.

Recognizing that, for most applications, the accuracy of the S-Parameter data becomes less important as the decibel value becomes greater, we introduce here another way to view the data. In Table 3.2, instead of listing the dB variation from the MEASURED reference we instead calculate the percent variation from a *reference dB* value chosen from the MEASURED data at the given frequency. Mathematically,

$$percent\_variation = 100 * (dB\_variation\_from\_Table\_1 / reference\_dB)$$

For example, at 10 GHz the measured data is approximately centered around 9 dB. From Table 3.1, the BUILT data misses the MEASURED by 1.0 dB. So in Table 3.2 the BUILT percent variation is 100(1.0dB/9.0dB) = 11%.

	3 GHz	**5 GHz**	**10 GHz**	**15 GHz**
BUILT	5%	5%	11%	17%
ACTUAL (lt=0.020)	7.5%	8.4%	13%	19%
ACTUAL (lt=0.023)	1%	2%	3%	8%
MEASURED	1%	1%	4%	11%
Reference dB	3.2	4.85	9.0	12.9

Table 3.2. Percent Variation from the given Reference dB

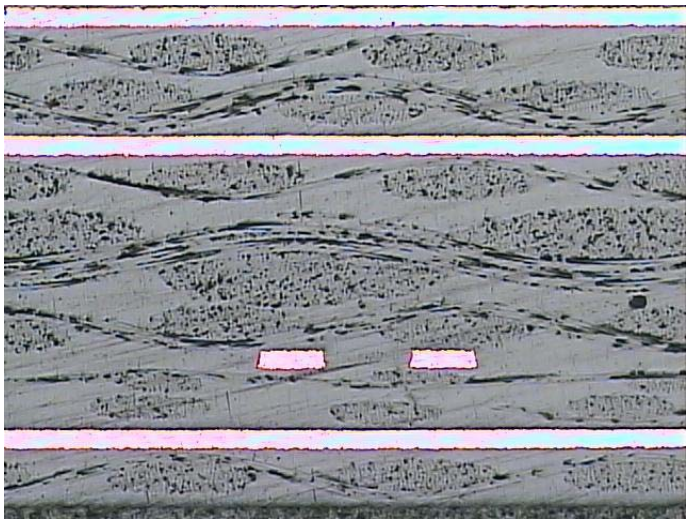
Table 3.2 shows correlation within roughly 10% up to 10 GHz.

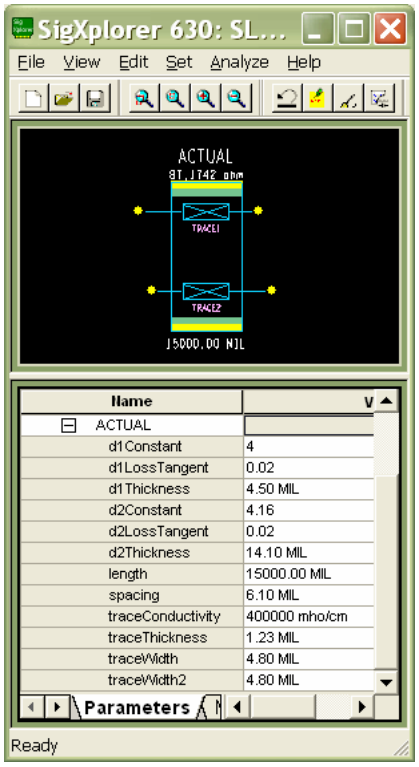
4. Case 2: 15” Stripline Differential Trace Correlation

The 15” stripline samples on the bottom half of the testboard are correlated next. As with the microstrip tests, on the actual board there were 5 differential stripline traces routed identically side-by-side with the same DESIGNED and BUILT parameters to help quantify the variation on a single PCB.

The correlation with generated S-Parameters from Allegro PCB SI 630 was attempted only with ACTUAL values, but in 2 ways: with and without a model for the vias to the stripline trace.

The ACTUAL stripline trace parameters as derived from the cross-section are shown in Figures 4.1. Note the even clearer view of the FR4 weave and resin in the cross-section photo.





Figures 4.1: Stripline Trace Cross-section Photo and ACTUAL Parameters

In order to prepare an accurate analytical via model, the stackup from the testboard must be available to the Via Model Generator (VMG) in SigXp. The stackup can either be read directly from the testboard’s .brd file, or one can use File -> Export -> Techfile from within the PCB SI tool to generate a .tech file that can also be read by the VMG.

The stackup, VMG setup, and via cross-section photo are shown in Figures 4.2 and 4.3.

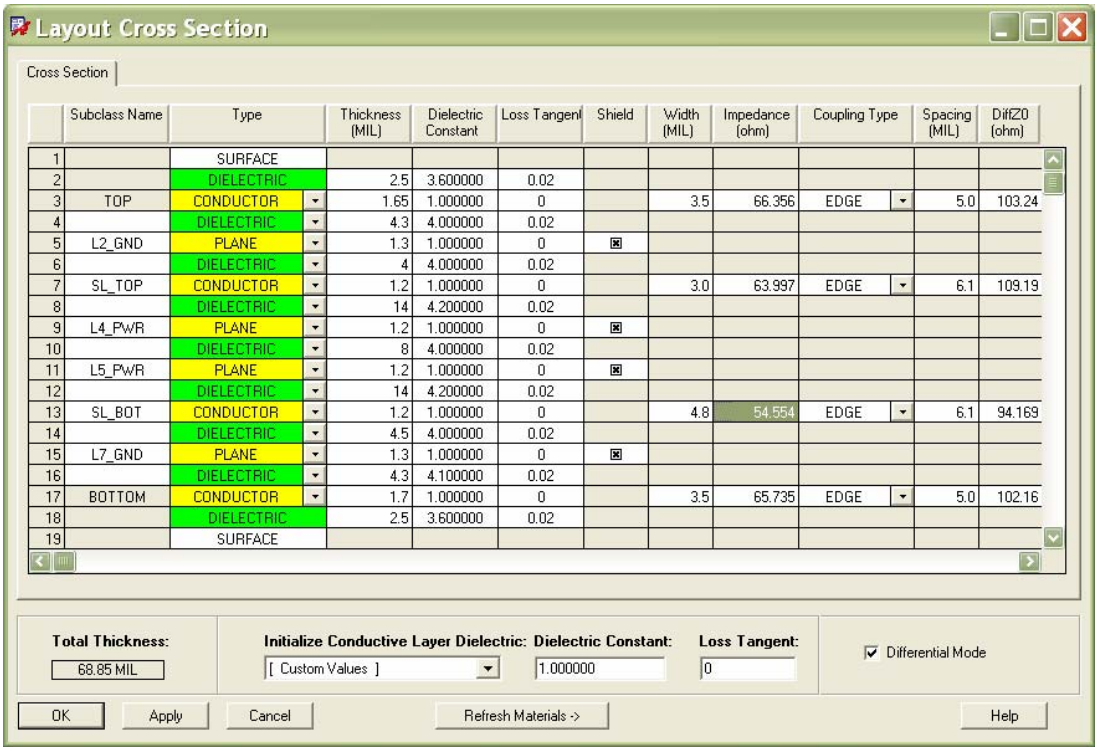
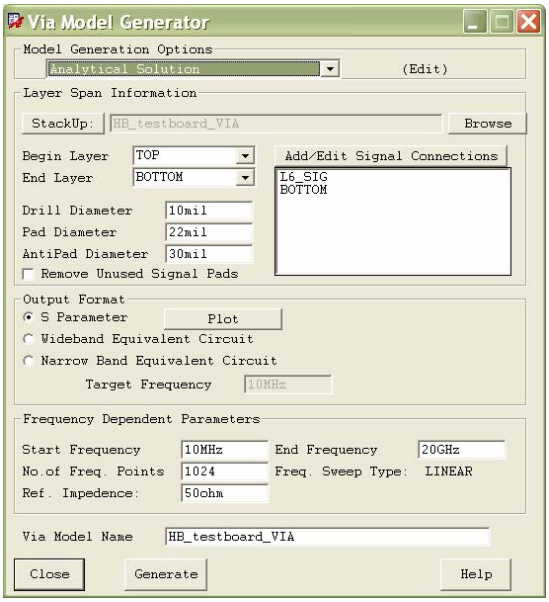
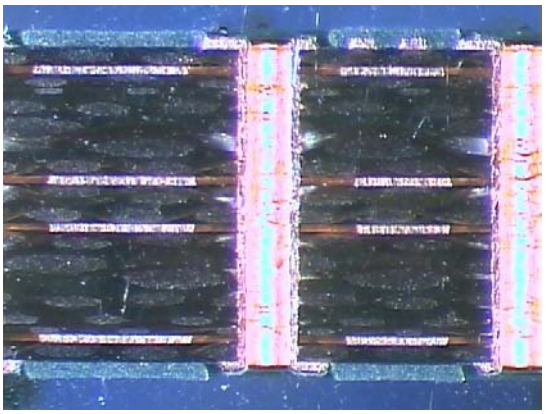


Figure 4.2: Testboard Stackup





Figures 4.3: Via Model Generator and Cross-section Photograph

Once the via model has been generated and available in the interconnect library, SigXp can be configured as shown in Figure 4.4 to generate S-Parameters with the vias in place.

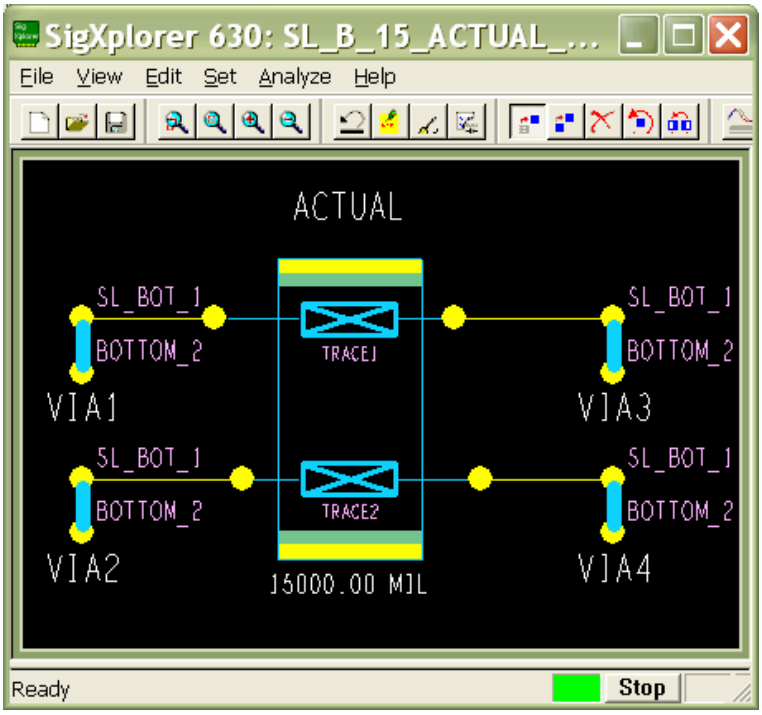


Figure 4.4: Stripline Trace Model with Vias Attached

The correlation plot is shown in Figure 4.5, this time plotting the single-ended S_21.

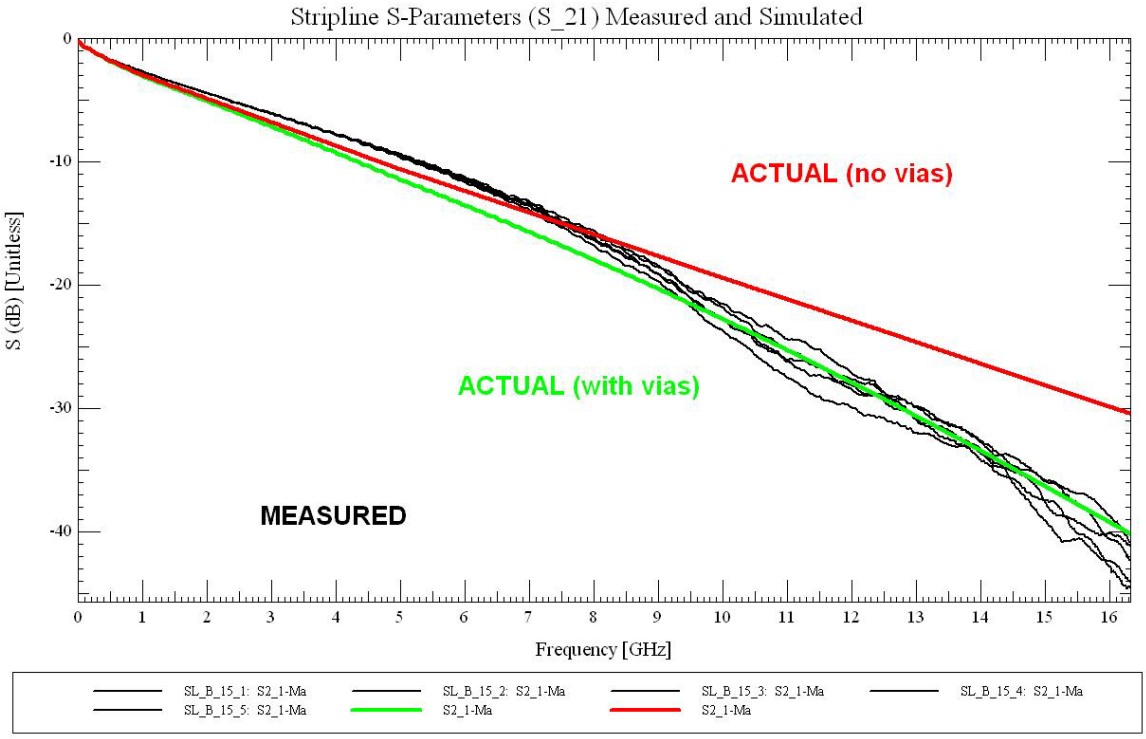


Figure 4.5: Stripline Trace Correlation (S_21)

Qualitatively, you can see that – as with the microstrip – the measured data for the 5 samples starts to spread out above 7 GHz. In this case, the variation around 5 GHz does not look as good as the microstrip example. However, it is simple enough to narrow the gap by adjusting the (approximate) values for the dielectric constant (Er) and the loss tangent (Lt). But we have not done so to highlight the issue that more accuracy may become required for Er and Lt values in common FR4 in the coming years, as well as new computational techniques. And, as can often be seen, when the vias are not in place the miscorrelation in the upper frequency range increases as well.

Common Mistake: Less-experienced engineers often expect perfect correlation, not recognizing that the measurements themselves have a built-in tolerance and variation. Instead, it's better to quantify realistic tolerances and use all tools available to make sound engineering decisions.

The fact that more high-frequency energy is reflected when the vias are in place can be seen from the S_11 plots shown in Figure 4.6.

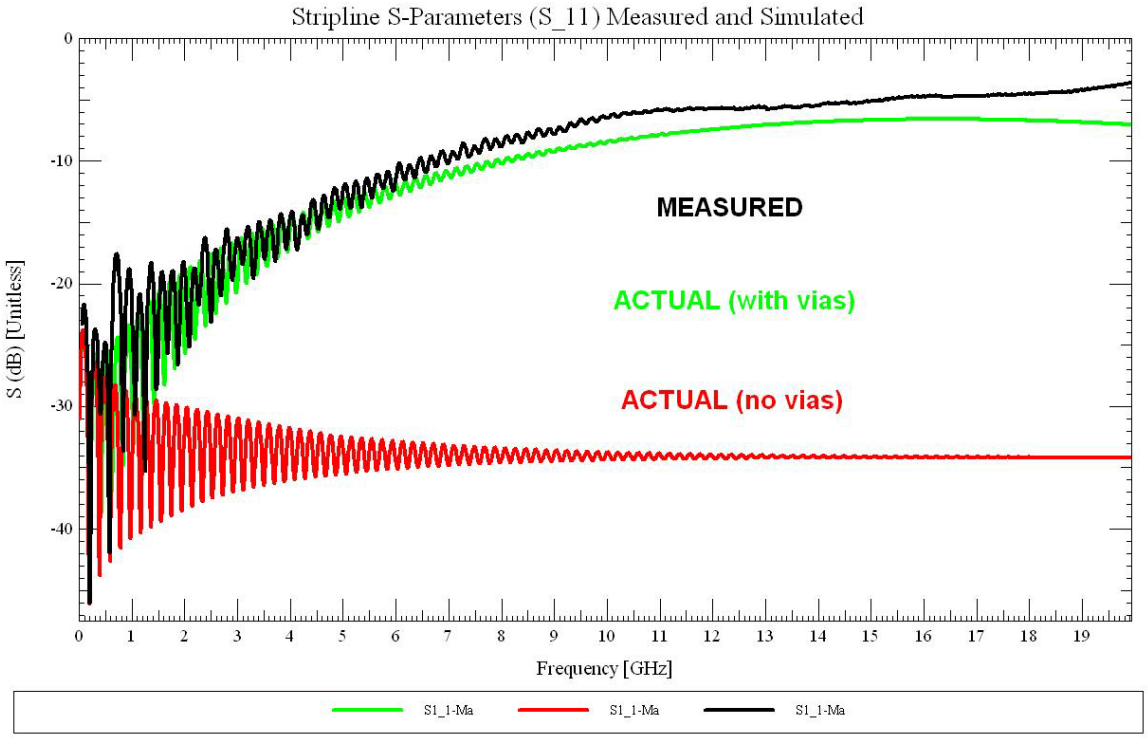


Figure 4.6: Stripline Trace Correlation (S_11)

The plots here show the importance of having a via model in place when correlating and/or simulating a Multi-GHz (MGH) differential signal.

Common Mistake: For simulations at lower frequencies, engineers often ignored vias or approximated them by adding a small capacitance at the location of the via. For effective MGH correlation and simulation, careful and accurate modeling of vias is now required.

5. Case 3: 10” Microstrip with Layer Changes

In this testcase, the 10” trace routing included both top and bottom layer microstrip traces and included 4 layer changes as shown in Figure 5.1. MS_B refers to microstrip on the bottom layer of the PCB, and MS_T refers to microstrip on the top layer.

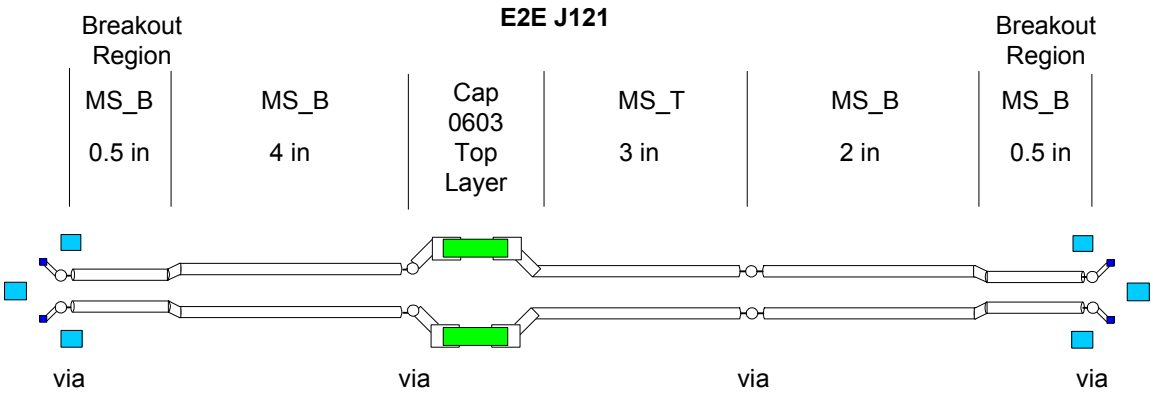


Figure 5.1: Complex Microstrip Configuration

The signal is shown in the physical layout database in Figure 5.2. It is the signal that alternates between the top green (top layer) and blue (bottom layer) signal.

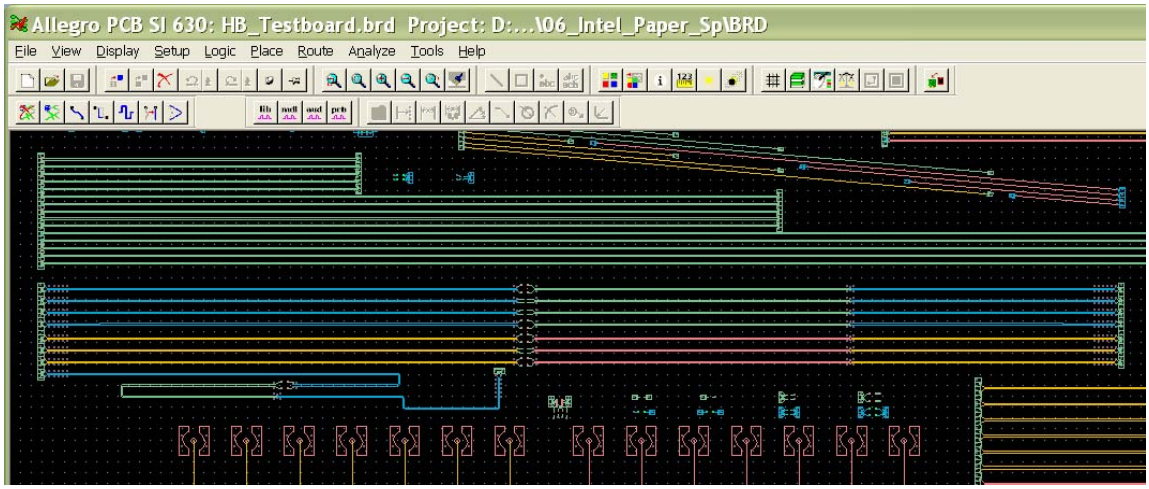


Figure 5.2: Complex Microstrip in PCB Layout Database

When differentially extracted into SigXp for S-Parameter generation, the tool captures all the small (uncoupled) segments to/from vias as well as the longer coupled segments as shown in Figure 5.3.

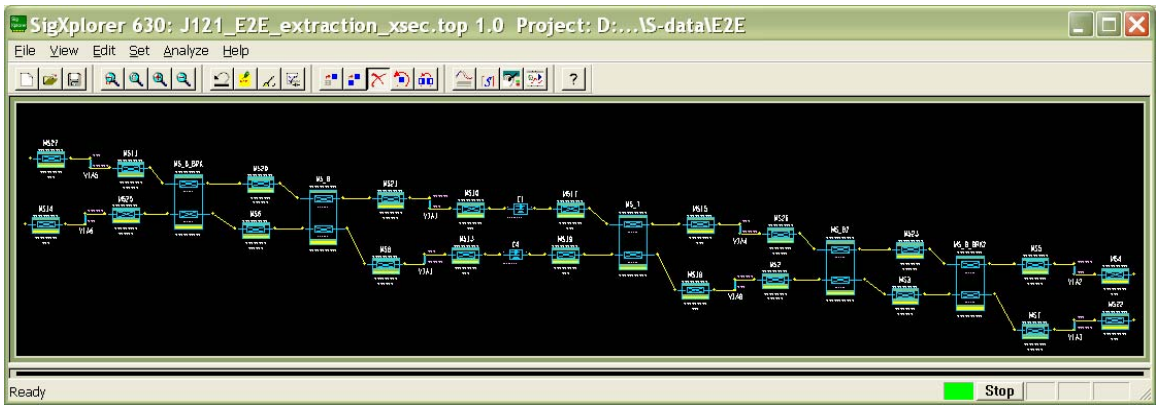


Figure 5.3: Complex Microstrip, Extracted from PCB Database

To study the S-Parameter correlation of this more detailed model, we began with the original extraction and iteratively refined it, examining the correlation at each of the following steps:

1. DESIGN extraction – original extraction from the PCB layout, simple via models
2. ACTUAL extraction - cross-section values corrected to microscope measurement
3. VMG_VIAS – as 2, with extracted via models replaced by SigXp's Via Model Generator's (VMG) analytical models
4. COUPLED_VIAS – same as 3, but replaced single vias with coupled vias (See Appendix B for complete details on how to generate and use coupled via models.)

The 0603 DC blocking capacitor model used a basic pi structure SPICE subcircuit that included both the ESR and the ESL of the capacitor.

The S_21 overlay of the above 4 scenarios versus the measured data is shown in Figure 5.4.

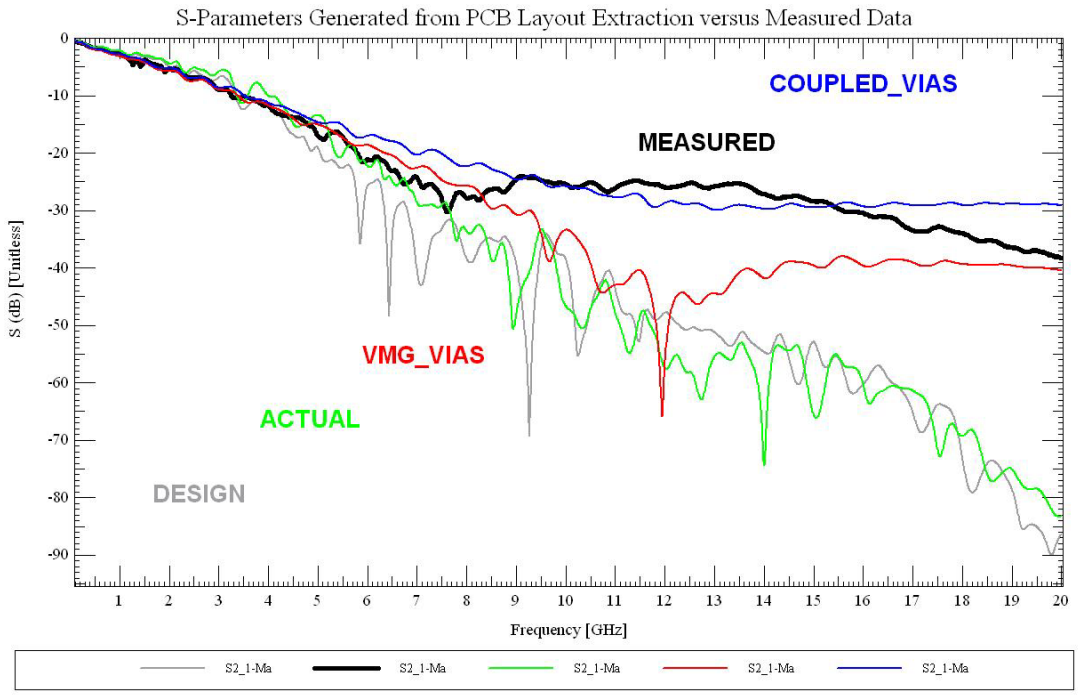


Figure 5.4: Complex Microstrip Correlation (S_21)

In general, as the accuracy of the via model improves, so does the correlation. While the lower frequencies correlate quite well, there are some discrepancies at the higher frequencies. But note that these variations are below the -20 dB point. A blow up of the lower frequency correlation is shown in Figure 5.5.

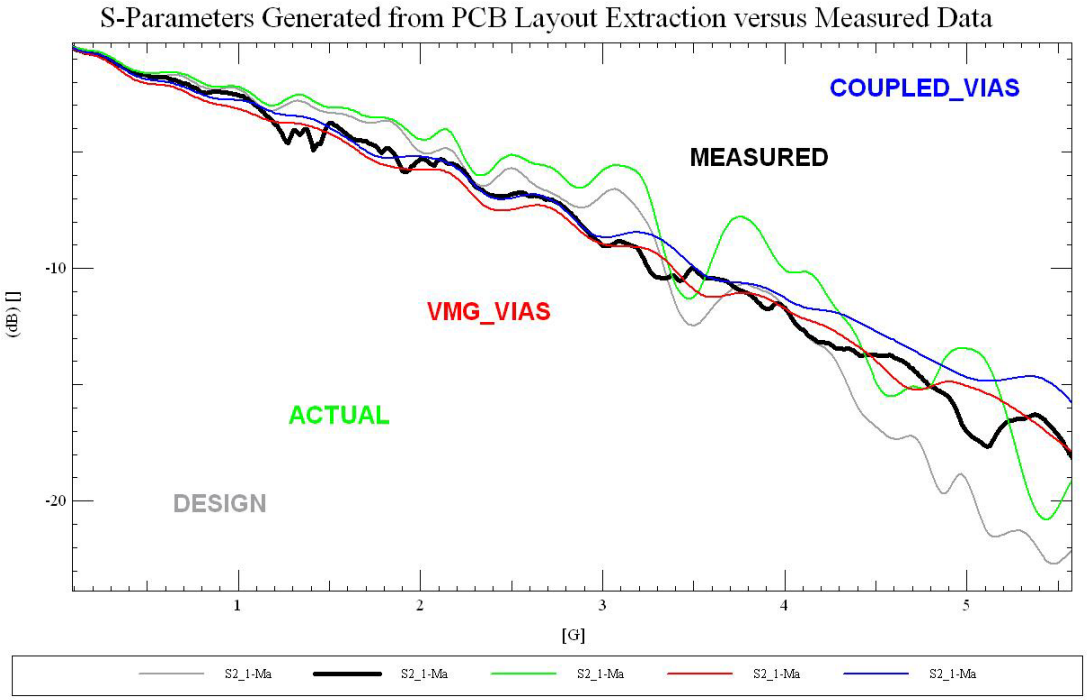


Figure 5.5: S_21 Correlation, 0-5 GHz

In this frequency range the red VMG and blue COUPLED solutions match the MEASURED data quite well, generally staying within 0.5 dB.

The relevance of adding via coupling can also be seen by looking at the S_41 (far-end crosstalk) plot shown in Figure 5.6. S_41 is a good measure of the overall coupling between the two traces in the differential pair over frequency.

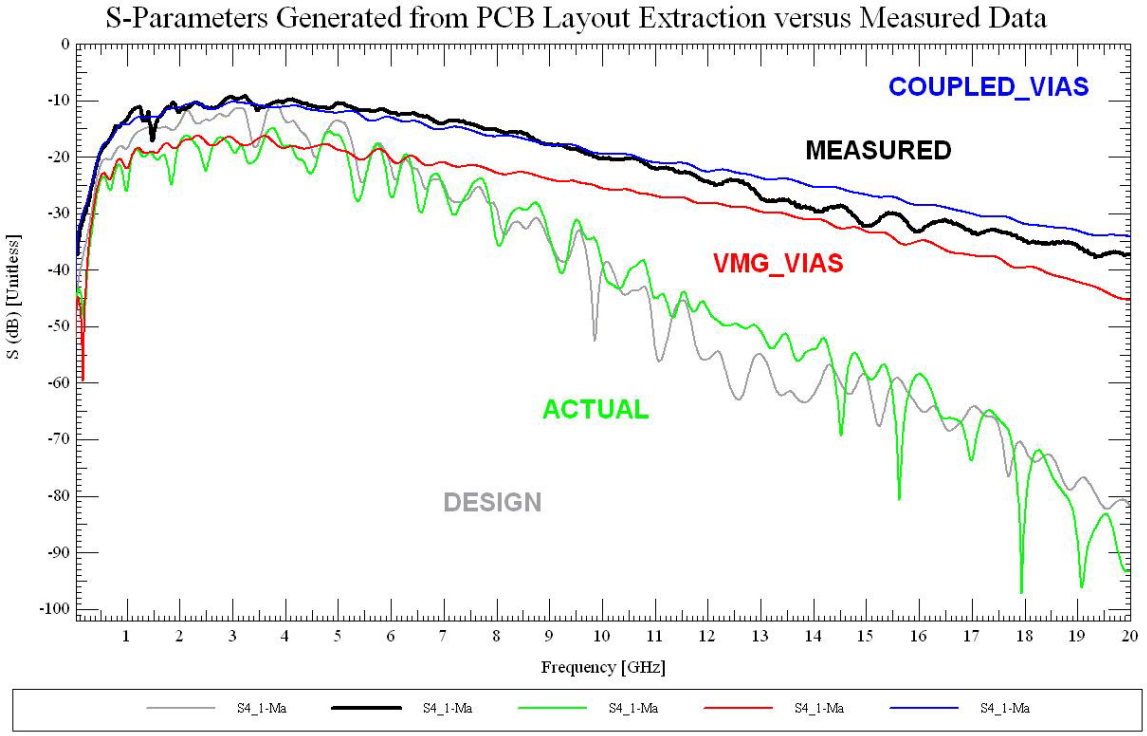


Figure 5.6: Complex Microstrip Correlation (S_41)

In the S_11 (reflection) plot in Figure 5.7, note that the simple via models predict excessive reflection whereas the more advanced models show a more flat response on average over frequency.

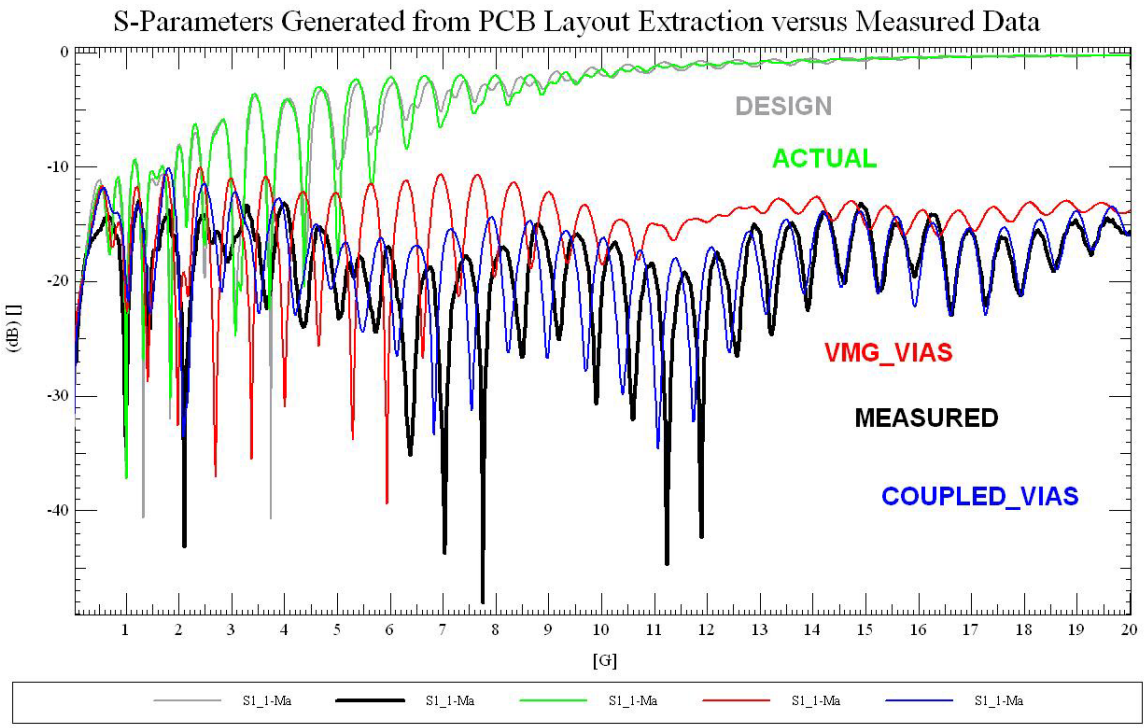


Figure 5.7: Complex Microstrip Correlation (S_11)

As with the stripline example, good correlation has been obtained and the importance of accurate via models has been demonstrated. Over time, we anticipate the correlation of these more complex structures to continue to improve as we learn to model not just the *elements* in the interconnect path, but also their *junctions*.

Common Mistake: Some S-Parameter specifications are described as "differential", meaning that the two differential nodes are referenced to each other instead of ground. This paper has included plots in both styles: differential and single-ended. In general, when the differential pair routing is loosely coupled then S_21_diff ~= S_21_se. Be sure to understand which type of plot is called for in your application. In Allegro PCB SI 630 version 15.2, differential S-Parameters are mathematically derived by using the "ts2dml" program's –DiffSparam option. This will produce an .s2p Touchstone format file with (what is commonly referred to as) the S_dd matrix. There is also a –MixedModeSparam option that will produce an .s4p file that includes sub-matrices of all four differential and common mode combinations (S_dd, S_dc, S_cd, S_cc). Type "ts2dml" at a command prompt for usage instructions.

6. Time Domain Simulation Correlation

S-Parameter data can be used both to examine interconnect loss as well as to produce a model of the interconnect for time domain (TD) simulation. Now that we have examined numerous S-Parameter correlation plots, a logical question might be: "How do these variations in S-Parameters affect time domain simulation?"

To answer this question, we compared the time domain simulation using the 7" microstrip example correlated in section 3. The first step was to model the interconnect in three different ways, annotated as follows:

1. NTL – interconnect modeled with SigXp's frequency-dependent lossy transmission line model populated with ACTUAL values
2. SPO – the NTL model transformed by SigXp into an S-Parameter model to represent the interconnect
3. VNA – the measured Vector Network Analyzer interconnect model translated by Model Integrity into an S-Parameter DML model for SigXp

After adding a PCI Express specification-level transmit (Tx) and receive (Rx) models with the exact same stimulus pattern, we had the three scenarios in SigXp shown in Figure 6.1.

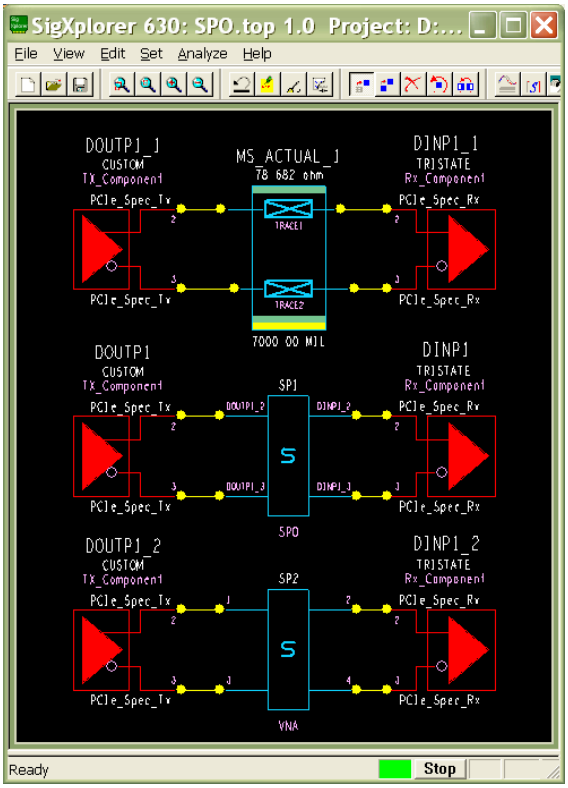


Figure 6.1: Time Domain Simulation Configurations

Plotting the time domain waveforms at the Rx package pin, we observe the time domain correlation shown in Figure 6.2.

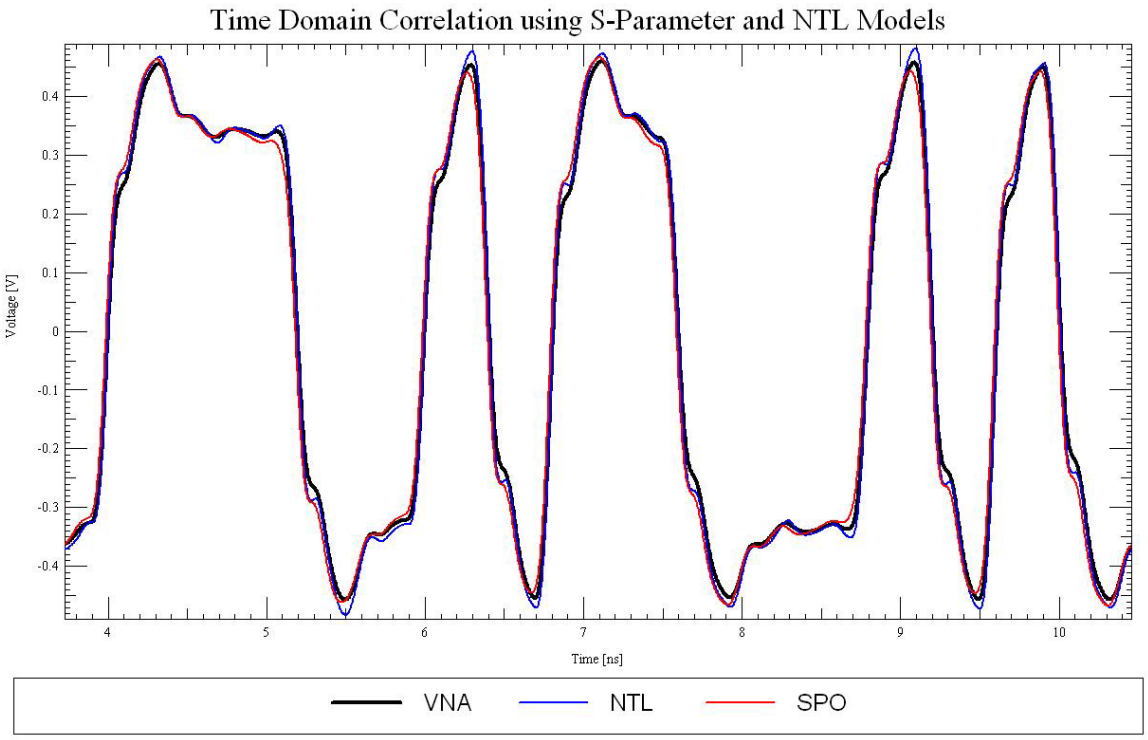


Figure 6.2: Initial Time Domain Correlation

Interestingly, the thicker VNA waveform seems to jump between the blue NTL and red SPO waveforms, and correlate reasonably well with both.

Perhaps a more interesting way to view this type of data is to compare eye heights for the different waveforms, since this is how they would typically be used. The eye diagram of the same data is shown in Figure 6.3.

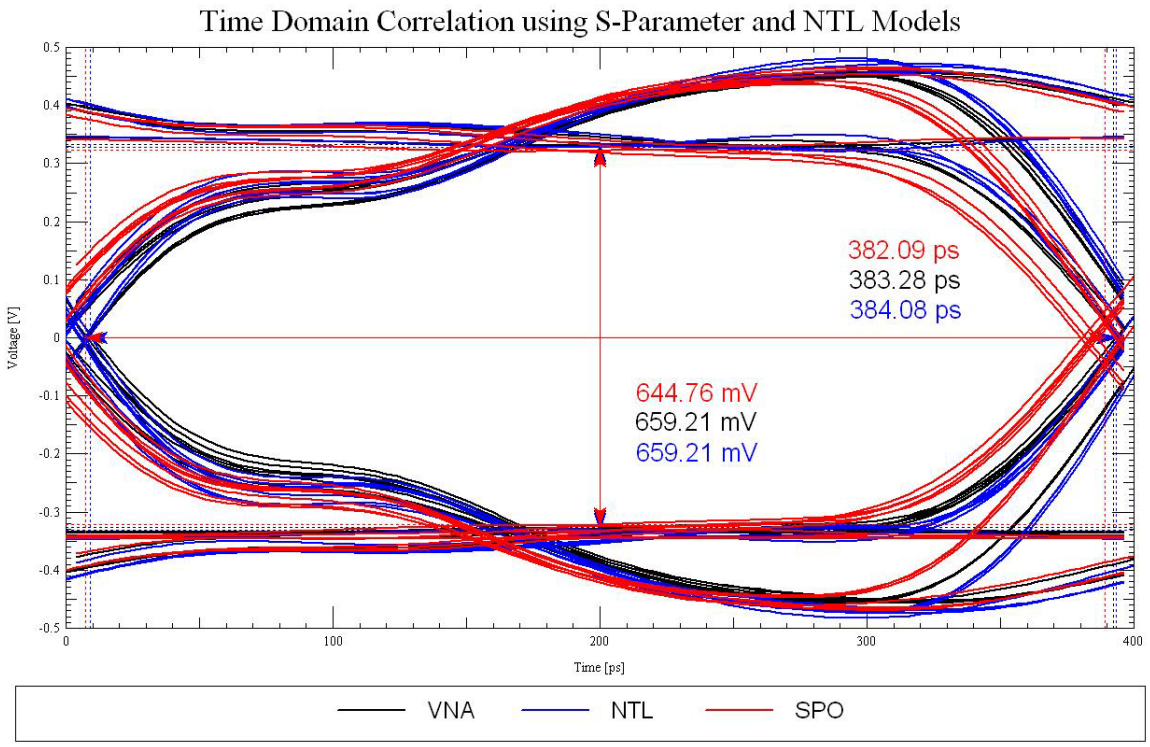


Figure 6.3: Initial Time Domain Correlation, Eye Diagram

From the eye height and width measurements we can see that all heights correlate to about 2% and the widths to better than 1%.

Comparing these plots closer, a few more observations can be made (and perhaps generalized for TD correlation):

1. S-Parameter model waveforms are somewhat phase-shifted in time from the NTL waveform. However, this effect has a negligible (~1%) difference in the eye width measurement.
2. S-Parameter model waveforms appear lossier and seem to transition sooner than the NTL waveform, which appears in as a more measurable difference (~2%) in the eye height.
3. The SPO model and the NTL model it was generated from yield slightly different waveforms.

Exploring point number 3 further takes us into a deeper discussion about the mathematical models involved, which are of course quite different. In fact, the models can be made to correlate quite well by doing 2 things: breaking the NTLs into smaller lengths (in this case, 7 1-inch traces), and setting the "Enforce_Causality" environment variable. This is shown in Figure 6.4.

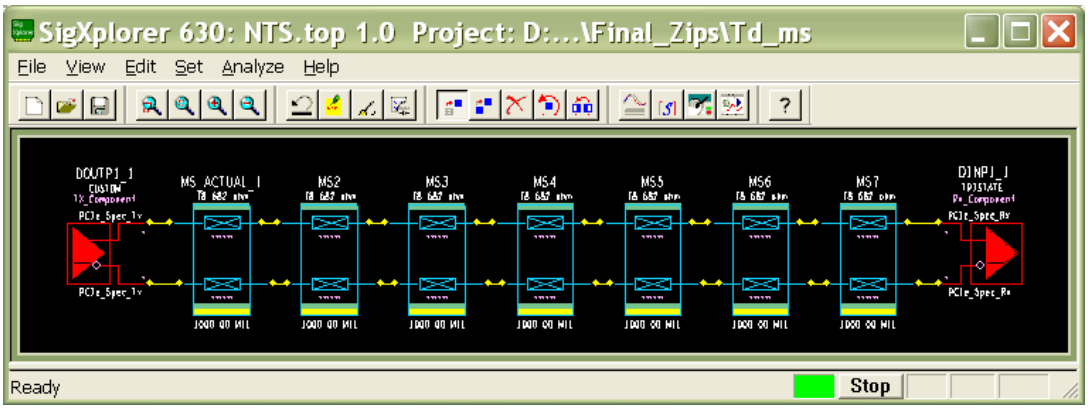


Figure 6.4: Shorter NTL Segments

These new simulations are annotated as follows:

1. NTS – 7-inch NTL model now segmented into 7 1-inch models
2. SSC – the S-Parameter model generated from the NTS circuit with Enforce_Casuality set.

These changes produce the following waveforms overlaid in Figure 6.5.

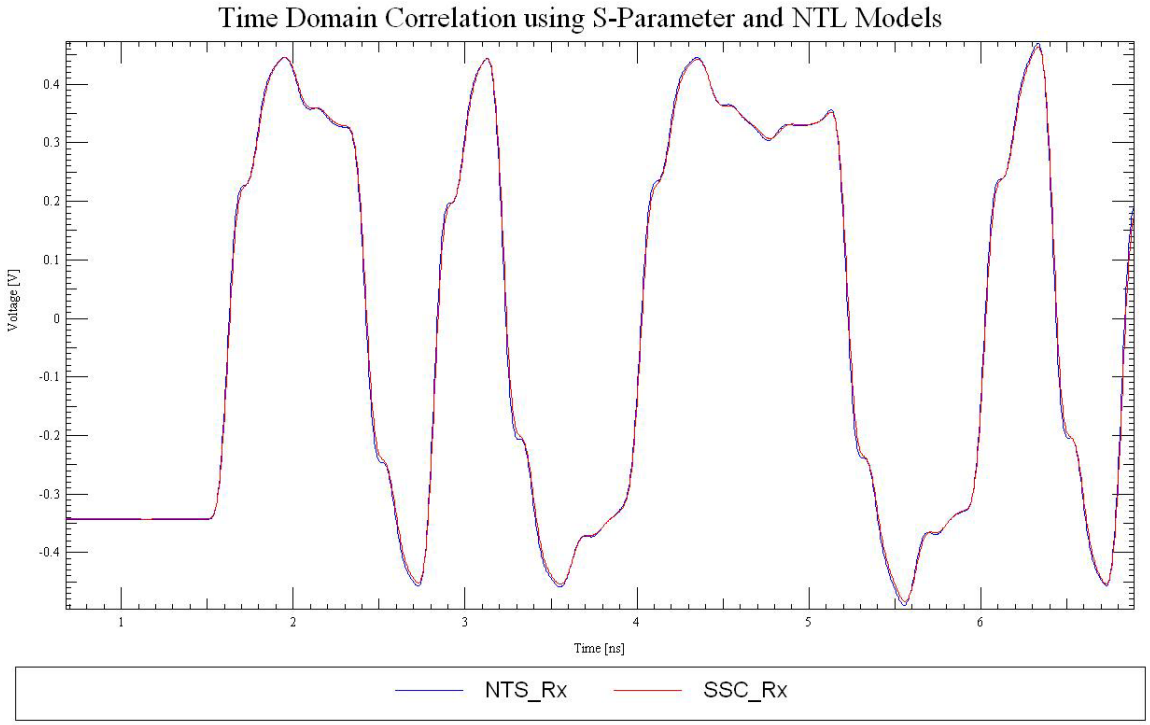


Figure 6.5: Correlating Simulation Methods

As seen above, the correlation is now nearly exact. So, for a little extra effort in some cases, both eye height and width measurements can be brought to well below 1% (to 0.25%) as shown in the Figure 6.6.

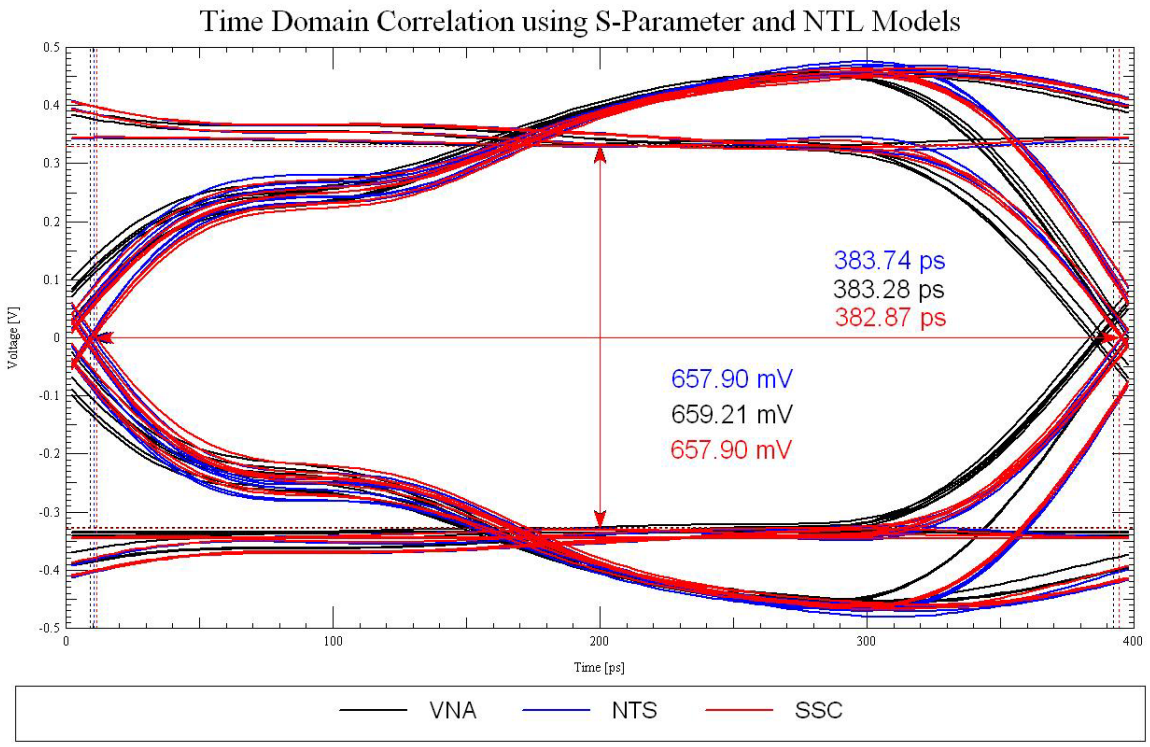


Figure 6.6: Enhanced Simulation Correlation Eye Diagram

Note that there are no noticeable simulation run-time penalties for making these changes, and we found that Enforce_Causality works best on shorter segments as in this example. It is possible to have the tool automatically break long transmission line segments into shorter ones by using environment variable "NtlLengthOptimization" entered in mils. For example, "set NtlLengthOptimization 1000" will force long segments to be broken into smaller sections of 1 inch or less. When using environment variables such as these that affect RLGC (field solution) data, be sure to either delete your .iml file or individual trace models to ensure that the tool replaces older RLGC data.

Common Mistake: When working with S-Parameters, engineers often use lots of data points in hopes of having a more accurate model. Note that a typical 4-port model with 2000 frequency points requires about a 1 MB text file. In Allegro PCB SI 630, each set of S-Parameters you generate is automatically stored in your working DML (library) file. DML files have typically been small, but with S-Parameters they can become very large – even tens or hundreds of megabytes. Depending on your operating system, the tool might become sluggish trying to load and manipulate huge library files. Be sure to delete unwanted S-Parameter models to keep your file size manageable.

7. Conclusions

Allegro PCB SI 630 has been used to generate S-Parameters for both pre-route and post-route differential pairs that were compared with empirical testboard measurements. In the structures tested, correlation within less than 1 dB has been demonstrated up to 7-10 GHz. A similar variation has also been seen when measuring equivalent structures on a single PCB. To make this level of accuracy predictable, it's likely that the industry will be required to improve methods on how Er and Lt values are determined and used. Though correlation is often much better, and occasionally worse, it is reasonable to expect correlation of the mathematically derived S-Parameter models to agree with measured S-Parameters to within about 10%. The importance of accurate via models has also been demonstrated, including the relevance of via coupling. Finally, time domain simulation using the various types of S-Parameter and transmission line models were shown to correlate to within 2% in eye height and width.

About the Authors

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Donald Telian has been involved in high-speed PCB design for over 19 years. At Cadence, he works with industry leaders to develop next generation tools, technologies, and "Design Kits" to support advances in technology. Prior to that, Donald worked at Intel Corporation where he founded and managed the Signal Integrity Engineering group that resolved high-speed design issues for 10 Intel Architecture desktop platforms for Pentium(R) processor-based systems. He also led the design and validation of the PCI Bus electrical specification, originated IBIS modeling, and founded the IBIS Open Forum

APPENDIX A: More Loss Plots for 7” Microstrip Trace

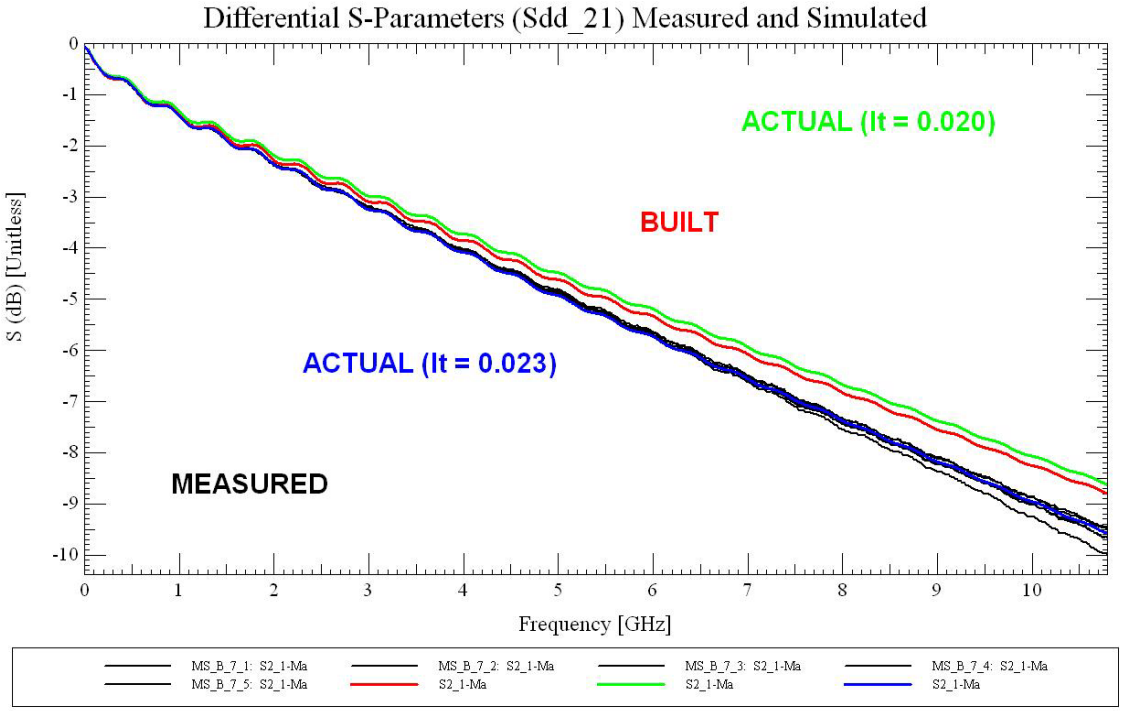

Figure A.1: Microstrip Correlation, 0-10 GHz (zoom-in of Figure 3.4)

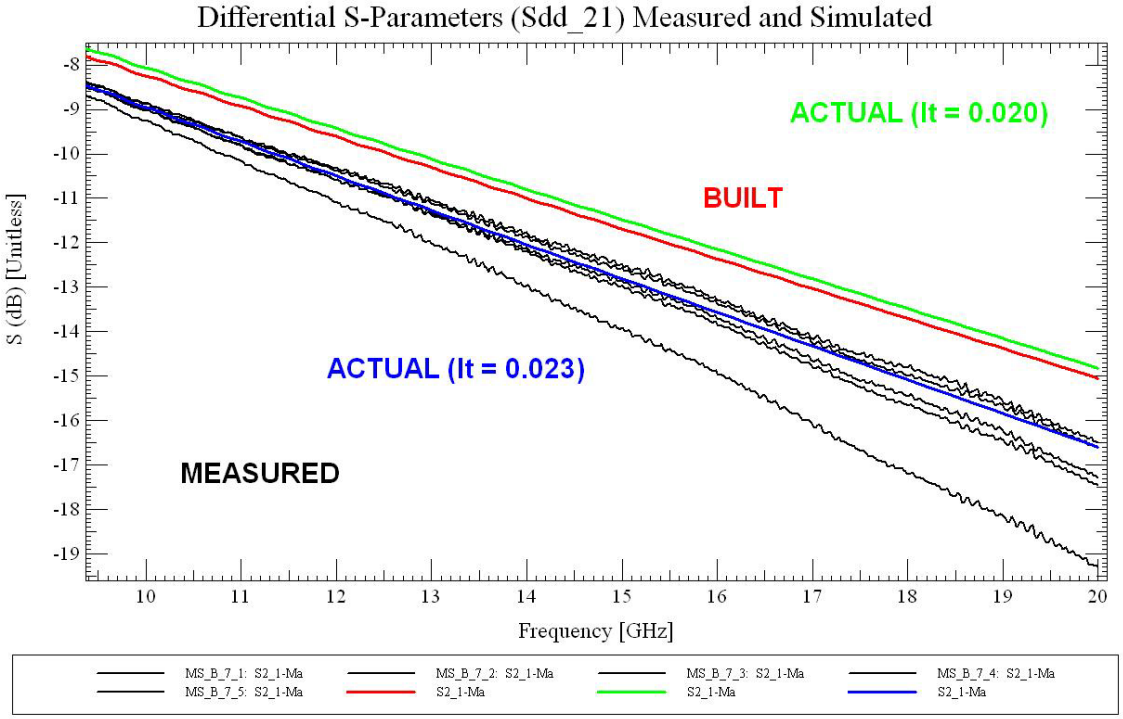

Figure A.2: Microstrip Correlation, 10-20 GHz (zoom-in of Figure 3.4)

APPENDIX B: How to Generate and Use Coupled Vias

To generate coupled via models, similar to those used in section 5, follow these steps:

1. Be sure you're using an Allegro PCB SI 630 version 15.2 ISR dated later than August 1, 2004.
2. Use this procedure for coupled vias that are plated all the way from the top layer of the PCB to the bottom layer.
3. Generate a model for one of the vias in the Via Model Generator (VMG).
4. Find the *.in file for the via you just made in your project directory. Open a command window and type:

   ```
   FSvia <input_single_via.in> 4 <start_frequency> <end_frequency>
   <number_frequency_points> <diffpairD2DinMil=xyz>
   ```

   …where xyz represents the center-to-center distance of the via pair, in mils.

5. Step 4 will generate an S-Parameter 4-port coupled via model in Touchstone format named dp_via_sparam.s4p. Browse to this file.
6. Open the Touchstone file in Model Integrity, right-click on it, and Translate to DML to produce a model for SigXp. Load this model into your library.
7. Browse to the model and place it on the SigXp canvas. The ports are numbered as shown in Figure B.1.

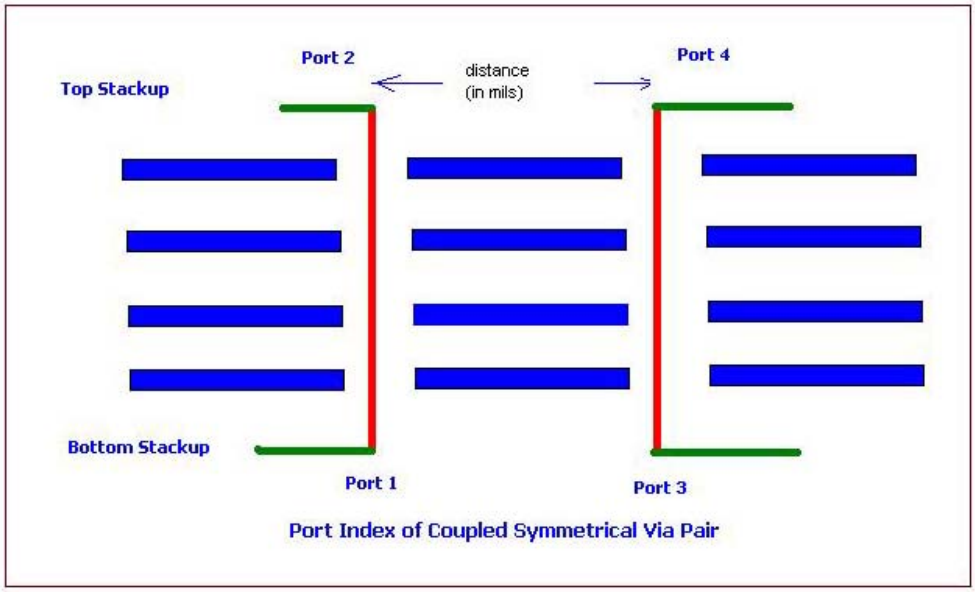

Figure B.1: Port (Node) Numbering for Coupled Vias