How to Build Fast and Accurate Multi-Gigabit Transceiver MacroModels

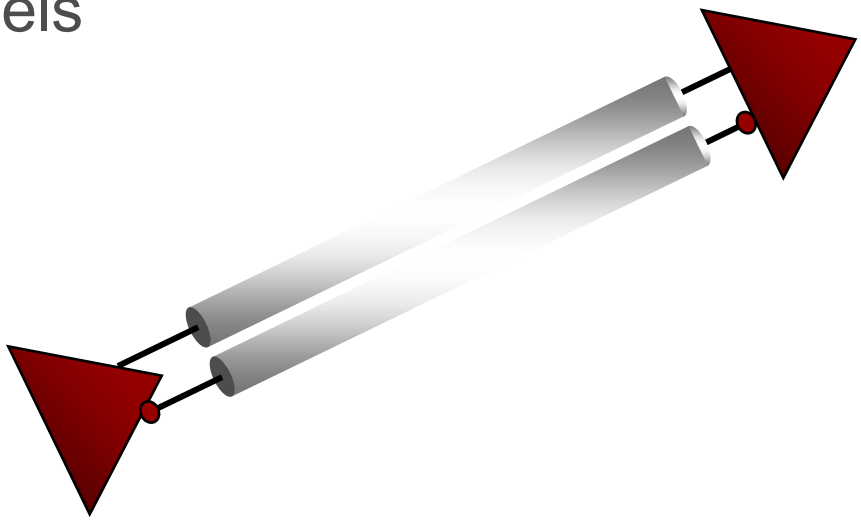
Donald Telian

About the Presenter

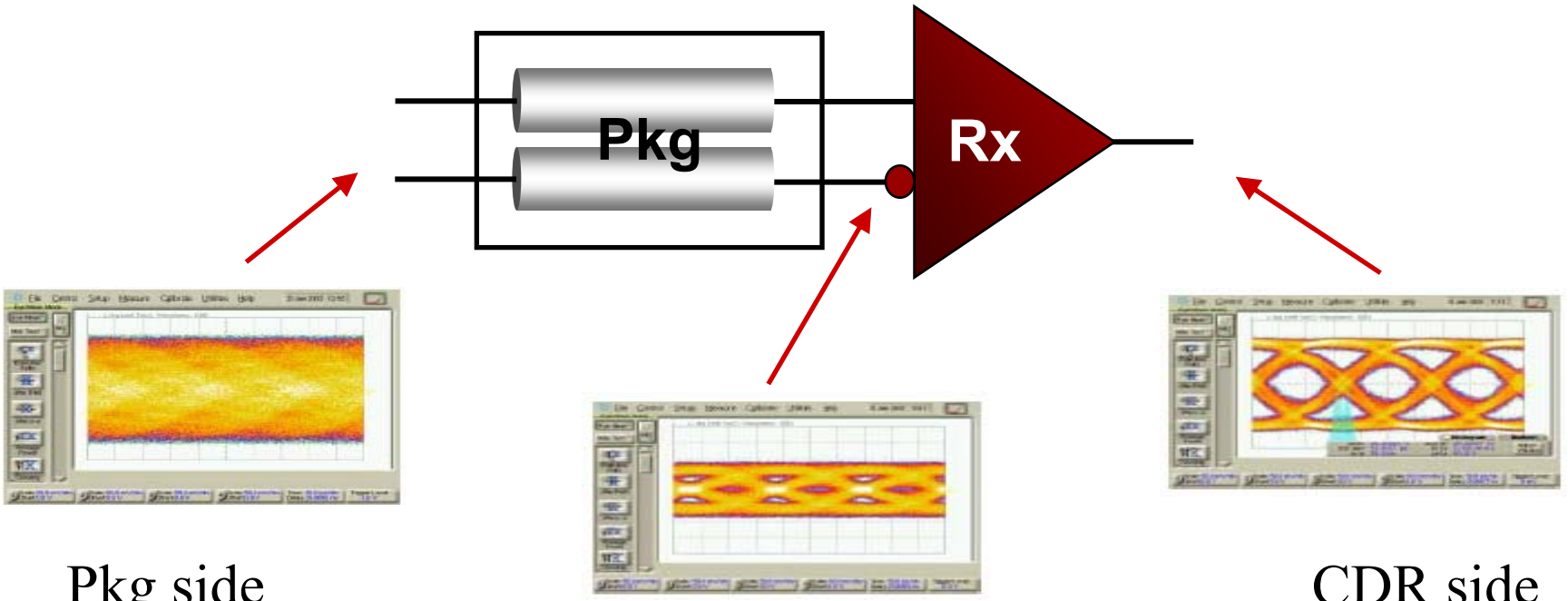
Donald Telian has been involved in high-speed PCB design for over 18 years. At Cadence, he works with industry leaders to develop next generation tools, technologies, and "Design Kits" to support advances in technology. Prior to that, Donald worked at Intel Corporation where he founded and managed the Signal Integrity Engineering group that resolved high-speed design issues for 10 Intel Architecture desktop platforms for Pentium(R) processor-based systems. He also led the design and validation of the PCI Bus electrical specification, originated IBIS modeling, and founded the IBIS Open Forum.

AGENDA: Multi-GigaHertz MacroModels

1. Why Multi-GigaHertz (MGH) Simulation?
2. About SPECCTRAQuest MacroModels
3. Understanding Pre-Emphasis
4. Building MacroModels
5. Demonstration
6. Summary



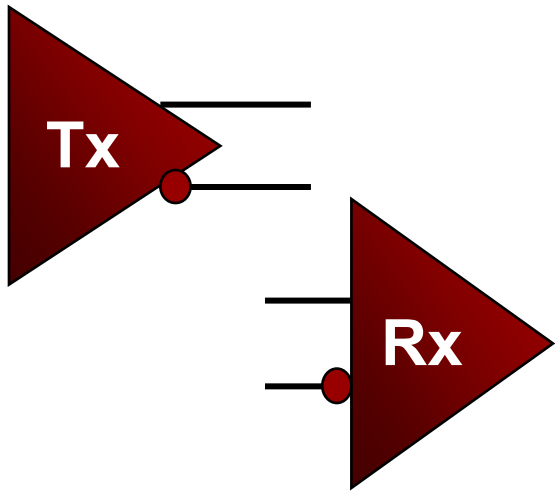
Why Simulate MGH Links?



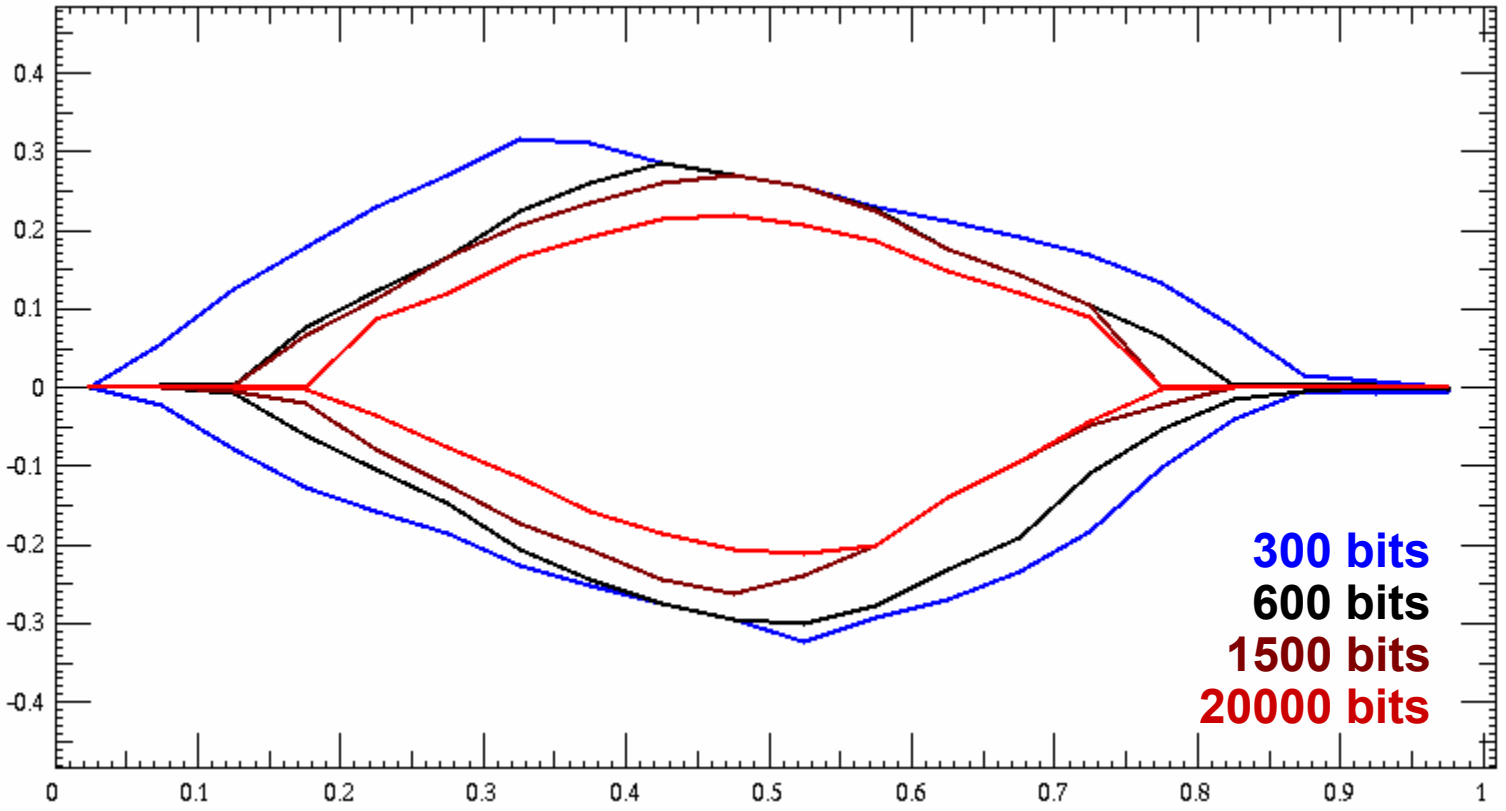
- Externally measured signal can not be distinguished (acute at 5+ Gbps)
- This requires probing *inside the IC* to do the measurement
- Must perform system simulation to engineer solution
- PCI Express guideline: “all interconnect paths must be simulated to ensure proper performance and compliance”

Tx/Rx Model (Simulator) Options

- Transistor-Level Model
  - \+ Accurate, available from IC design process
  - – Long simulation time
- IBIS
  - \+ Fast simulation, wide vendor support
  - – Rarely used for MGH applications
  - – No simple solution for pre-emphasis
- MacroModel
  - \+ Fast simulation, nodal language
  - – Can be challenging to build

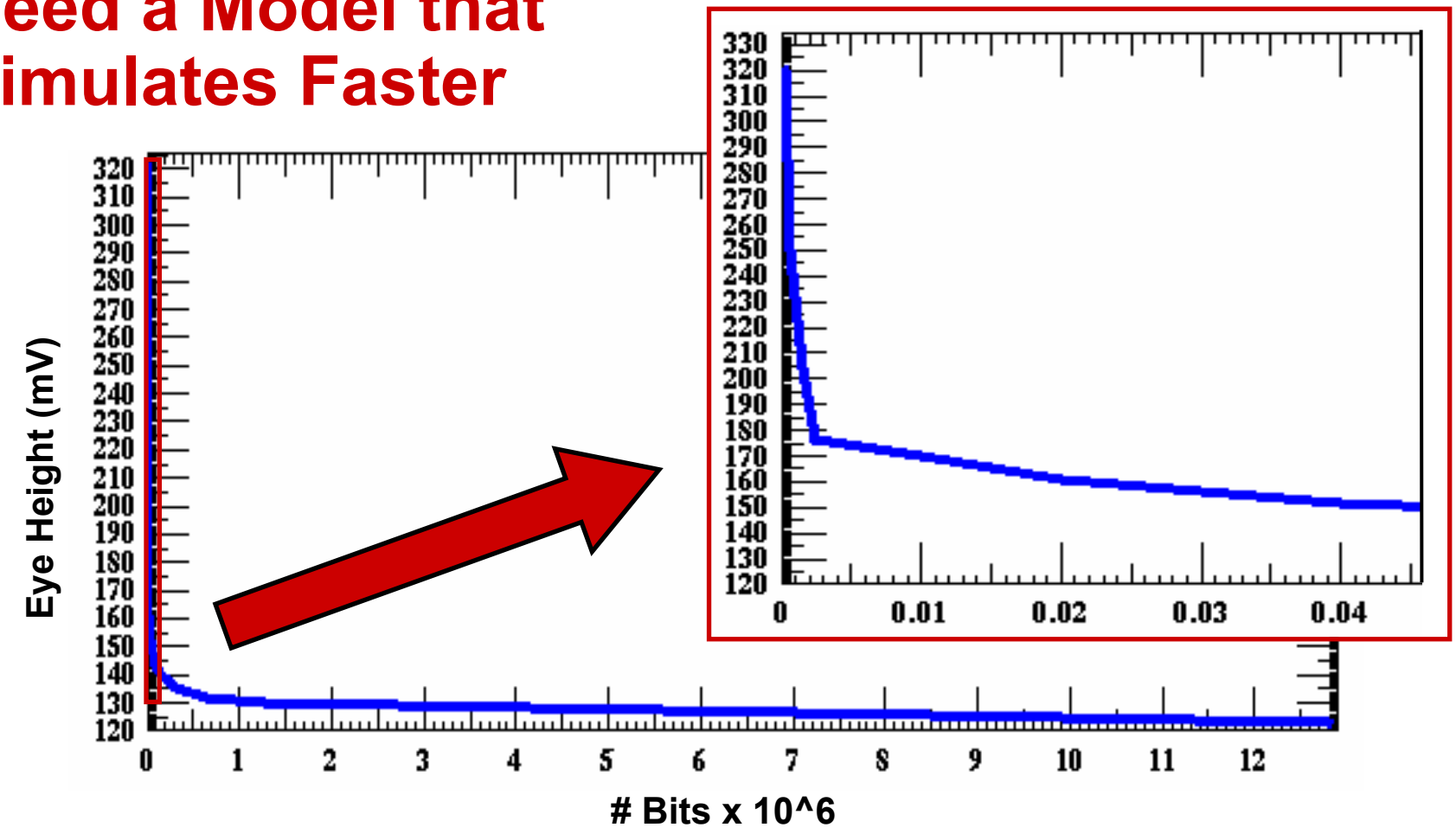


MGH Serial Link Simulation Consideration



- Contour plots of interior eye region vs. # bits
- Eye shrinks with more bits simulated
- Need to simulate lots of bits to verify design

Need a Model that Simulates Faster



- It takes 1 million bits to round the knee on the curve
- Typical transistor-level simulation would require 420 days
- MacroModels typically simulate hundreds of times faster

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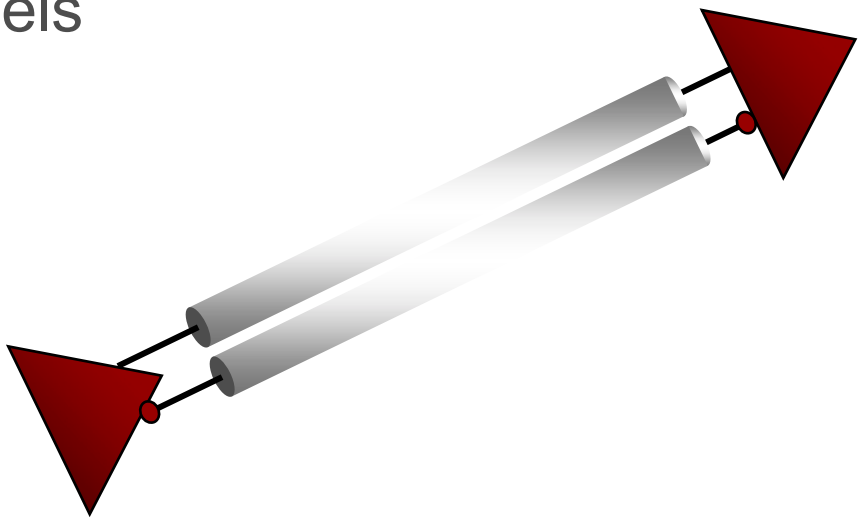
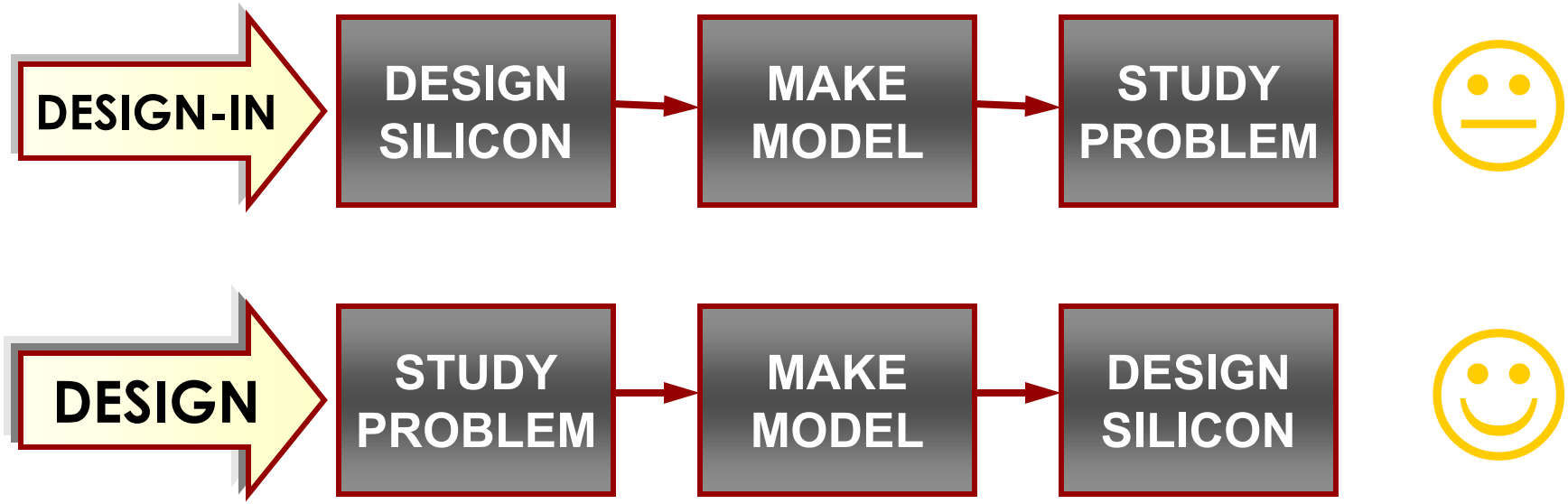


SPECCTRAQuest MacroModels

- SPECCTRAQuest feature for many years now
  - Nodal, behavioral, spice-like (espice) syntax
  - Includes special elements unique to high-speed PCB
- MGH MacroModel templates can be downloaded now
  - Pre-emphasis/equalization drivers/receivers on www.specctraquest.com
  - http://register.cadence.com/register.nsf/macroModeling?OpenForm
  - These templates will be used in this presentation
- PCI Express MacroModels available in March (Optimize -> DesignKits)
- More MacroModel info at:
  - http://www.specctraquest.com/Optimize/O_Models.asp#macromodels
- Useful to model both known and “what_if…” behaviors

MacroModels: Good for Both Flows



- In Design-in flow, MacroModel conforms to silicon behavior
- In Design flow, MacroModel determines ideal silicon behavior
  - More and more IC design problems are solved this way

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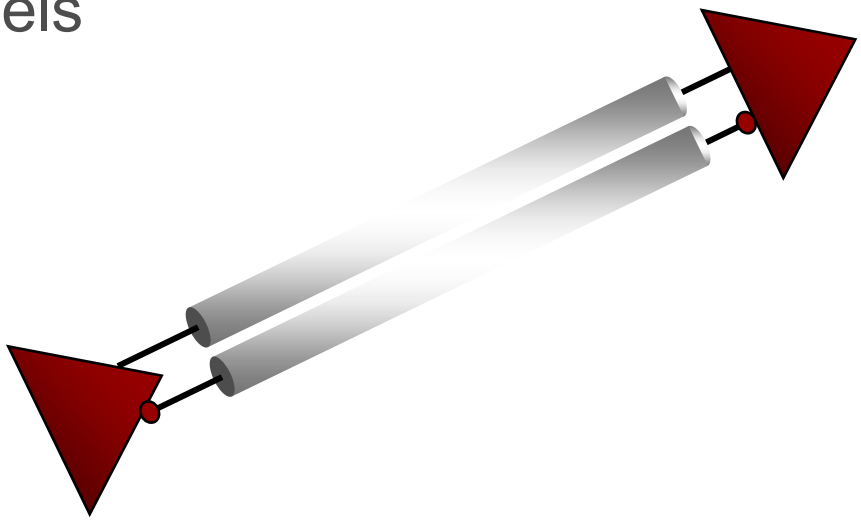
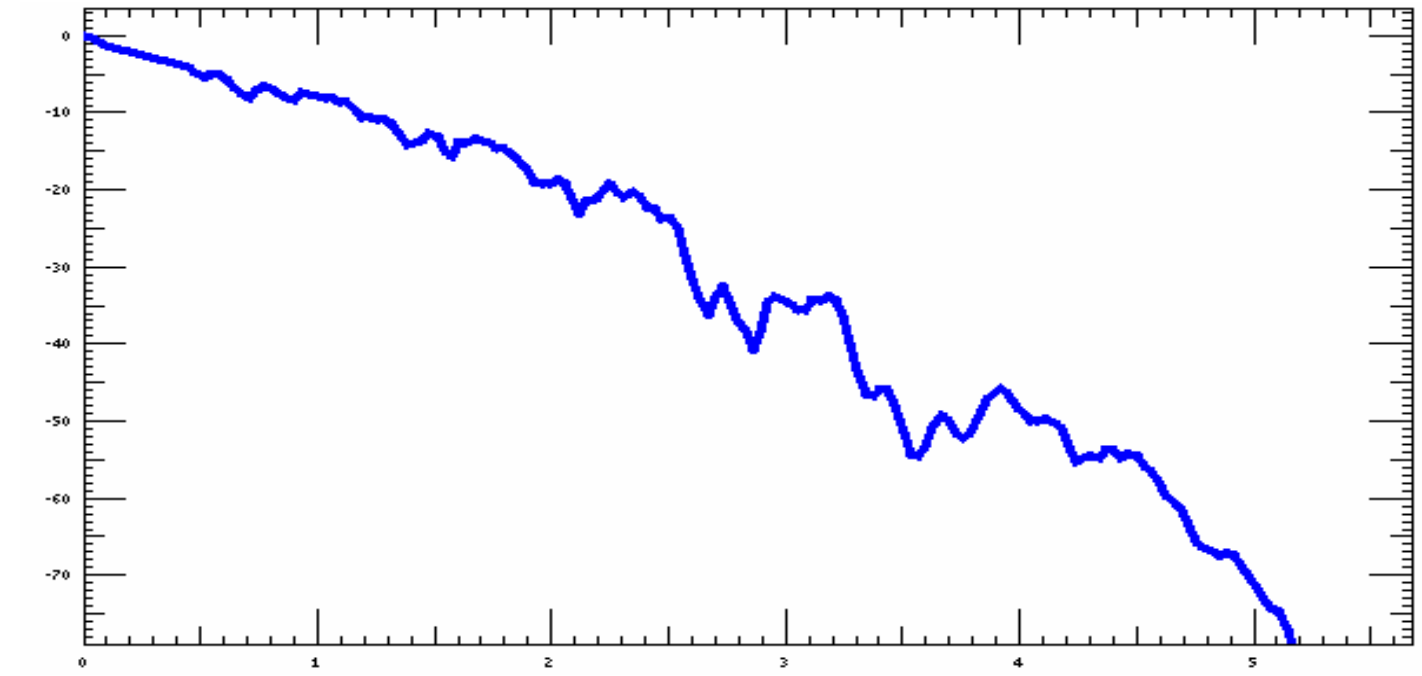
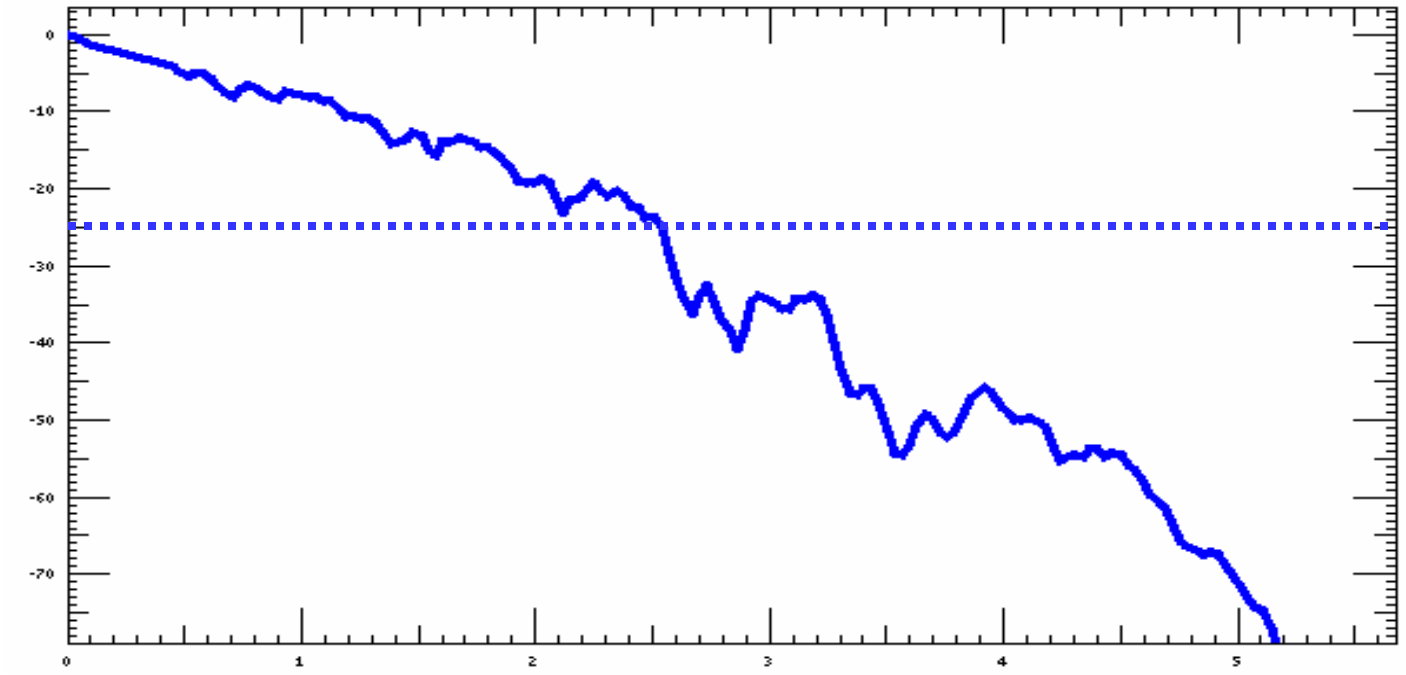


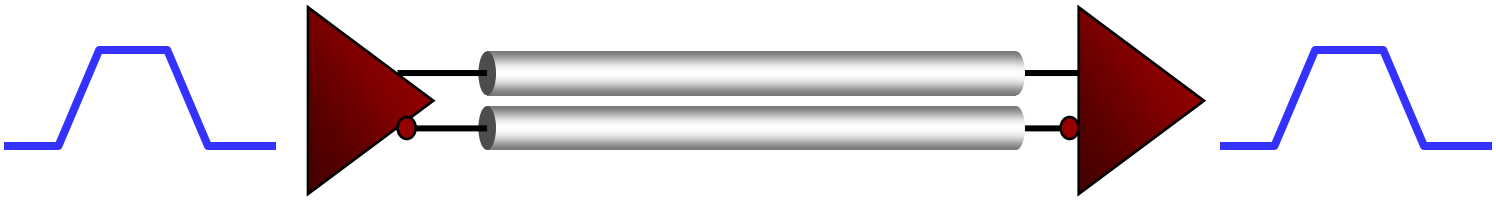
Main Challenge: Loss Compensation



Channel loss causes decrease in signal amplitude

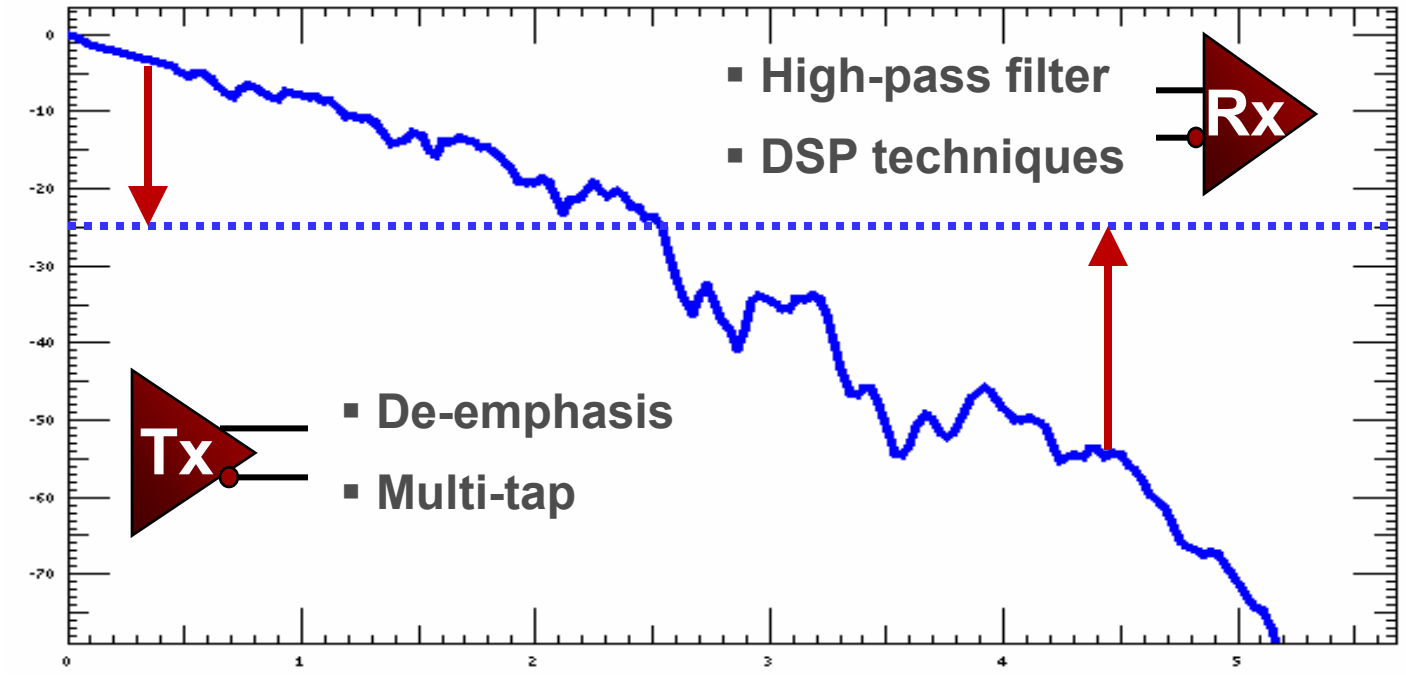
Goal: Flatten Channel Response

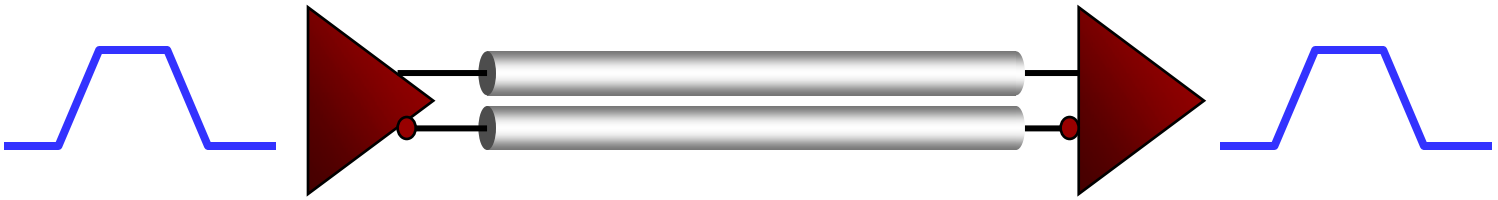




Attenuate low frequencies, boost high frequencies

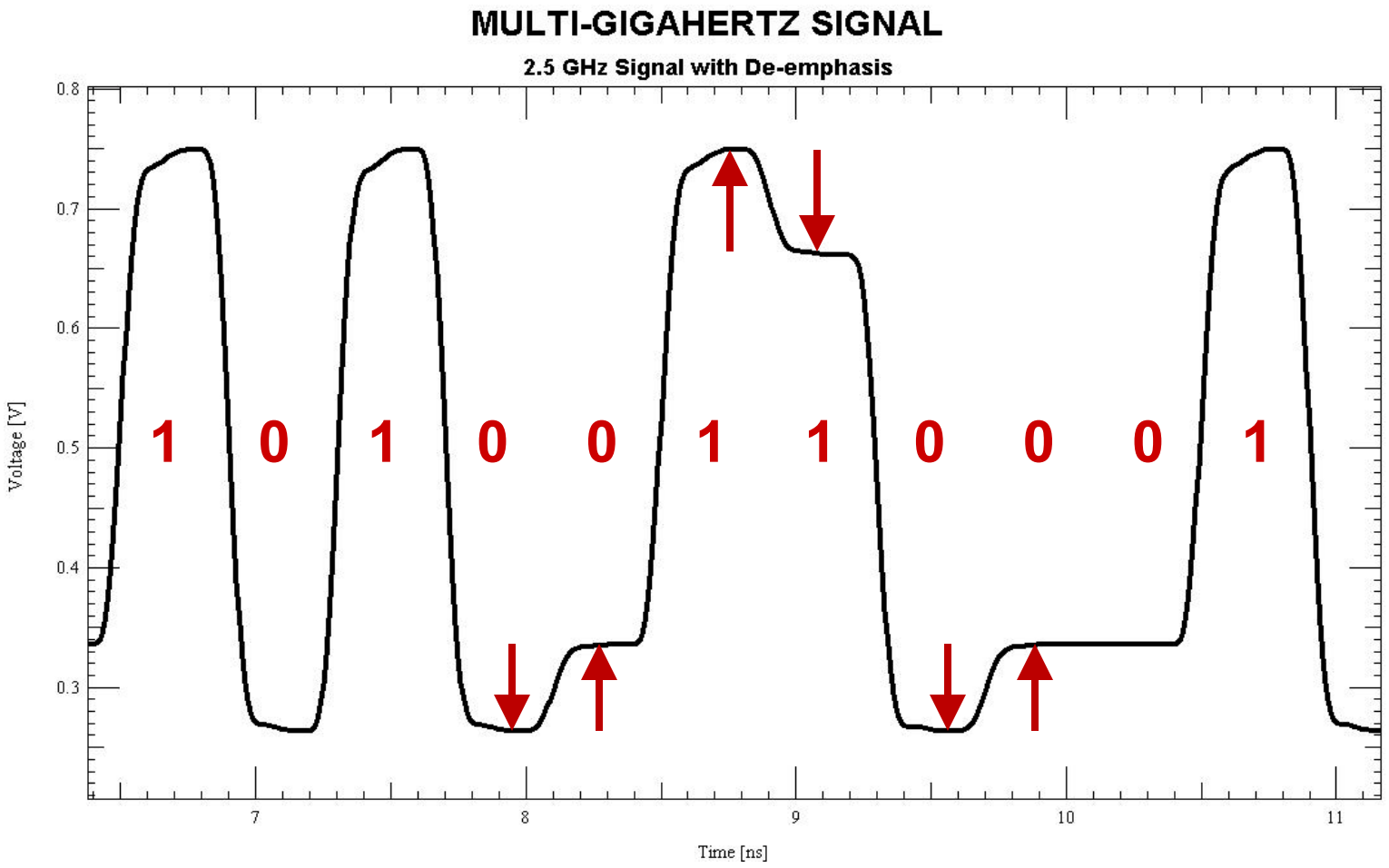
Some Common Techniques





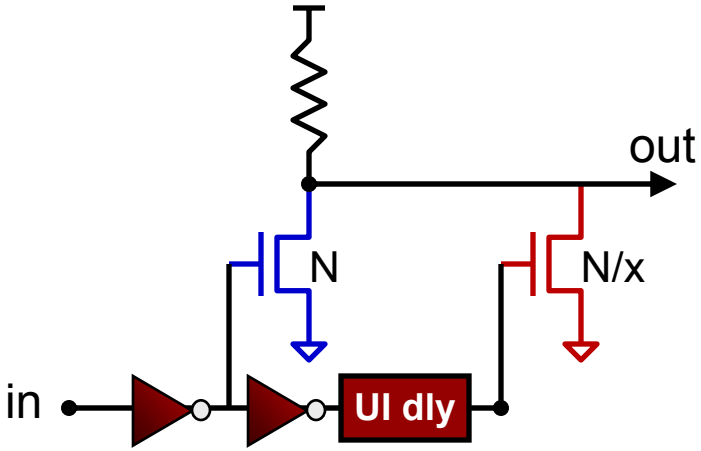
Attenuate low frequencies, boost high frequencies

Transmit Pre/De-Emphasis



Boost high frequencies, attenuate low frequencies

Tx Implementation



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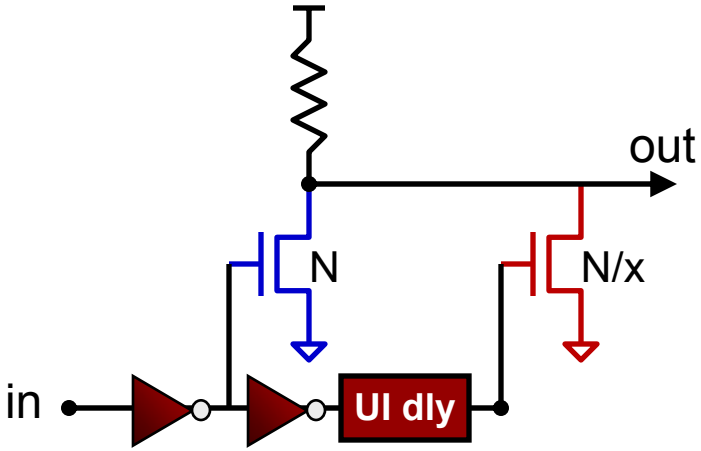

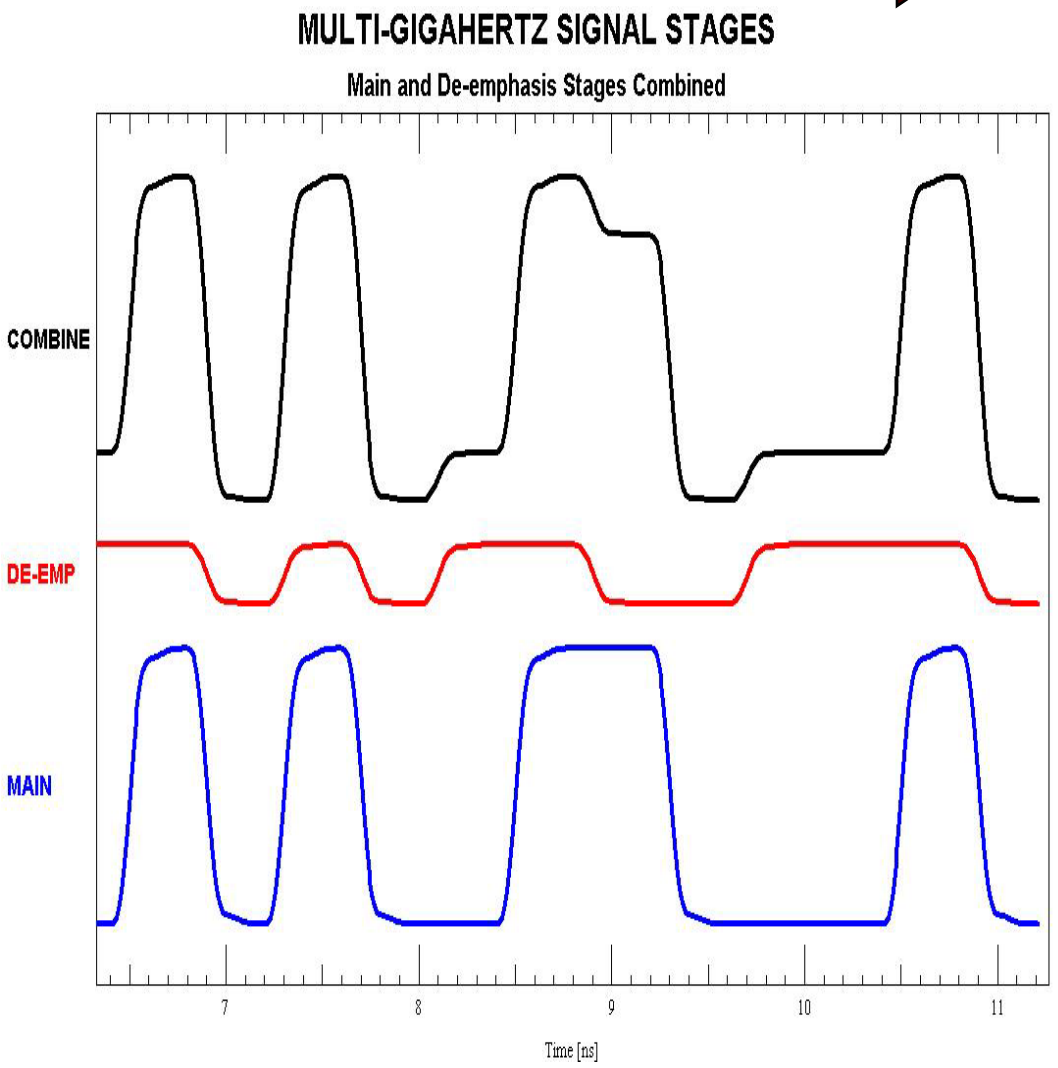

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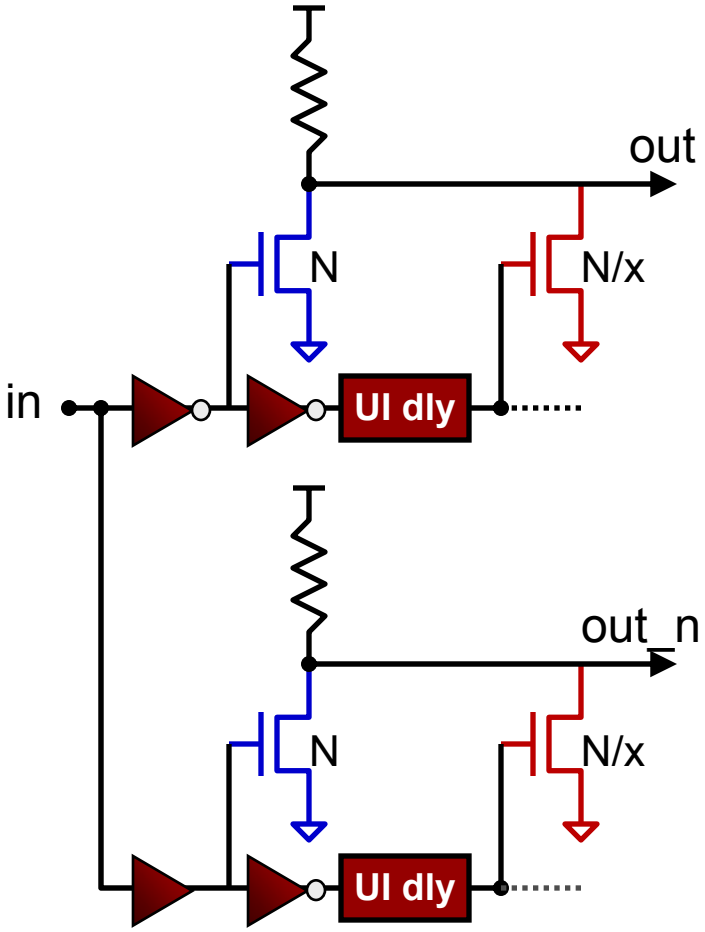
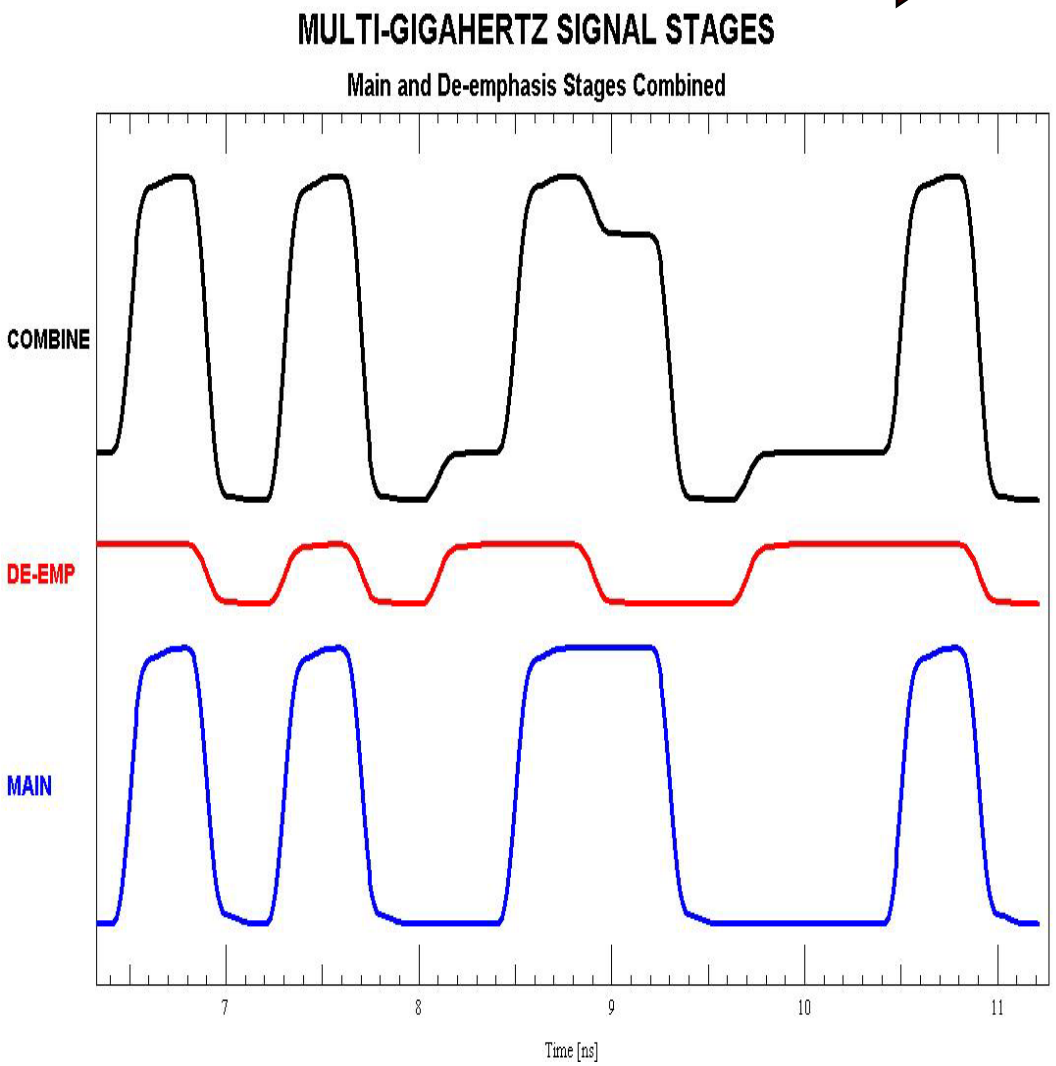
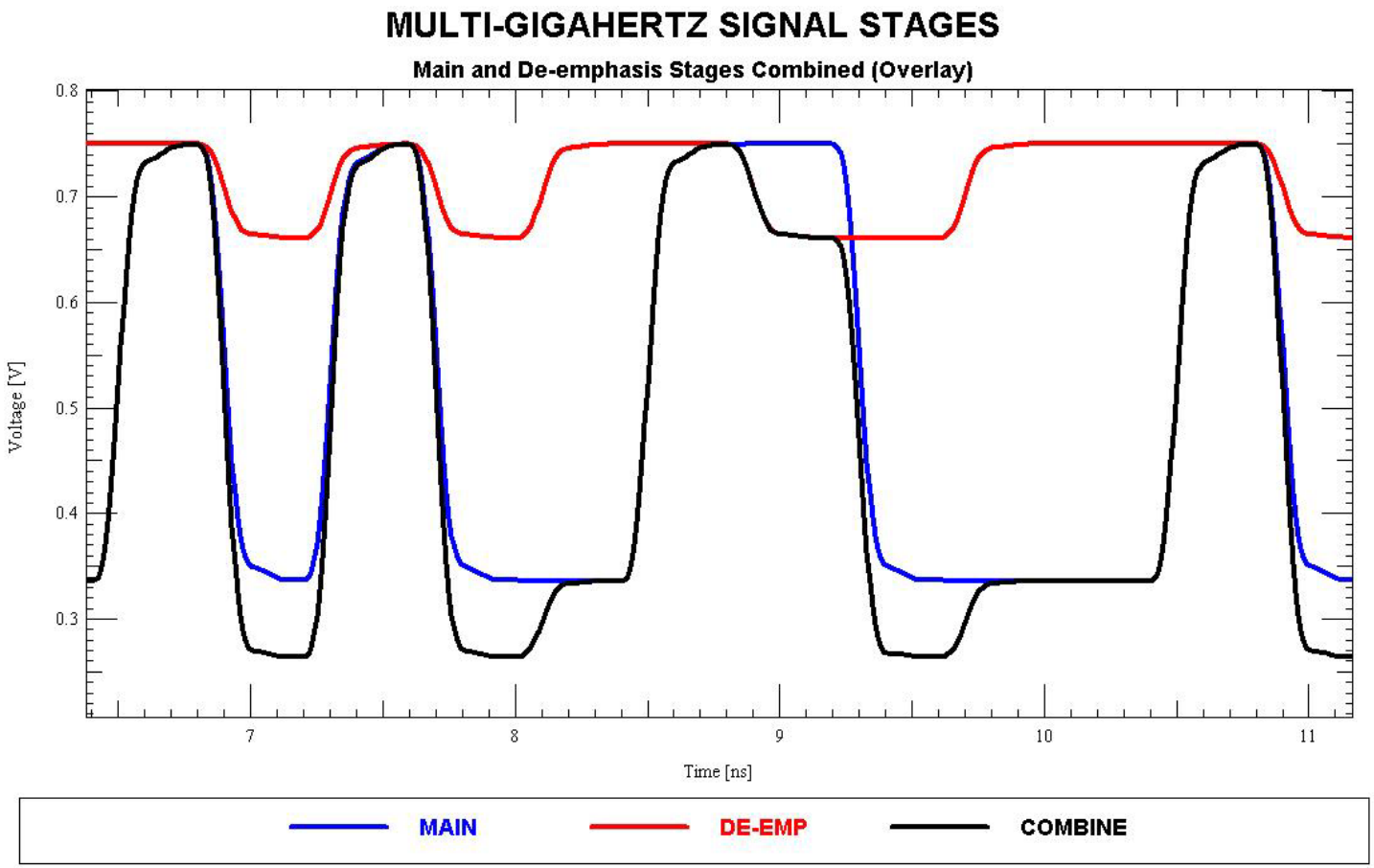


Multi-tap: choose x, y, z



Another View



- Main stage **(blue)** shows basic digital signal
- De-emphasis stage **(red)** shows the scaled-down, inverted, delayed signal
- Combine these **(black)** to see the multi-gigabit signal

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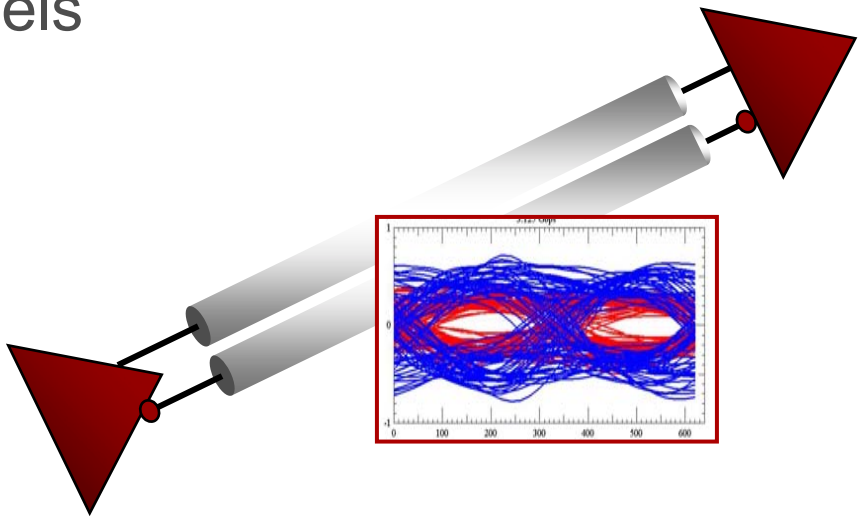
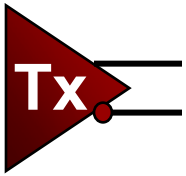
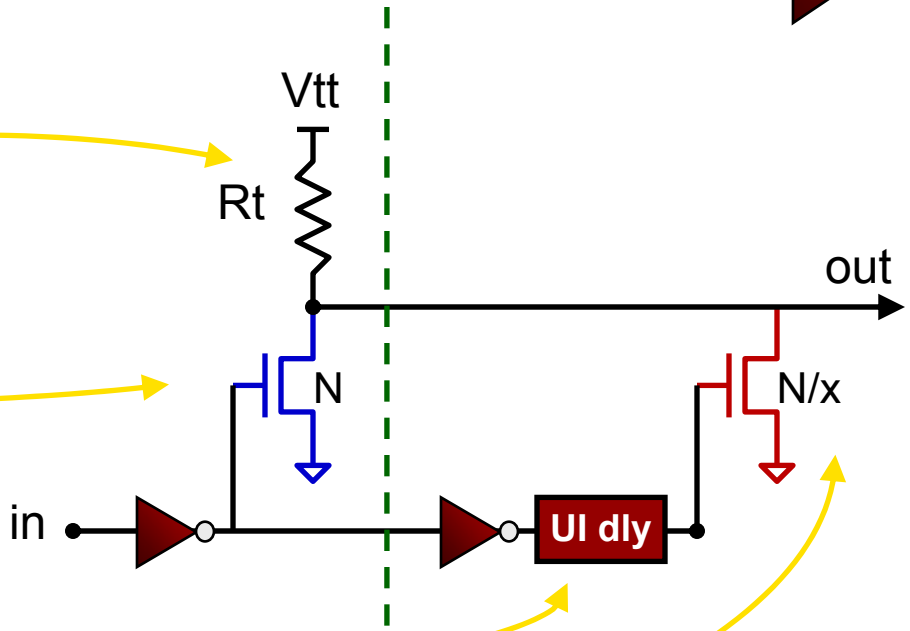


To Build MacroModel, Collect:

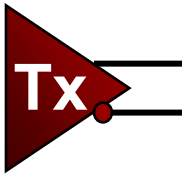


- Normal IBIS data
  - Vtt
  - Rt
  - Pulldown VI Curve
  - Ramp rate
  - C_comp
- Additional data
  - Unit interval
  - Pre-emphasis dB, or
    - Scale factor (x)
  - If correlating, get a waveform of your silicon model into a known load



Get the MacroModel templates from www.specctraquest.com

Where to Place Data in Template



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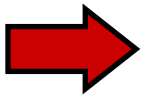
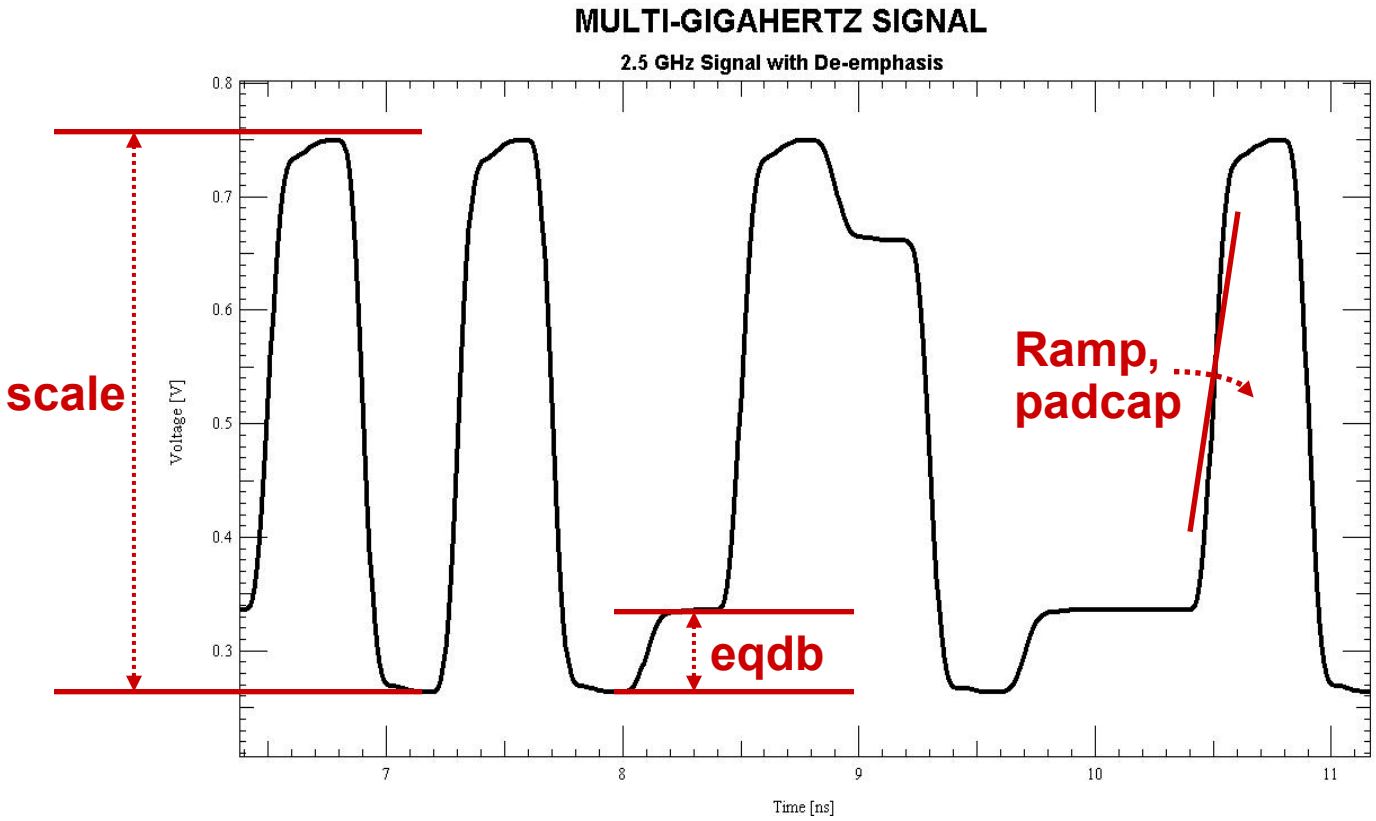


- Place in template
  - (Pullup (ReferenceVoltage
  - rt
  - (Pulldown (VICurve
  - (Ramp (dt
  - (C_comp and/or padcap
  - bitp
  - eqdb
    - cf1

If you get all this right, your model will be "close"

Adjusting Behavior (or, Correlation)



If you want to change:

- Voltage swing amplitude
- Pre-emphasis
- Edge speed

Adjust:

- scale
- eqdb
- Ramp, padcap

Relating Specs* to Model Parameters

4.3.3. Differential Transmitter (TX) Output Specifications

The following table defines the specification of parameters for the differential output at all Transmitters (TXs). The parameters are specified at the component pins.

Table 4-5: Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak to Peak Output Voltage	0.800		1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes 2 and 5.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential Mode Low impedance
$Z_{TX\text{-}DC}$	Transmitter DC Impedance	40			Ω	Required TX D+ as well as D- DC impedance during all states

*Specs courtesy of PCI Express™ Base Specification 1.0a pages 211 & 212

Model Parameter:

bitp

scale

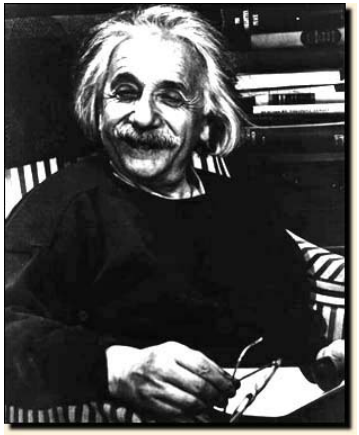
eqdb

Ramp dt, padcap

rt

rt

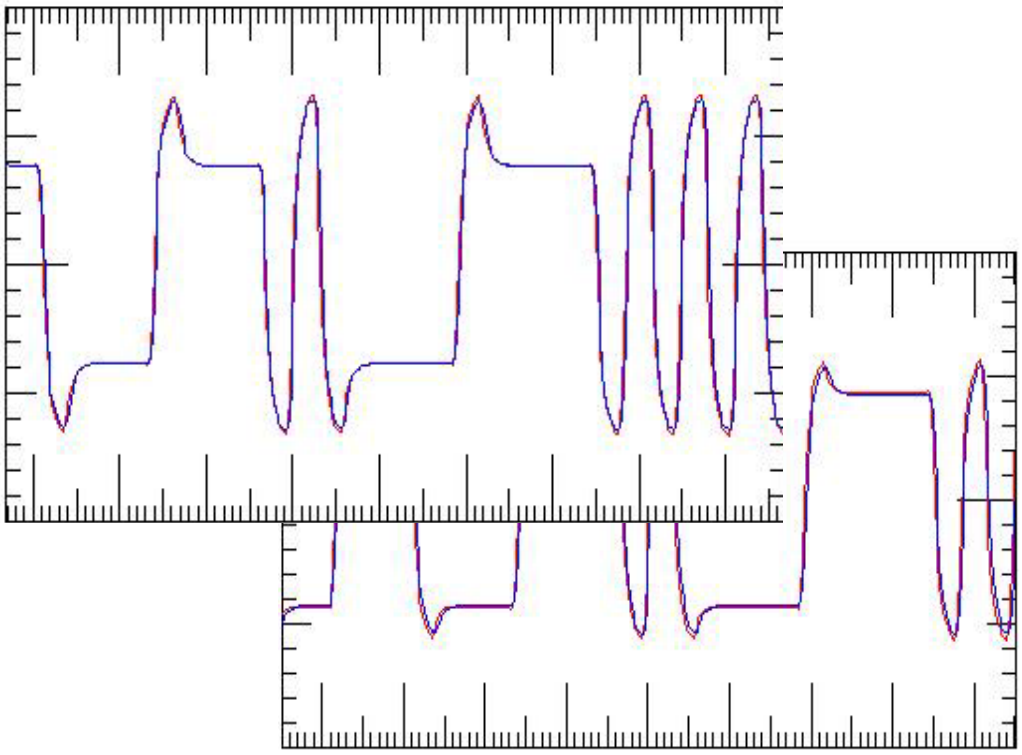
Technical Notes



- Use [Ramp] data instead of VT curves
  - Works fine for these CML (non-push/pull) drivers
  - Eliminates charge storage and over-clocking issues
  - Much simpler to adjust and correlate
- Some Tx designs exhibit miller capacitance effects
  - May cause slight miscorrelation when pulldown is on
  - See “Data Dependent Buffer Characteristics” Arpad Muranyi
    - http://www.eda.org/pub/ibis/summits/jan03/muranyi.pdf
  - May offer template for this, if necessary
- Visit “Modeling” discussion group at www.pcbhighspeed.com

Early User Feedback & Correlation

"Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab."



Correlation: MacroModel vs TransistorModel

"Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design."

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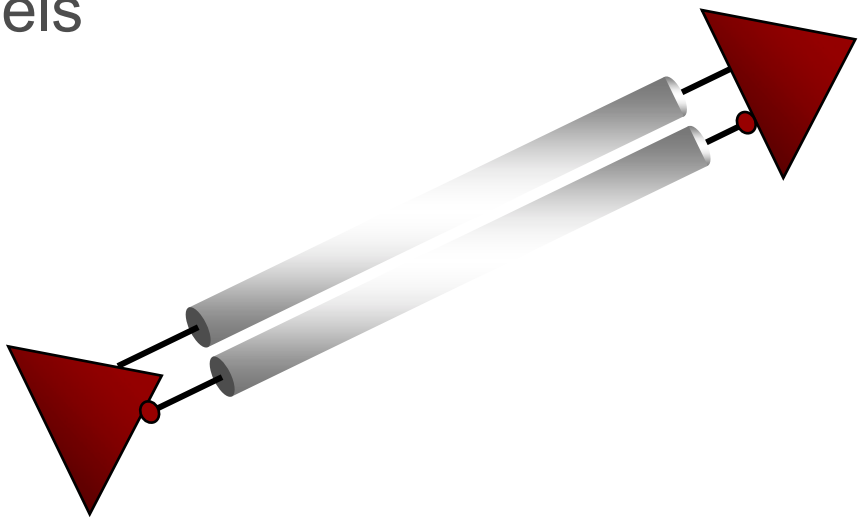

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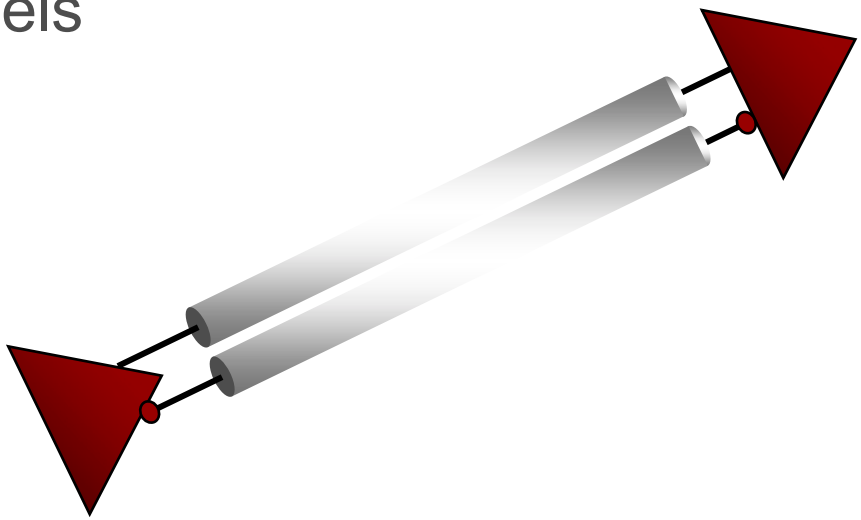

Summary

- It is important to simulate MGH serial links
- Link simulations should be done with long bit patterns
- Long simulations require fast models
- SQ MacroModels are fast, and templates are available
- The steps to build your MacroModel have been outlined here


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