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## New Serial Link Simulation Process, 6 Gbps SAS Case Study

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## **Abstract**

This case study details a pre-hardware serial link simulation process developed for 6+ Gbps link designs. Industry standards such as Serial-Attached SCSI (SAS) now require simulation to verify compliance since recovered link signals are only visible after equalization deep inside silicon. First-generation AMI models are used to simulate this equalization and quantify performance at 1e15 bits while comprehending a variety of jitter sources. Techniques for specification compliance testing are illustrated, some of which previously could only be performed with physical hardware. Design margins are quantified against a range of system configurations including PCB trace length, connector, and cabling options.

## **Authors Biographies**

**Donald Telian** is an independent Signal Integrity Consultant. Building on 25 years of SI experience his recent focus has been on new simulation techniques for Multi-GHz serial links. Donald is known as the SI designer of the PCI bus and the originator of IBIS modeling. He has taught SI techniques to thousands of engineers in more than 15 countries.

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**Kent Dramstad** is an ASIC Application Engineer at IBM. He has over 27 years of experience working on both power and signal integrity issues for a wide variety of applications. His current emphasis is on helping customers select and integrate IBM's series of High Speed Serdes (HSS) cores into their ASIC designs.

**Adge Hawes** is a Development Architect for IBM at its Hursley Labs, United Kingdom. He has worked for IBM for more than 30 years and currently develops simulators for High Speed Serial Links. He has represented the company in standards bodies such as PCI, SSA, and Fibre Channel and has worked on the development of graphics displays, printing subsystems, and PCs.

## 1. Introduction

Over the past decade, Printed Circuit Board (PCB) signaling has made a steady migration to high-speed serial links for the reasons stated in [1]. To enable third-generation (6 to 10 Gbps) serial link design, technology providers have partnered to develop compatible simulation tools and model formats such as Algorithmic Modeling Interface (AMI) models [2, 7, 8]. This paper explores the viability of these technologies by applying IBM's first-generation of AMI models on future Hitachi Global Storage Technologies (Hitachi GST) 6.0 Gbps Serial Attached SCSI (SAS) disk drive designs.

Coincident with the emergence of these new simulation technologies has been new industry-wide standards that require them [3]. While first- and second-generation serial links have leaned heavily on physical measurement tools to verify compliance, this is not possible for certain aspects of third-generation links. Relevant signals can no longer be probed externally due to the integration of extensive signal recovery and processing inside Integrated Circuits (ICs). As a result, the signal's true performance can only be probed virtually using simulation tools. Signal integrity has moved inside the ICs [4].

This paper illustrates how to apply the new technologies both to verify compliance to industry standards (e.g., the new 6.0 Gbps SAS specification [3]) and also to determine design margin in a range of system designs. A range of system simulations are included because SAS (and other specifications) verify Transmit and Receive (Tx and Rx) compliance in isolation by connecting them to generic reference loads, as will be explained. The processes and solutions described will likely be useful for similar third-generation serial link design projects.

## 2. Hard Disk Drive Simulation Scenarios

This section will describe how the Hard Disk Drive (HDD) system interface was modeled and simulated. Figure 1 offers a simplified view of the HDD model.

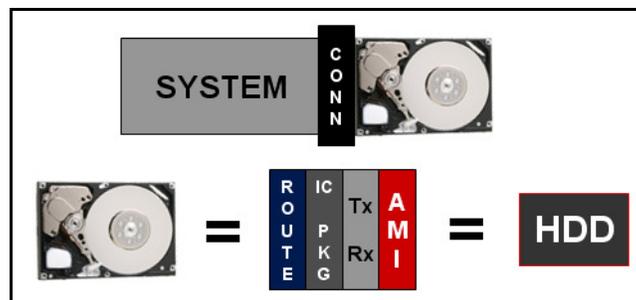


Figure 1: Simplified View of Hard Drive Model

As shown in the upper part of Figure 1, the HDD model is connected to the system through a connector model. The connector is an 8-port S-parameter model that captures the coupling internal to each port. Each SAS HDD has two ports, each with its own differential Tx and Rx. Two different 8-port connector models were used since mechanically, and hence electrically, the port connections are quite different.

The lower part of Figure 1 shows a breakdown of the HDD model, which includes the PCB route, IC package, analog Tx/Rx models, and the AMI models. Coupled, lossy, frequency-

dependent models for the HDD PCB route are used. Within each Rx pair series capacitors are included to couple the high-frequency signal and block DC current. The IC package model consists of two sets of S-parameter models; one to represent the wire-bond package and the other for on-chip routing. Next, the analog portion of the IBM SerDes Tx and Rx is modeled including such elements as die capacitance, terminations, and switching sources for the Tx. The IBM AMI model is the final element required to correctly model the equalization inside the HDD SerDes.

Since IBM was instrumental in the development of the AMI modeling standard, the SerDes models are among the first AMI models available in the industry. These models contain complex signal processing routines that are compiled into separate executables (DLL files) called by the simulation tools.

One of the unique features of AMI models is their equalization behaviors (both Tx FFE and Rx DFE) can not be seen when running normal time domain simulation. Instead, the user must simulate the link using a technique called Channel Analysis (CA). CA first executes a “Characterization” of the channel and then calls the AMI DLL files to apply equalization to the channel. While running normal time domain simulation does produce waveforms, those waveforms are generated using only the analog portions of the Tx and Rx. This distinction is important to understand and keep in mind when working with AMI models.

Figure 2 shows the three test fixtures defined by the SAS Specification [3] to verify compliance of a device’s Tx behavior, Rx performance, and passive Port interconnect. Both the Tx and Rx are independently required to deliver good performance against reference SerDes and system loads, while the passive interconnect must comply with various S-parameter limits. Note that the relevant measurement point for the Tx and Rx tests is at the output of the Rx DFE, inside the IC.

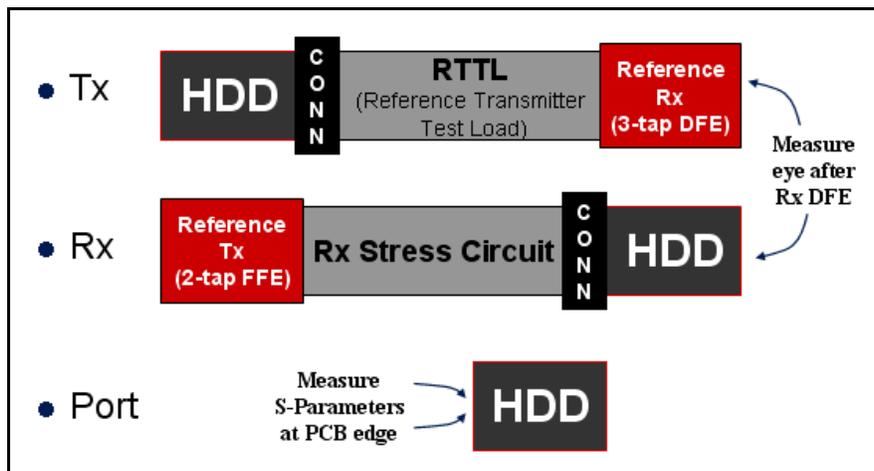


Figure 2: SAS Specification’s Compliance Test Fixtures

In addition to the compliance simulations shown above, design margin against the three system configuration scenarios shown Figure 3 is also quantified. The three system models present a variety of channel losses and discontinuities with overall lengths of 12”, 20”, and 36” as shown. Each scenario is described in more detail in the System Analysis section.

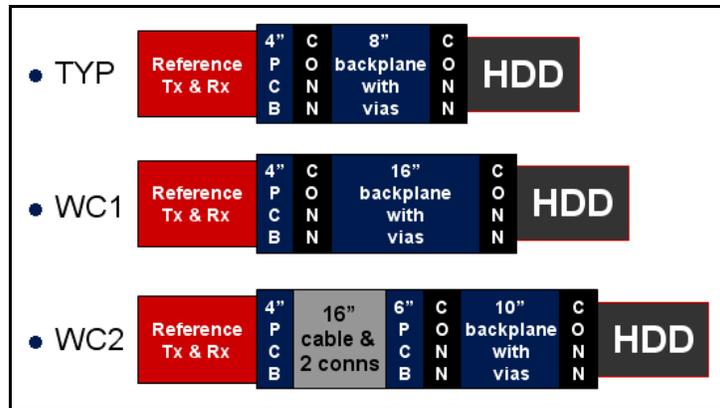


Figure 3: System Configuration Simulation Scenarios

### 3. Adherence to 6 Gbps SAS-2 Specification

To confirm Hitachi GST’s future 6 Gbps Hard Disk Drive (HDD) compliance to new SAS specifications the implementations are tested in three areas:

1. **Tx RTTL Testing** – requires the HDD Tx to adequately drive a 10-meter cable in such a way that a reference Rx can recover a valid signal
2. **Rx Stress Testing** – requires the HDD Rx to adequately recover a signal from a worst-case channel as driven by a reference Tx
3. **S-Parameter Limits** – requires the S-Parameters of both the HDD Tx and Rx portions of the channel stay below specified limits.

These analyses will be presented in the next three sub-sections.

#### 3.1 Tx RTTL Testing

SAS Specification Transmitter (Tx) testing is described in the spec’s Table 61 [3]. According to the Table’s note g in Figure 4 below, the specified way to confirm proper Tx signaling is to measure eye height and width at the *output* of a 3-tap reference Rx DFE – a node inside the IC that can only be probed by a simulator. This requirement is unprecedented, yet was necessitated by the fact that the anticipated signal at the *input* to the Rx device is typically not measurable; Tx equalization alone can not overcome anticipated 6 Gbps system loss.

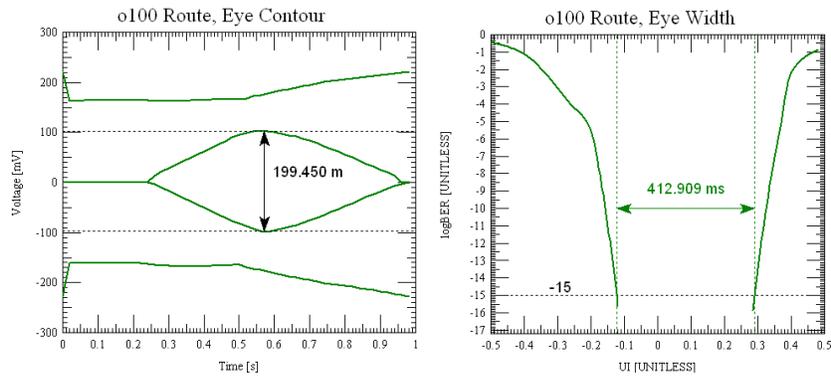
<sup>9</sup> This value is obtained by simulation. It represents the resulting signal output within the reference receiver device (see 5.3.7.4.3) after equalization, when the transmitter device output signal of CJTPAT is transmitted through the reference transmitter test load (see 5.3.2.5).

Figure 4: SAS Specification Note Requiring Simulation

As noted, the reference Rx DFE is to be connected at the other end of the “Reference Transmitter Test Load” (RTTL), described further below. The spec also recommends that reverse channel traffic be present in order to include the effects of crosstalk (see [3] section 5.3.5.3). Spec limits are 100mV eye height and 0.4 UI width at the 3-tap DFE’s output.

Implementing this test in simulation tools raises some considerations. The RTTL is physically a 10-meter cable captured in an S-Parameter model file. While using a long cable helped the spec





**Figure 6: CA Results from Tx Compliance Simulation**

Table 1 summarizes the simulated data and associated design margins.

Parameter	Value	Unit
Eye Height (1e6 bits)	199	mV
Eye Height Margin (100mV - 10%)	79	mV
Eye Width (1e15 bits, with Dj)	0.413	UI
Eye Width Margin (spec = 0.4UI)	0.013	UI
Eye Width Margin (target = 0.2UI)	0.213	UI

**Table 1: SAS Tx Compliance Design Margins**

The Table shows that the eye height has good margin, yet the width raises questions. As such, the eye width margin is calculated both to the spec limits and the HDD SerDes target. While performance to the spec limits seems marginal, we believe this is not a concern because:

1. The spec is heavily guard-banded. It suggests that simulation output to be judged at 1e15 instead of the 1e12 used for physical testing reasoning that “simulations typically do not include all aspects of noise that may degrade the signal quality” (see 5.3.3.3.3 in [3]). While this may be true, there are also many limits and inaccuracies associated with physical testing. Due to the slope of the bathtub curves, measuring performance at 1e12 recovers at least 3% more margin in all cases. We believe the simulations performed here are well-toleranced to worst-case and represent a more conservative analysis than is anticipated by the specification.
2. Comparing the spec’s width compared to the IBM SerDes device’s design target we find they differ by 100%. This suggests that the spec might be overly conservative. While we’re unclear on the origin and derivation of this value in the spec, we did note that it was one of the last values to be resolved and may still be up for revision. Note that the height spec is 1.7x the actual device’s target, while the width spec is 2.0x.
3. Good margin is realized to an actual device. While this device may be more robust than others, there appears to be margin to allow for various device characteristics.

In conclusion, simulation reveals that the Tx performs well when tested against the RTTL. The IBM Tx has more EQ capabilities that could improve the performance further, however standard settings were applied to confirm compliance in applications where firmware may not be able to adjust the settings on the fly.

### 3.2 Rx Stress Testing

The SAS Specification [3] outlines Rx compliance testing in “Section 5.3.7.4.4 Receiver device physical testing”. Note that this is specified as “physical testing”, meaning that it is meant to be performed on actual hardware rather than simulation. Indeed, prior to AMI models it was difficult to perform a system-level analog simulation and probe within the IC behind the Rx DFE. However, using IBM’s AMI models we can use simulation to get very close to the desired physical testing.

Table 2 describes most of the parameters for Rx stress testing specified by the SAS standard.

Characteristic	Units	Minimum	Typical	Maximum	Reference
Tx data pattern		CJTPAT			Annex A
Tx peak to peak voltage	mV(P-P)			800	5.3.6.5.1
Tx minimum rise/fall time	UI	0.24 (41.6 ps)			5.3.6.5.1
Transmitter equalization	dB			2	5.3.6.5.5
Tx RJ	UI	0.15 (25 ps)			5.3.6.5.1
Tx bounded uncorrelated jitter	UI	0.000 22 (0.036 ps)			
Link dispersion penalty <sup>a b</sup>	dB	13			5.3.7.4.4.8
D24.3 delivered eye opening (Z1) <sup>b</sup>	mV	75		95	5.3.5.4
D24.3 delivered eye opening (X1) <sup>b</sup>	UI	0.15			5.3.5.4
NEXT offset frequency <sup>b</sup>	ppm	20			
Total crosstalk amplitude <sup>b c</sup>	mV <sub>rms</sub>	4			

**Table 2: Stressed Receiver Test Characteristics from SAS Specification**

Per the upper portion of the Table, the Tx characteristics can be configured in the simulation to use a Compliance Jitter Pattern (CJTPAT) driven by a SAS Reference Tx with an 800mV swing, -2dB de-emphasis, and 42pS edge rates. This allows us to precisely implement the Tx behaviors in the first four rows of Table 2 in the simulation.

The spec then calls for an Rj of 0.15 UI (Tx RJ in Table) that it earlier defines as 17x the 1-sigma value for a simulated BER of 1e15. As such, the correct value to use in a simulator is (0.15/17=) 0.88% UI (0.0088 UI). The spec also calls out an additional 0.10 UI of sinusoidal jitter in a later section/Table. These jitter components must be included in the simulations.

To implement the rest of the necessary items for Rx stress testing we need to develop a system-level simulation testbench with the specified behaviors. Utilizing the knowledge and measurements obtained in the “System Analysis” section of this paper, we note that the desired behaviors of the Rx stress testbench lie between WC1 and WC2. As such, the topology shown in Figure 7 was built and tuned until it delivered the specified characteristics. Note that, according to Table 2, the characteristics need to be delivered to the compliance testpoints “IR” or “CR”. In our case this is the HDD side of the SAS connector. As such, the SAS connector is included in the testbench circuit, and probes are placed at the connector to measure the signal delivered to IR/CR as shown at right.

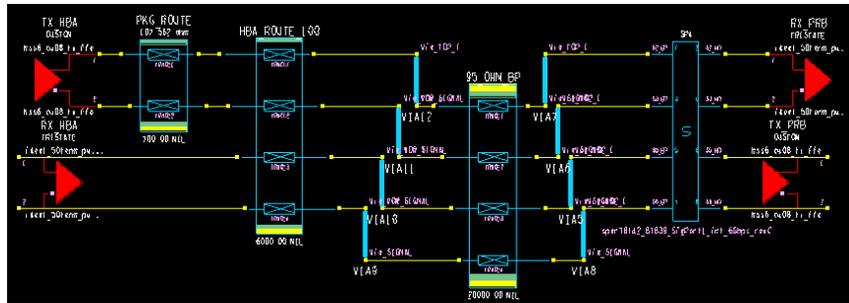


Figure 7: Testbench Circuit for Rx Compliance Stress Testing

From left to right, the Rx\_Stress circuit includes:

1. SAS Reference SerDes
2. Extra package-level routing on the SAS Tx to tune the edge rate and displace the crosstalk
3. Six inches of ~100 Ohm microstrip routing to allow the magnitude of pair-to-pair crosstalk to be tuned
4. Backplane-type vias for both extra loss, ISI, and discontinuities
5. Twenty inches of ~100 Ohm stripline routing, primarily for loss tuning
6. Another set of backplane vias
7. The PORT1 SAS Connector model, for worst-case crosstalk
8. Probes to measure the signal delivered to IR/CR

The plots in Figure 8 demonstrate that the Rx\_Stress topology shown above correctly implements the specified values in the Table 2. At left, we see that the system loss delivers the desired minimum value of 150 mV eye height at IR/CR when driven by the 800mV Tx swing. At right, we see that the eye width at IR/CR is reduced to ~0.30 UI as specified at 1e15 bits. The physical testing desired is specified at 1e12, but the spec derates this in other places to 1e15 for simulation. Note that at this point, no Rx device has been connected and hence DFE has not yet been applied.

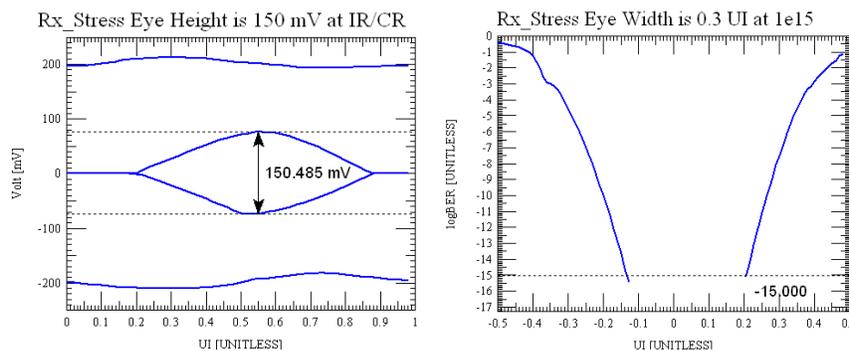
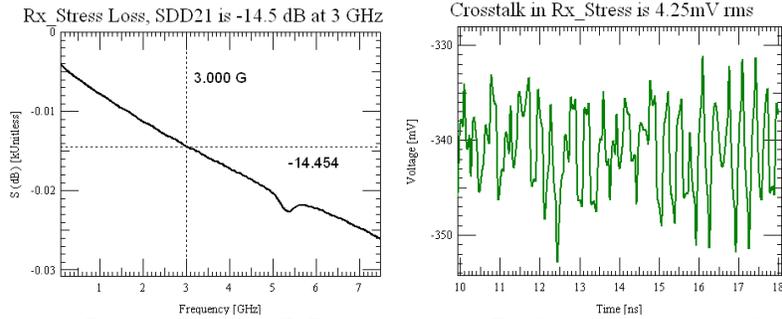


Figure 8: Performance of Rx Compliance Stress Circuit as Measured by CA

Implementing the loss has two components: ISI and SDD21. For ISI, Table 2 calls out a 13 dB “loss dispersion penalty (LDP)”. Unfortunately, at the time of this writing and analysis, the spec fails to describe how this is to be calculated and the document it points to is no longer available. Since contacting the spec owners/authors also failed to produce any definition, various

discontinuities were added to the Rx\_Stress topology to introduce additional ISI. For SDD21 loss, the specification recommends ~15 dB similar to the RTTL. From the desired voltage swing values of Tx=800mV and Rx=150mV we can derive the necessary loss to be 14.5 dB, and implement it by tuning the channel length as shown in the SDD21 plot at left in Figure 9. At right, we see that the models and diff-pair spacing were chosen to provide 4.25 mV rms of crosstalk, slightly above the spec's minimum of 4 mV in Table 2.



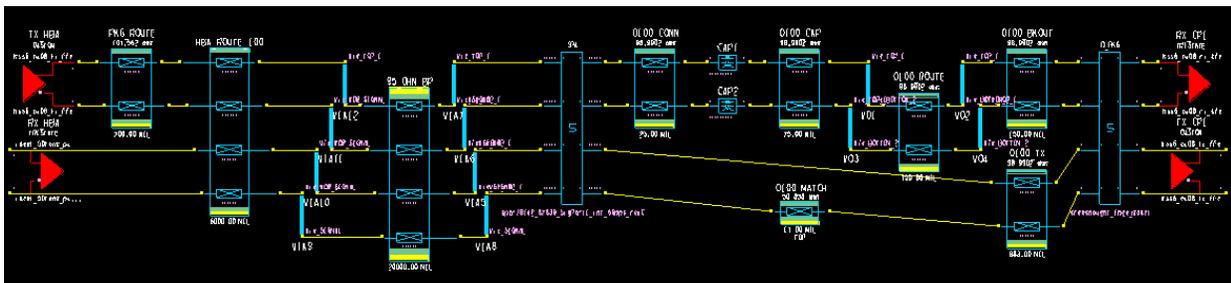
**Figure 9: Loss and Crosstalk Performance of Rx Compliance Stress Circuit**

At this point, we've addressed all items in Table 2 except for the crosstalk pair's offset frequency. Since CA does not allow us to enter this directly, we can offset the pairs to displace the crosstalk to the center of the other channel's Unit Interval (UI) by introducing extra routing in the upper pair using the "PKG\_ROUTE" trace segment shown in Figure 7.

With the Rx\_Stress circuit properly configured, we are now able to compare the performance of various HDD implementation options in simulation by simply connecting them to the Rx\_Stress testbench circuit above. The following sections compare two HDD routing options: (1) 100 Ohm outer-layer routes, and (2) 85 Ohm inner-layer routes. For each scenario, one layer change on the Rx and one inch of routing is assumed.

**100 Ohm Outer-layer Route**

Connecting the HDD to the Rx\_Stress circuit we arrive at the link shown in Figure 10. The SAS Connector is the blue S-parameter box in the middle of the canvas.



**Figure 10: HDD Model Connected to Rx Compliance Stress Circuit**

In order to comprehend the contribution of the Rx DFE, at left in Figure 11 is a plot of a short time domain simulation measured at the input to the Rx that shows the eye completely collapsed. After the DFE is applied, the eye is recovered as shown at center to 108 mV at 1 million bits. Over more bits the eye width continues to shrink to 0.408 UI at 1e15 bits as shown at right.

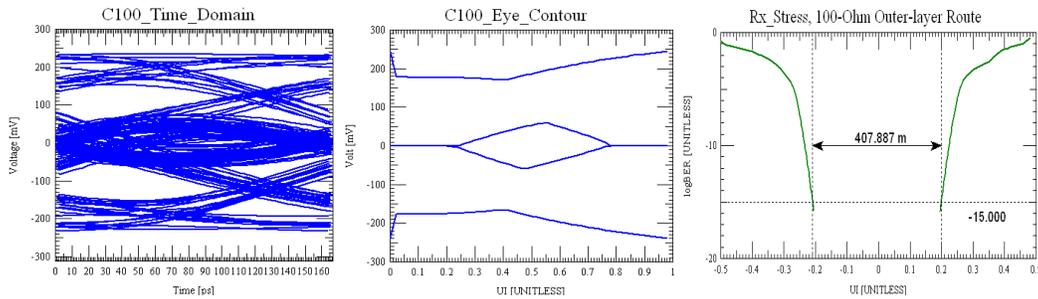


Figure 11: HDD Rx Compliance Plots, 100-Ohm Route

### 85-Ohm Inner-Layer Route

Testing an 85-Ohm inner layer route we see this route achieves still better performance of 131 mV eye height and 0.418 UI eye width at 1e15 bits as shown in Figure 12.

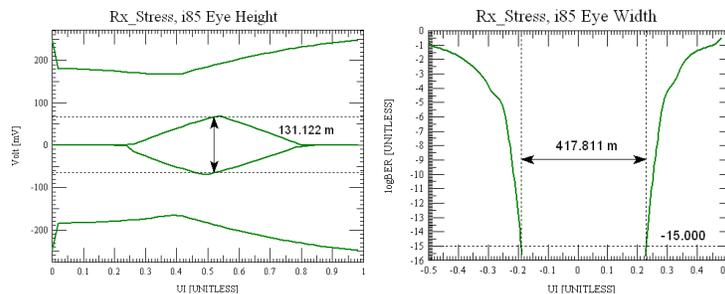


Figure 12: HDD Rx Compliance Plots, 85-Ohm Route

The following table summarizes the simulated performance of the two HDD route styles when connected to the Rx\_Stress testbench channel defined by the SAS spec.

Parameter	o100	i85	Unit
Eye Height (1e6 bits)	108	131	mV
Eye Height Margin (60mV - 10%)	37	58	mV
Eye Width (1e15 bits)	0.408	0.418	UI
Margin in UI (target = 0.2 UI min)	0.208	0.218	UI
Margin in pS	35	36	pS

Table 3: Simulated HDD Rx Compliance Margins

Since the tool does not report the eye height at 1e15 bits the margin calculation subtracts an additional 10% of the measured height. This value is derived from and is consistent with the amount the eye width changes between 1e6 and 1e15 bits.

There is good margin on both configurations, which illustrates both the power of the IBM DFE and the robustness of its design targets of 60mV/0.20UI. Note that if the simulations were measured against the SAS specification's 100mV/0.40UI values all measurements would be marginal, as with the Tx RTTL test. Though both implementations performed acceptably, it's interesting to note that the inner-layer 85-Ohm route performed measurably better.

This section has demonstrated that AMI models can be used to perform pre-hardware testing the authors of the SAS Specification outlined for post-hardware physical measurement.

### 3.3 S-Parameter Limits

The SAS Specification defines magnitude limits for both the Tx and Rx portions of the HDD as shown below. Since in this version of the spec [3] the values for the Tx (spec Table 63) are the same as the Rx values (spec Table 70), the Rx Table is not repeated here.

Characteristic <sup>a</sup>	Reference	L (dBmV)	N <sup>b</sup> (dBmV)	H (dB)	S (dBmV/decade)	f <sub>min</sub> (MHz)	f <sub>max</sub> (GHz)
S <sub>CC22</sub>	Figure 125	-6.0	-5.0	0	13.3	100	6.0
S <sub>DD22</sub>	Figure 125	-10	-7.9	0	13.3	100	6.0
S <sub>CD22</sub>	Figure 126	-26	-12.7	-10	13.3	100	6.0

Figure 13: S-Parameter Limits Defined by SAS Specification

S-Parameters were generated using the simulator for both the Tx and Rx port models. Note that it is also possible to perform these tests on physical hardware using a VNA.

For simulated S-Parameter generation, diff-pairs can be drawn as shown in Figure 14 for a typical Tx port (left) and Rx port (right). Per the spec, the S-Parameters are measured at the HDD card-edge without the SAS connector in place (the spec refers to this point as ITs/CTs and IRs/CRs).

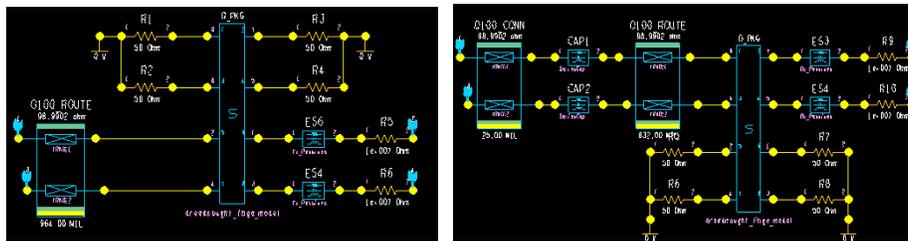


Figure 14: HDD Implementation Configured for S-Parameter Measurement

The plots for each port's passive interconnect are shown in Figure 15. In each plot the Specification's limit line is shown in red along with the simulated S-Parameters. In all cases simulated values are below the spec limit lines, as required.

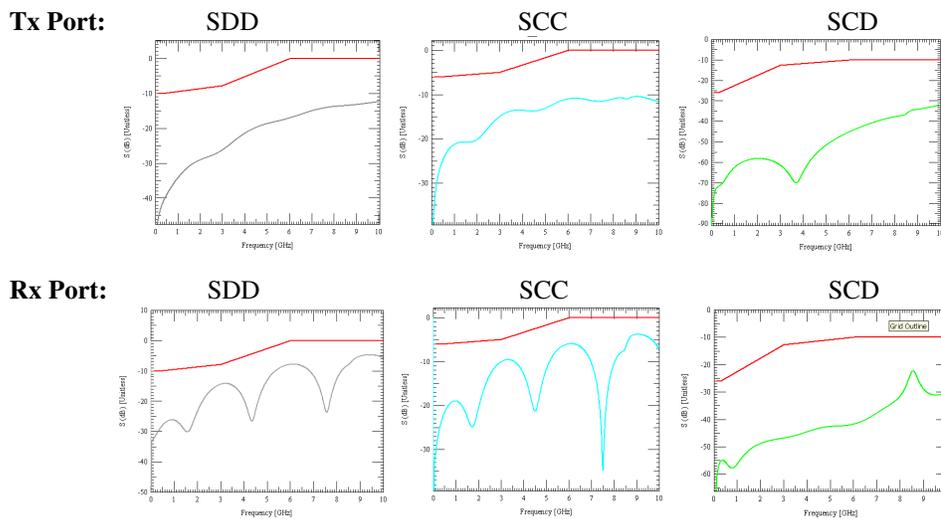


Figure 15: Compliance of HDD Passive Interconnect S-Parameters to SAS Limits

## 4. System Analysis

In this section the signal integrity performance of the HDDs is analyzed in various typical and worst-case system configurations. While adherence to the spec – as addressed in the previous section - is obviously important, analysis of additional system models is deemed necessary for the following reasons:

- 1) It is difficult for any Specification to adequately ensure performance
- 2) Specification adherence does not provide a sense of anticipated margin in actual systems
- 3) Aspects of the SAS-2 Specification target physical, rather than virtual device testing
- 4) SAS system configurations vary greatly compared to other interfaces such as Fibre Channel
- 5) Examining a range of system configurations helps develop an intuitive sense of configuration limits given the technology and data rates at hand

Taken alone, examining only system configurations or specification compliance would likely be insufficient. We believe the combination of both methods provides a more robust sense of system performance. As such, this section examines the behavior and details performance of the following system configurations whose composition is summarized in Table 4.

- a) TYP – Typical System Configuration, based on the author’s experience
- b) WC1 – Worst-Case System One, worst-case seen by the authors in practice
- c) WC2 – Worst-Case System Two, attempted retrofit into very bad legacy system

Parameter	TYP	WC1	WC2	Unit
PCB & Cable Length	13	21	37	inches
# of Connectors	2	2	4	#
# of Vias	4	4	4	vias
Propagation Time	2.5	4	6	nS
6 Gbps bits in channel	15	24	36	bits
Channel Loss (SDD21 @ 3 GHz)	-8.9	-13.6	-16	dB

**Table 4: System Simulation Configurations, Basic Metrics**

As shown, these systems represent a wide range in discontinuities, loss, and length and are configured to provide both a measured and an intuitive sense of how much margin is available in various system configurations.

For the analyses in this section, emphasis is placed on the IBM SerDes’ Rx DFE’s ability to recover a valid signal given each system configuration. As such, the channels are driven by a minimal SAS Reference Tx (2 taps with -2 dB de-emphasis and a minimum SAS voltage swing of 800 mV ppd). Since the eye shape will be probed at the output of the IBM DFE, all design margins derived in this section are based on IBM design targets. This method will give a good sense of received link performance with a minimal fixed tap Tx. It may also be interesting to drive the link with the HDD’s fixed Tx tap settings and check the margins against either a Reference Rx or another vendor’s Rx at the other end of the link, but that configuration is not addressed in this section.

### 4.1 System Analysis Process

Table 5 defines a serial link analysis process that will be applied to each system configuration, and each process step is described briefly below.

Step	Task	Purpose	Output
1	Collect and Connect Models	Build Link Model	Link Ready-to-Run
2	Model Sanity Check	Verify Models	TD Functional
3	Quantify Loss & Crosstalk	Understand & Gauge Link	S21 dB, mV RMS
4	Plot Impulse Response & ISP	Measure ISP, Calculate #bits	#bits for CA
5	Verify Eye Convergence	Test #bits, Confirm Coverage	CA Functional
6	Parameter Determination	Setup for Worst-Case	CA Parameters
7	Corner Case Analysis	Derive Design Margins	Eye h/w Margins

**Table 5: Serial Link System Analysis Process Steps**

- 1. Collect and Connect Models.** This step involves collecting and/or building all the necessary sub-models and connecting them to form the end-to-end link. Be sure all necessary vias, connectors, and series capacitors are included. Approximate trace construction parameters as needed. The output of this step is a link that is expected to simulate correctly in time domain simulation.
- 2. Model Sanity Check.** Begin by running a short time domain simulation. Watch for simulation errors, unreasonable voltages or DC shifts, and signals not reaching their destination. When there are problems during this step it is often necessary to temporarily delete elements from the simulation and add them back one at a time until the problematic element is isolated. S-parameter models are particularly suspect of causing problems. Ensure that the end-to-end time delay is reasonable and the voltages look correct. It's possible the eye will be completely closed at the Rx; this does not necessarily mean the simulation is incorrect, particularly at higher speeds. The output of this step is the ability to simulate in the time domain with confidence. Without achieving that, none of the subsequent steps can be performed.
- 3. Quantify Loss and Crosstalk.** Quantifying factors such as loss and crosstalk can help double-confirm the link simulation is performing correctly since there is a direct correlation between insertion loss (an Rx/Tx transfer function) and Tx and Rx voltages. Measuring S21 insertion loss is typically done in SI tools by generating S-Parameters. Take the value derived by the tool and double-check it against both the time domain voltages at the Tx and Rx and a hand calculation that sums the loss of each individual element. This will typically match within 10%. It's also important to gain an intuitive sense that can approximate performance across link metrics such as frequency, loss, and crosstalk. The outputs of this step include channel loss expressed in either dB or as a fraction. The latter reveals exactly what fraction of Tx voltage will appear at the Rx, while dB is less straightforward (though more common). A typical way to quantify crosstalk is to calculate the Root-Mean-Squared (RMS) value of the coupled signal on a quiet net. While most waveform tools do not calculate this number, it can be derived by exporting the waveform to a spreadsheet.
- 4. Plot Impulse/Pulse Response & ISP.** This is done by running a characterization of the channel (or, injecting a single pulse into the Tx and measuring the Rx) and viewing the impulse response waveform. The Interconnect Storage Potential (ISP) can be measured

directly from the impulse response as described in [5]. Furthermore, equations in [5] allow you to use the ISP to calculate the number of bits a high-capacity simulation will require to converge on a stable eye diagram. It is also important to verify the integrity of the characterization. As such the outputs from this step are a good channel characterization, the number of bits to apply in Channel Analysis (CA), and a sense of confidence that that quantity of bits will be sufficient for coverage. This saves time during subsequent simulations, since you are not running more bits than necessary.

5. **Verify Eye Convergence.** Channel Analysis simulation is run during this step, as various bit-stream lengths are overlaid to verify the eye converges correctly with the number of bits calculated in step 4. This value can be double-confirmed by comparing the number of bits derived with the knee on the bathtub curve plot. As such, the outputs of this step are a verified number of bits and a functional CA environment.
6. **Parameter Determination.** In order to derive meaningful CA results and design margins it's important to input correct parameters into CA for items such as jitter, bit patterns, and crosstalk. There are many components of jitter, and the industry does not always use consistent terminology. During this step you will determine the various sources of jitter imposed by the Tx such as random, deterministic, sinusoidal, and periodic jitter, as well as duty cycle distortion, and map them into the forms provided by your CA tool. Explore what types of data patterns are driven on the link (such as 8b/10b) or if there is a certain pattern (such as CJTPAT) that the link suggests to use. Much of this data is extracted from datasheets and other specifications. The outputs from this step are a complete set of Channel Analysis parameters necessary to derive worst-case eye diagrams and design margins.
7. **Corner Case Analysis.** This step runs CA to derive relevant eye diagrams and bathtub curves. From these, the necessary design margins are determined. If tolerances in the interconnect need to be tested, additional characterizations must be run. However, note that if tap values are variables in your AMI model they can typically be explored and adjusted without a new characterization. Compare the CA results derived during this step with link specifications. Insufficient margin may cause you to iterate all or parts of this process.

These steps will now be applied on each of the 6 Gbps system link configurations that follow.

## 4.2 TYP – Typical System Analysis

### Step 1: Collect & Connect Models

Models are collected for the various elements and the trace structures are built and connected to derive the drawing/shorthand description of the TYP channel shown in Figure 16.

Ctl Tx/Rx – 4" trace – Conn – BpVia – 8" trace – BpVia – Conn – 85Ohm 1" stripline & vias – Pkg – IBM Tx/Rx

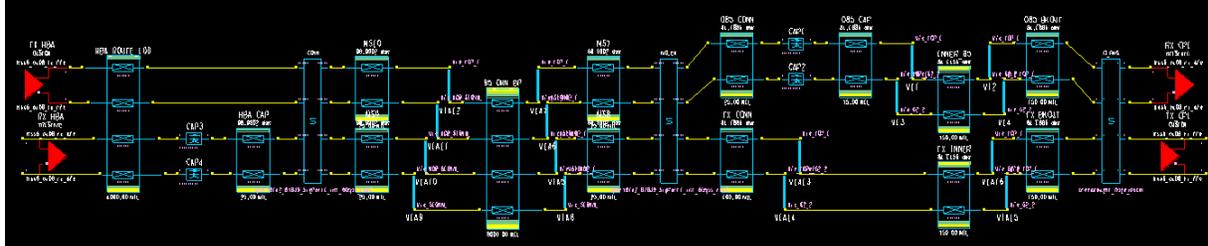


Figure 16: TYP Channel System Configuration

This channel has an overall length of 13” and spans 2 connectors. It includes 4” of route on the controller/expander at left and an 8” midplane route. The routing on the HDD is 85 Ohms and PORT1 connector models are used at both ends of the midplane. This channel represents a typical system configuration with typical loss. The upper channel is the active channel and the lower is the crosstalk channel.

**Step 2: Model Sanity Check**

For the TYP system a short time domain simulation reveals the eye at the Rx input (Figure 17, at left) is not completely collapsed without any DFE applied. Interestingly, the shape behind the inner eye has the basic shape of the Rx after the DFE is applied (at right). Applying Rx DFE with a 1 million bit CJTPAT shows the eye can be opened to 275mV height and 0.72UI width.

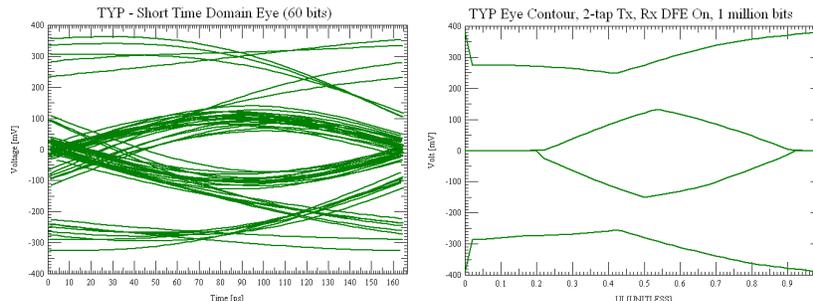


Figure 17: TYP Channel Initial Simulations

**Step3: Quantify Loss & Crosstalk**

Figure 18 (at left) plots the loss in the TYP Rx (topmost) channel. The loss is -8.9dB which is much less than the SAS spec’s RTTL at -15dB, as would be expected of a typical channel. Crosstalk induced in the quiet channel by the active channel appears as shown at right. The red waveform is the Rx pins, the green waveform after the die routing.

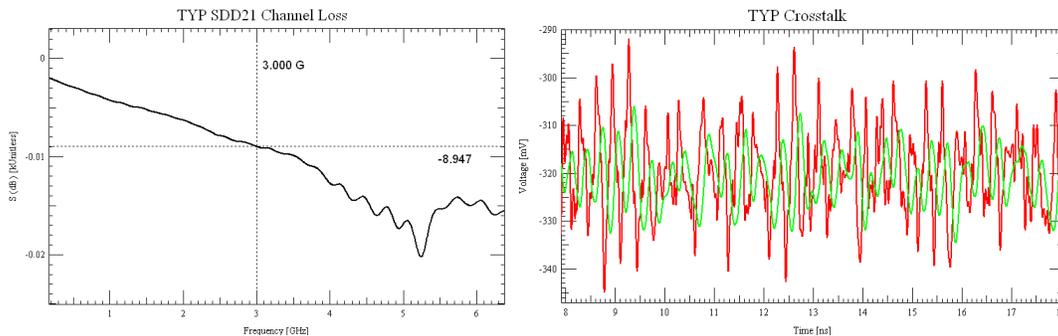


Figure 18: TYP Channel Loss and Crosstalk

The RMS voltage of the crosstalk for TYP can be calculated (by exporting the waveform’s spreadsheet data into Excel) to be 9.1mV rms. Interestingly this is higher than the value calculated for both WC channels, which could be due to any or all of the following reasons: more damping due to loss/discontinuities in WC, more crosstalk in the PORT1 model than PORT2, variations in round-trip time, or other reasons. Indeed, changing the connector model in WC1 from PORT2 to PORT1 raises the crosstalk from 5.6 mV rms to 7.9 mV rms. This agrees with plots that showed PORT1’s crosstalk to be ~30% higher than PORT2’s.

#### Step4: Plot Impulse Response & ISP

Figure 19 plots the impulse response in the active channel (left) and the crosstalk channel (right).

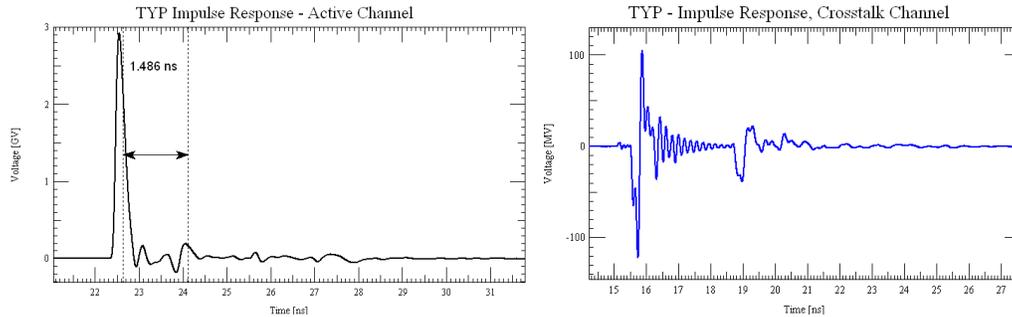


Figure 19: TYP Channel Impulse Response

The end-to-end propagation of TYP is  $\sim 2.5$  ns, hence the time offset of the near-end crosstalk (NEXT) and the  $\sim 5$  ns round-trip settle time in both plots.

The plot at left includes vertical markers measuring the Interconnect Storage Potential (ISP) to be 1.49 ns, or 9 (=ISP/UI=1.49/0.167, rounded up) bit times. This implies that each 8b/10b symbol's performance might be influenced by the prior symbol. Using equation (4) in reference [5] we find that for 8b/10b encoding we may need to run only  $\sim 10$  k bits to ensure adequate coverage. The low ISP suggests that this interconnect will converge quickly to a bounded eye.

#### Step 5: Verify Eye Convergence

Based on the ISP shown/calculated above, we expect the eye shape to converge quickly. Figure 20 confirms this since the TYP eye contours (produced using the 2-tap Tx driving CJTPAT) change slightly between 10k (red) and 100k bits (green), while the 1,000k (blue) bit pattern can barely be seen. Viewing the “bathtub” curve (at right) further illustrates that above 10k bits the eye width has converged and then continues to decrease linearly to 0.58UI at  $1e15$  bits.

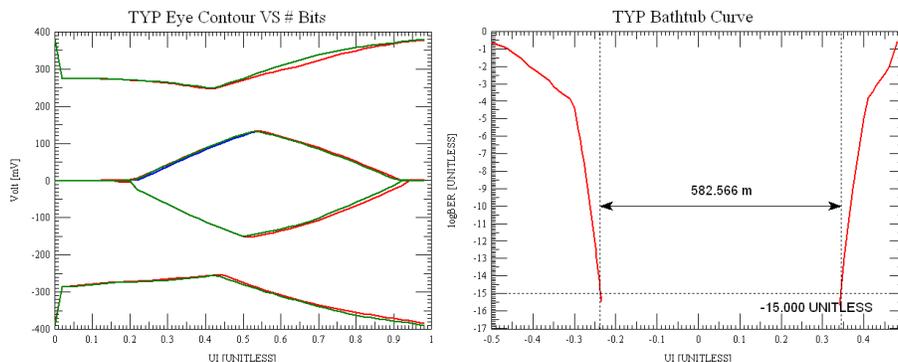


Figure 20: TYP Channel Eye Convergence

#### Step 6: Parameter Determination

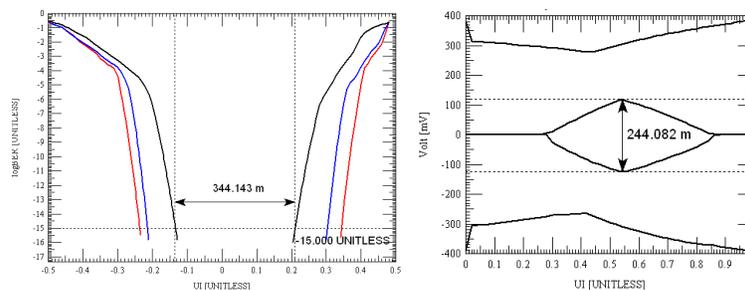
Corner case analysis can be performed by using worst-case values as defined by the IBM AMI, the IBM SerDes, and the SAS Specification. Table 6 summarizes these values and parameters. It should be noted that the process and values associated with tolerancing the simulations for worst-case are quite different than those used for more typical, lower-speed, SI analysis.

#	Variable	Influences	Source	Value	Unit	Apply In	Notes
1	Tx Swing	Eye shape	SAS Spec, Table 61	800	mV	Tx Model	minimum allowed
2	Tx De-emp	Eye shape	SAS Spec. Tables 64 65	-2	dB	Tx AMI	Ref Tx value
3	Bit Pattern	Jitter, Eye	SAS Spec, numerous	CJTPAT		CA	
4	Dj	Eye, Bathtub	Tx Parameter	23.4	pS p-p	chsim.clm	= 0.14% UI
5	Rotator Linearity	Eye, Bathtub	AMI Model Kit	pr_slow.dat	file	Rx model	pr_fast.dat a bit better edit into "just_ideal_corner"
6	On-chip Sparsams	Eye shape	AMI Model Kit	0		Tx/Rx models	
7	Rj	Eye, Bathtub	Tx Parameter	1.4	pS rms	CA	= 0.84% UI
8	Duty Cycle Dist.	Eye shape	Tx Parameter	0.05	UI	CA	Use 45 as HI%
9	Pj Magnitude	Jitter, Eye	AMI Model Kit	0.05	UI	CA	Enter as 0.05
10	Pj Cycles/UI	Jitter, Eye	AMI Model Kit	0.01	UI	CA	Enter as 0.01

**Table 6: Worst-Case Parameters, All Channels**

### Step 7: Corner Case Analysis

Simulating with all worst-case values except Dj in place further decreases the bathtub curve, as shown in Figure 21 in blue. Adding in Dj produces the worst-case eye width (black, at left) for TYP of 0.34UI at 1e15 bits, providing a good margin of 14% (24 pS) to the IBM design target of 0.20UI minimum. At right is the 1e6 eye height of 244mV. Following the same linear decrease as the eye width, we approximate that the eye height will decrease another 10% to 220mV at 1e15, leaving a good margin of 160mV to the 60mV design target.



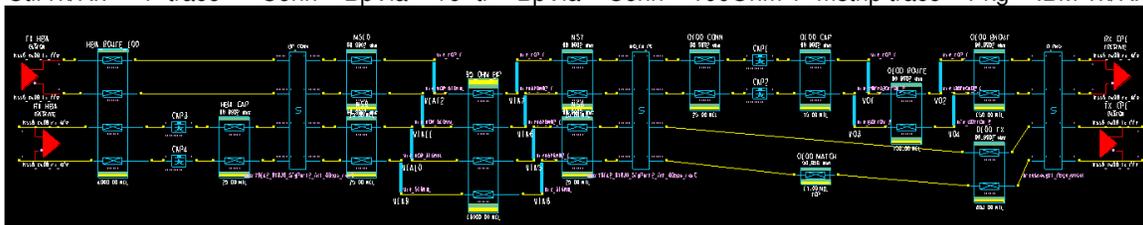
**Figure 21: TYP Channel, Eye Width and Height**

## 4.3 WC1 – Worst-Case System One Analysis

### Step 1: Collect & Connect Models

The layout drawing and shorthand description of WC1 is shown in Figure 22. This channel includes a much longer backplane trace than TYP and represents the worst-case system design anticipated for this family of HDDs.

CtrlTx/Rx – 4" trace – Conn – BpVvia – 16" tr – BpVvia – Conn – 100Ohm 1" mstrip trace – Pkg – IBM Tx/Rx



**Figure 22: WC1 Channel System Configuration**

### Step 2: Model Sanity Check

Leftmost in Figure 23 is a very short time domain simulation that shows how WC1 system loss shrinks the Tx waveform (red) substantially as it arrives at the Rx input (blue). Plotting the Rx waveform eye diagram (center) reveals that the eye is almost closed with only a few bits. However, recall that time domain simulation does not include equalization since that portion of the AMI models only appears in CA. Using CA, at right is an eye contour of 1 million bits (8b10b) with a -2dB 2-tap Tx and Rx DFE on. Based on this data, the channel appears to be performing reasonably and warrants further investigation.

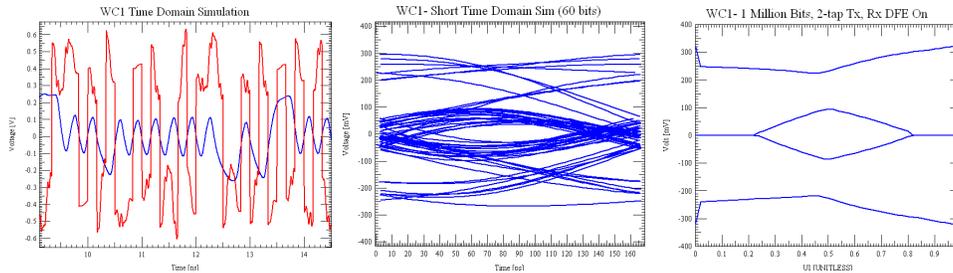


Figure 23: WC1 Channel Initial Simulations

### Step3: Quantify Loss & Crosstalk

At left in Figure 24 is a plot of the loss in the Rx (topmost) channel. The loss in WC1 is -13.6dB which is on par with the spec's stressed Rx LDP at -13dB and the RTTL at -15dB. This loss is a combination of all the elements in the worst-case model. To understand the system-level loss, at center is a plot of the loss in the two vias and at right is a plot of the connector loss.

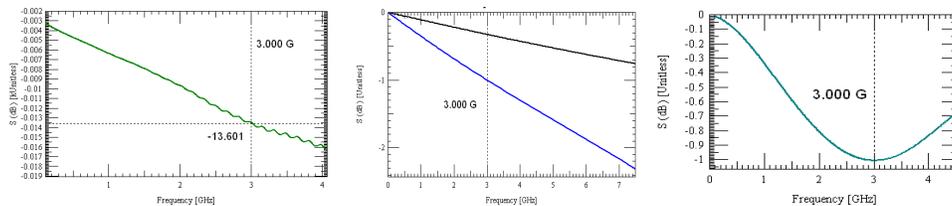


Figure 24: WC1 Channel Loss

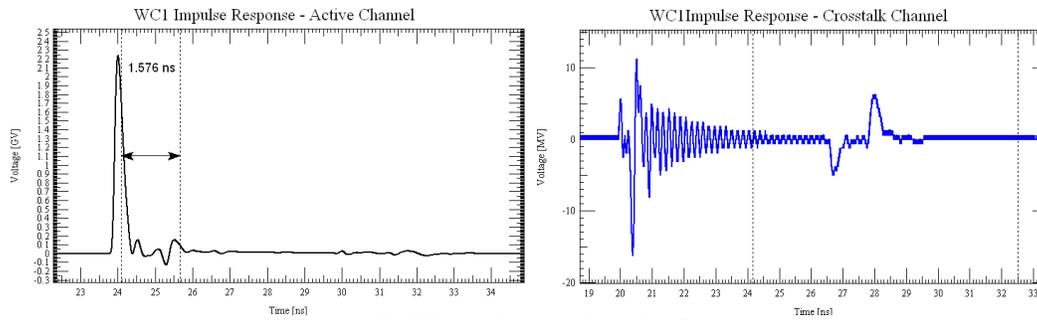
A simple summation of the individual elements shows good agreement with the end-to-end loss of -13.6dB measured above leaving 2 dB for the miscellaneous items not quantified here (capacitors, SerDes package, etc.).

$$\begin{aligned} \text{Total Loss} &= 2 * BpVia + 2 * CdVia + 2 * Conn + 21 * 0.33dB/inch + Misc \\ &= 2 * 1 + 2 * 0.3 + 2 * 1 + 21/3 + 2 = 13.6dB \end{aligned}$$

Crosstalk induced in the quiet channel by the active channel was simulated to be 5.6 mV rms. This value is 30% higher than the 4mV rms value recommended by the SAS-2 Specification for a stressed signal input to an Rx, and hence represents both a practical and challenging amount of crosstalk to submit to the high-capacity simulator and Rx DFE.

### Step4: Plot Impulse Response & ISP

Figure 25 shows the impulse response of the active channel at left and crosstalk channel at right.

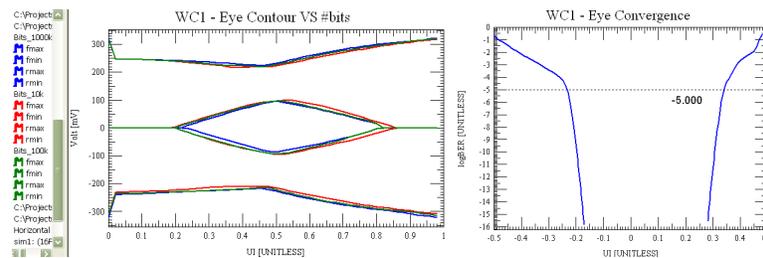


**Figure 25: WC1 Channel Impulse Response**

Both responses behave as desired, with matching stable/quiet voltages before and after the impulse (note that a ~20nS quiet/stabilization time was used). Since WC1's end-to-end propagation time is ~4ns we see the impulse at the active channel (left) around 24nS while near-end crosstalk can be seen in the quiet channel around 20nS (at right). And since the round-trip time in the channel is ~8nS, additional noise is seen in both plots ~8nS after the initial spikes. The plot at left includes vertical markers measuring the ISP to be 1.58 nS, or 10 (=ISP/UI=1.58/0.166, rounded up) bit times. This implies that each 8b/10b symbol's performance might be influenced by the prior symbol. The ISP is similar to that found with TYP since the discontinuities in the channels are similar; it is primarily the length that has changed. Using equation (4) in reference [5] we find that for 8b/10b encoding we may need to run only ~100k bits to ensure adequate coverage. The ISP suggests that this interconnect will converge to a bounded eye prior to 1e6 bits.

### Step 5: Verify Eye Convergence

Based on the ISP shown/calculated above, we expect the eye shape to continue to change as the number of bits increases up to ~100k bits. Figure 26 at left confirms this by showing the WC1 eye contours using 8b10b patterns of different lengths, 10k bits (red), 100k (green), and 1,000k (blue). The eye height/width continues to visibly decrease with the number of bits until it stabilizes around 1e6 bits, requiring an order of magnitude more bits than TYP as seen in the knee of the bathtub at right.



**Figure 26: WC1 Channel Eye Convergence**

### Step 6: Parameter Determination

The worst-case parameters for WC1 are the same as those for TYP. Refer to TYP step 6.

### Step 7: Corner Case Analysis

Applying all corner case values to WC1 (Figure 27, red) narrows the typical bathtub curve (in green) significantly to produce an eye width of 0.25 UI. This has 0.05 UI (9 pS) margin to the IBM design target of 0.20 UI, which is acceptable for this type of analysis. At right below is the

1e6 bit eye height (CJTPAT, Ref Tx) of 172mV which derates to 95 mV of margin at 1e15 given a 10% reduction and 60mV target. As such, WC1 has good margin against worst-case analysis.

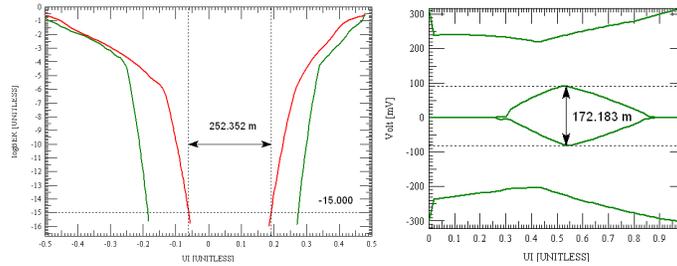


Figure 27: WC1 Channel Eye Width and Height

#### 4.4 WC2 – Worst-Case System Two Analysis

##### Step 1: Collect & Connect Models

A drawing/shorthand description of the WC2 channel is shown in Figure 28.

HBATx/Rx – 4” tr – 16” cbl – 6” ipsr - Cn – BpV – 10” tr – BpV – Cn – 1” HDD stripline trace – Pkg – IBM Tx/Rx

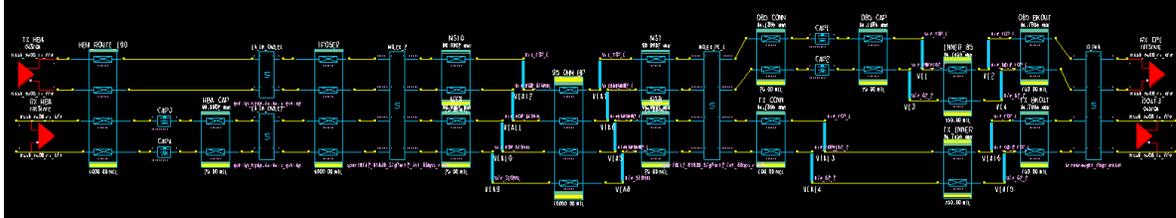


Figure 28: WC2 Channel System Configuration

This channel has an overall length of 37” and spans 4 connectors. It includes 16” of differential flat cable (model includes mated connectors on both ends), a 6” legacy interposer PCB, and a 10” backplane. The backplane, though shorter, is similar to the one in WC1. The interposer uses 7/7 (trace/space widths) for a differential impedance of 85 Ohms. This channel is contrived for lots of loss, many impedance changes/reflections, and is likely well beyond the worst system design the 6 Gbps HDD might be connected to in practice.

##### Step 2: Model Sanity Check

After confirming proper operation for the majority of the WC2 models during the previous two sections, confidence is high that they are operating correctly. As shown in Figure 29, for WC2 even a short time domain simulation reveals the eye at the Rx input is basically closed without any equalization applied. This channel represents a significant challenge for the Rx DFE.

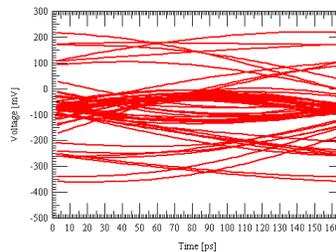


Figure 29: WC2 Channel Initial Simulation

### Step3: Quantify Loss & Crosstalk

Figure 30 (left) plots the loss in the WC2 Rx (topmost) channel as -16dB, significantly higher than the spec's stressed Rx LDP at -13dB and slightly more than the RTTL at -15dB. Crosstalk induced in the quiet channel by the active channel appears as shown at right. The red waveform is the Rx pins, green after the die routing (further damped). The RMS voltage of the crosstalk for WC2 was calculated to be 7.4mV rms.

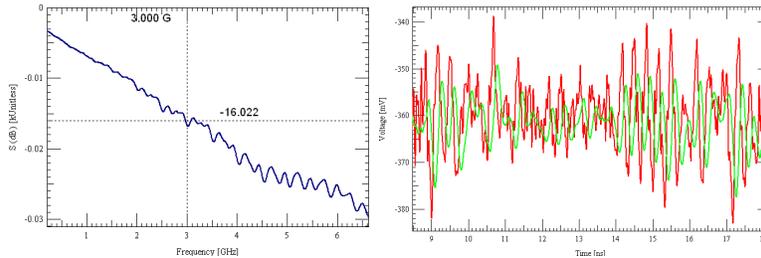


Figure 30: WC2 Channel Loss and Crosstalk

### Step4: Plot Impulse Response & ISP

Figure 31 shows the active channel (left) and crosstalk channel (right) impulse response.

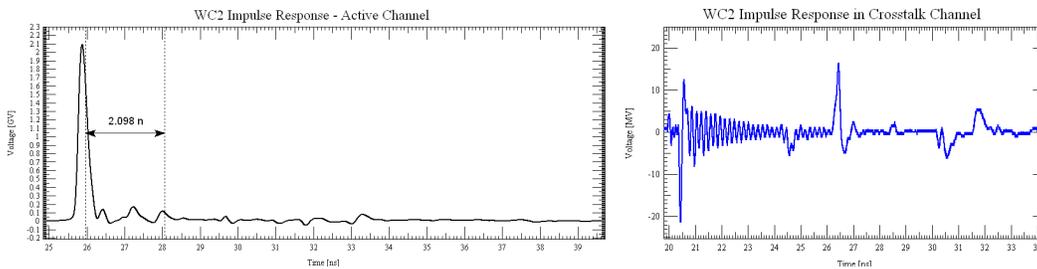


Figure 31: WC2 Channel Impulse Response

The end-to-end propagation of WC2 is ~6nS, hence the time offset of the NEXT and the 12nS round-trip settle time in both plots. The longer settle time suggests that a larger quiet time of 30nS should be used for WC2 during Characterization. The ISP of 2.1 nS (12 bits) is longer than WC1 and the overall ringing lasts longer likely due to more discontinuities. Equation (4) in [5] suggests that 100k bits would be necessary to bound eye opening behavior for this channel, similar to the other channels.

### Step 5: Verify Eye Convergence

Based on the ISP shown/calculated above, we expect the eye shape to continue to change as the number of bits increases. Figure 32 confirms this channel converges similar to the others.

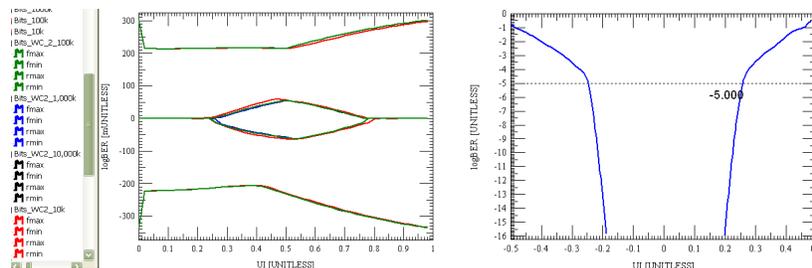


Figure 32: WC2 Channel Eye Convergence

### Step 6: Parameter Determination

The worst-case parameters for WC2 are the same as those for TYP. Refer to TYP step 6.

### Step 7: Corner Case Analysis

Applying corner case analysis decreases the eye a bit further as shown in Figure 33 in red. Adding in the  $D_j$  of 0.14UI narrows the eye further as shown in black to 0.22 UI for 1e15 bits. This reveals that WC2 has little margin to the design target of 0.20 UI minimum and represents a marginal system configuration.

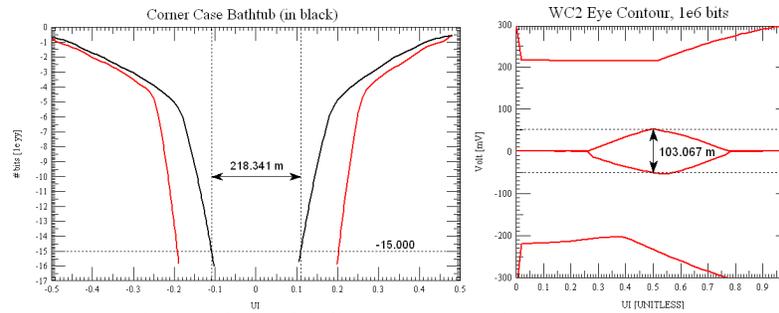


Figure 33: WC2 Channel Eye Width and Height

## 4.5 System Analysis Summary

To summarize our system analysis we have tested three system configurations: TYP, WC1, and WC2. These systems have been described previously, and can be characterized by the basic metrics repeated in Table 7 below. Though all three systems performed decently in a typical analysis using 1 million bits, corner case analysis shows design margin becomes minimal at 1e15 bits for WC2 as shown. To the IBM Rx DFE's credit, it was able to compensate for the loss and ISI in all channels showing positive margin in all cases. Clearly the boundary of acceptable system configuration lies somewhere near WC2. Sound engineering judgment can determine the boundary as guided by the design process and tools, and proper hardware verification.

Parameter	TYP	WC1	WC2	Unit
PCB & Cable Length	13	21	37	inches
# of Connectors	2	2	4	#
# of Vias	4	4	4	vias
Propagation Time	2.5	4	6	nS
6 Gbps bits in channel	15	24	36	bits
Channel Loss (SDD21 @ 3 GHz)	-8.9	-13.6	-16	dB
Crosstalk	9.1	5.6	7.4	mV rms
ISP	1.5	1.6	2.1	nS
#bits for Coverage	1e4	1e5	1e5	bits
Corner Eye Height (1e6 bits)	244	172	103	mV
Eye Height Margin (60 mV -10%)	160	95	30	mV
Typ Eye Width (1e6 bits)	0.72	0.59	0.52	UI
Corner Case Width (1e15 bits)	0.344	0.252	0.218	UI
Margin in UI	0.144	0.052	<b>0.018</b>	UI
Margin in pS	24	9	<b>3</b>	pS

Table 7: Design Margins for Analyzed System Configurations

To further illustrate the system configuration design boundary, consider the plot of design margin versus channel length in Figure 34. Even though there are many factors involved besides length, we can extrapolate the lines in the plot to estimate where all margin might be consumed.

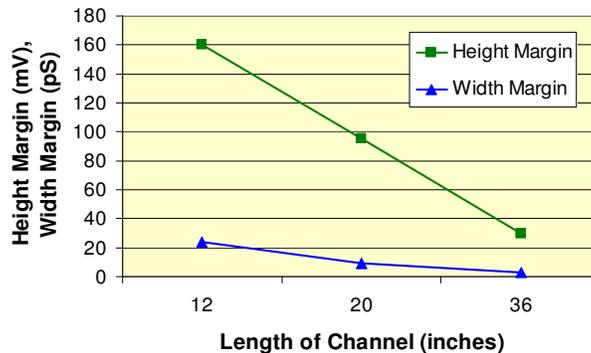


Figure 34: Design Margin vs. Channel Length

The data presented in this section suggests that the IBM Rx DFE in the HDD can compensate for a minimal fixed-tap Tx on the other end of the link, even in the presence of crosstalk. However, the boundary for robust system performance is close to the system configuration and loss of WC2. This correlates well with the SAS-2 Specification's view that Tx and Rx components must work together to overcome a channel loss of around -15dB.

## 5. Key Learnings and Conclusions

Throughout this case study we have determined the following items:

1. It is possible to construct a useful 6 Gbps SAS simulation environment using open market tools [6] and IBM SerDes AMI models. The performance of this environment appears to align well with both SerDes vendor and the SAS specification's expectations.
2. As shown through simulation, the HDD implementation and IBM SerDes performed well with good margin against both compliance tests and actual system loads.
3. More margin can be obtained by routing the Rx channels at 85 Ohm (instead of 100 Ohm) differential impedance. The Tx channels can be routed either way.
4. Even against worst-case tolerances, decent margin exists in applications around -14 dB (SDD21 @ 3 GHz) channel loss. Worst-case margins become questionable around -16 dB. Typical applications are likely less than -10dB.
5. The SAS Specification's physical Rx stress test environment can be implemented through simulation. In this setting, the HDD SerDes' DFE performed exceptionally well with margins in the 20% (or better) range.
6. Spec-level Tx testing also performed well. Although eye width measurements were marginal to the current spec, this is not believed to be an issue due to the reasons stated.
7. Spec-level passive S-Parameter limits were achieved for all ports, as verified through simulation.

In conclusion, we have seen that as serial link frequencies continue to increase so do system loss and IC integration complexity. These changes have required new types of models, tools and specifications, and even a new approach to signal integrity engineering in general. This paper has shown that AMI models are starting to appear and illustrated how they can be used in practice to perform both specification compliance testing and system design margin analysis.

## Acknowledgements

The authors wish to thank Cal Yoshikawa, Cliff Jeske, and Michael Flannery at Hitachi GST for their interest and support in pioneering new simulation methodologies as described here. Also Joe Ablner and Kevin Kramer at IBM for their support of advanced SerDes SI through advancing the AMI standard and model releases. Additional thanks to Hemant Shah, Ken Willis, Ambrish Varma, and Brad Griffin of Cadence for driving the timely and robust release of AMI capabilities in Allegro PCB SI. C. Kumar for his visionary effort behind the AMI solution, and Todd Westerhoff of SiSoft for helping to drive the standard across the industry. Without the efforts of these and others this work would not have been possible.

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[6] Cadence Allegro PCB SI GXL, version 16.01, 16.1 s006 (v16-1-53M) [1/24/2008] i86. Version 16.0 (or later) is required to run AMI models, this version of 16.01 (or later) is the first to remove requirements to run various IBM AMI features from a command-line. See: [http://www.cadence.com/products/pcb/pcb\\_si](http://www.cadence.com/products/pcb/pcb_si)

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