DesignCon® 2014

Moving Higher Data Rate Serial Links into Production – Issues & Solutions

ERICSSON

SI GUYS

SiSoft™

Session 8-FR1

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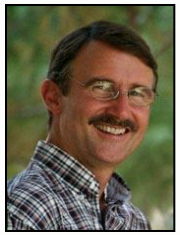
UBM Tech

About the Authors



Donald Telian is an independent Signal Integrity Consultant. Building on over 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-Gigabit serial links. He has published numerous works on this and other topics that are available at his website siguys.com. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries.

Sergio Camerlo is an Engineering Director with Ericsson Silicon Valley (ESV), which he joined through the Redback Networks acquisition. His responsibilities include the Chassis/Backplane infrastructure design, PCB Layout Design, System and Board Power Design, Signal and Power Integrity. He also serves on the company Patent Committee and is a member of the ESV Systems and Technologies HW Technical Council. In his previous assignment, Sergio was VP, Systems Engineering at MetaRAM, a local startup, where he dealt with die stacking and 3D integration of memory. Before, Sergio spent close to a decade at Cisco Systems, where he served in different management capacities. Sergio has been awarded fourteen U.S. Patents on signal and power distribution, interconnects and packaging.

Kusuma Matta has been working with Ericsson Inc. as a hardware engineer in the field of signal integrity engineering since 2007. Prior to Ericsson, she worked at LSI also in the field of signal integrity. Her research interests include signal integrity for SerDes and DDR interfaces, board and package level SI optimizations, and VNA and TDR measurements. Kusuma has M.S. in Electrical Engineering from University of South Carolina and B.S. in Electronics and Communications Engineering from JNTU (Jawaharlal Nehru Technological University), Kakinada, India.

Barry Katz, President and CTO for SiSoft, founded SiSoft in 1995. As CTO, Barry is responsible for leading the definition and development of SiSoft's products. He has devoted much of his efforts at SiSoft to delivering a comprehensive design methodology, software tools, and expert consulting to solve the problems faced by designers of leading edge high-speed systems. He was the founding chairman of the IBIS Quality committee. Barry received an MSEE degree from Carnegie Mellon and a BSEE degree from the University of Florida.

Dr. Walter Katz, Chief Scientist for SiSoft, is a pioneer in the development of constraint driven printed circuit board routers. He developed SciCards, the first commercially successful auto-router. Dr. Katz founded Layout Concepts and sold routers through Cadence, Zuken, Daisix, Intergraph and Accel. More than 20,000 copies of his tools have been used worldwide. Dr. Katz developed the first signal integrity tools for a 17 MHz 32-bit minicomputer in the seventies. In 1991, IBM used his software to design a 1 GHz computer. Dr. Katz holds a PhD from the University of Rochester, a BS from Polytechnic Institute of Brooklyn and has been awarded 5 U.S. Patents.

Michael Steinberger, Ph.D., Lead Architect for SiSoft, has over 30 years experience designing very high speed electronic circuits. Dr. Steinberger holds a Ph.D. from the University of Southern California and has been awarded 14 patents. He is currently responsible for the architecture of SiSoft's Quantum Channel Designer tool for high speed serial channel analysis. Before joining SiSoft, Dr. Steinberger led a group at Cray, Inc. performing SerDes design, high speed channel analysis, PCB design and custom RAM design.

Agenda

- Introduction
- Design Improvements
- Manufacturing
- Summary

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- Introduction
  - Background
  - Links: Generations & Features
- Design Improvements
- Manufacturing
- Summary

Background

- Very large scale system design
  - Over 7,000 sq in of PCB
  - Thousands of serial links
- Multi-year/generation project
  - Comprehends range of data rates
- Bringing key learnings every 2 years
- Virtual simulation bias/dev
  - Relentless measurement/correlation

Serial Link Generations & Features

(nice to have) (required)	1st Generation 1.5 Gbps	2nd Generation 3 Gbps	3rd Generation 6 Gbps	4th Generation 12 Gbps	5th Generation 24 Gbps
P/N Symmetry					
Tx Pre-emphasis					
Rx CTLE					
Rx DFE					
Via Design					
Via Back-drilling					
Antipad Etch Tapers					
Via Cage Symmetry					

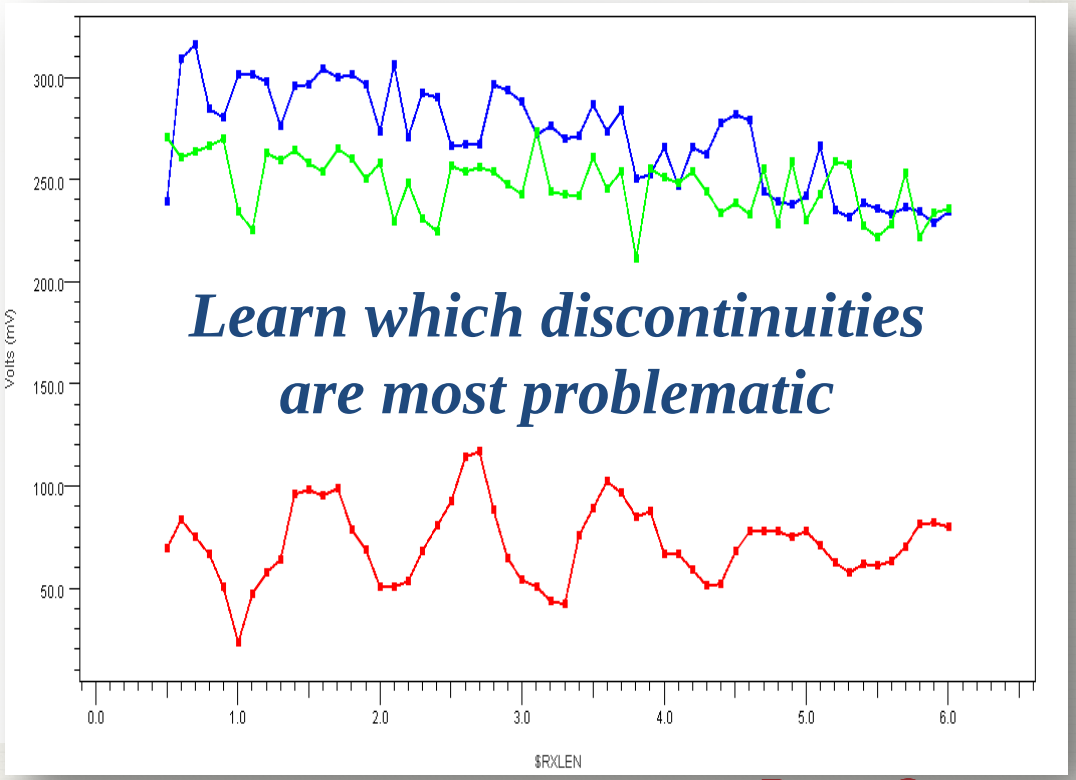
Each generation's improvements become the next generation's requirements

Agenda

- Introduction
- Design Improvements
  - Remove Discontinuities
  - Derive EQ Settings
  - Adjust Layout
- Manufacturing
- Summary

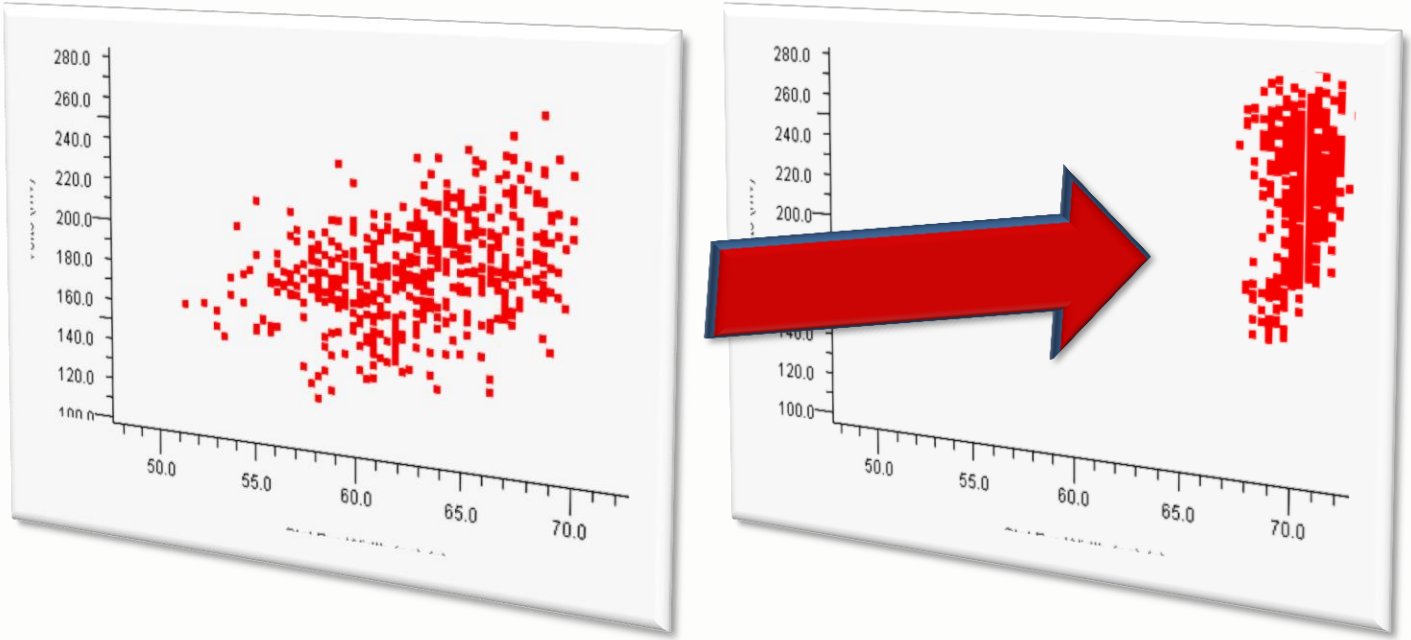
Design: Remove Discontinuities

- With present EQ worst channels often shortest
- Short channel eye height vs distance to via
  - Red is baseline
    - 100% variation
  - Green fixes 2 vias
    - ~400% gain
  - Blue fixes all discontinuities
    - Slight gains



Same Change, 100s of Links

- Eye height vs eye width, before & after



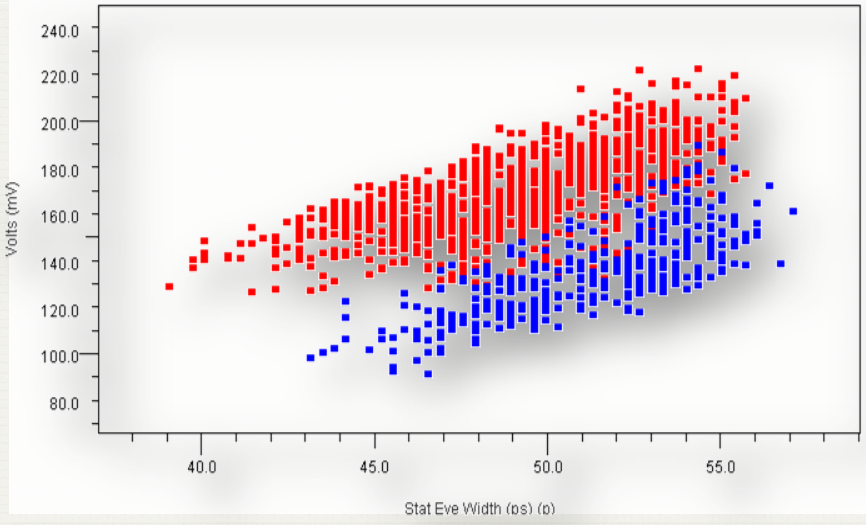
- Eye width variation stabilized – improved 4x

Only 1% of channel length was adjusted for this improvement

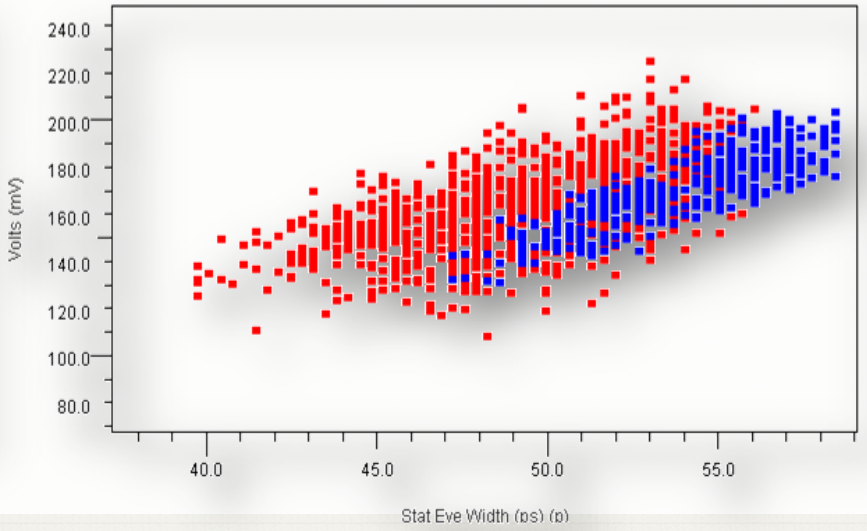
Design: Derive SerDes Settings

- Increasing number of EQ setting options
- “Default” settings typically not ideal
- 1000+ links, blue=long/amplitude_constrained

Default settings

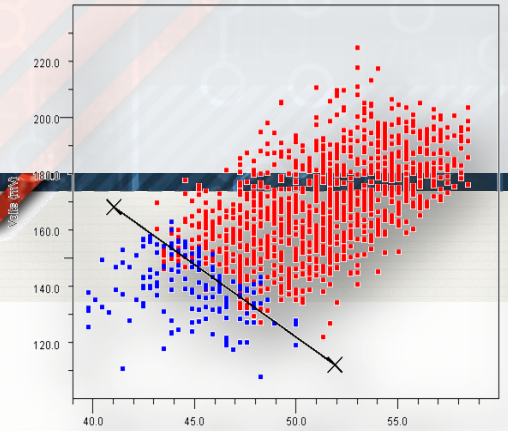


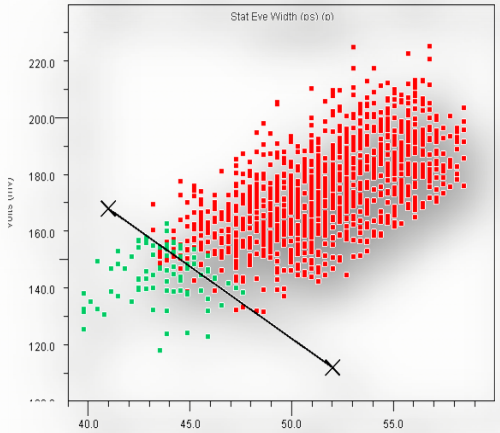
Main Cursor +

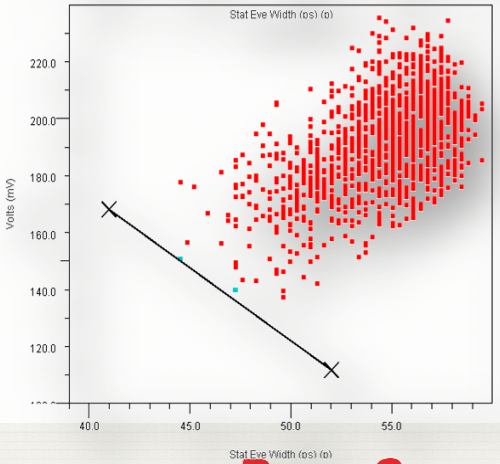


Resolving Performance

- Relevant metric is BER
  - Not eye height and width
    - Combination of eye metrics
  - Diagonal line
- Two corrections necessary
  - Amp+ on medium length links
  - Improve discontinuity on short links
- Significant improvements
  - BER=ok, signals better clustered

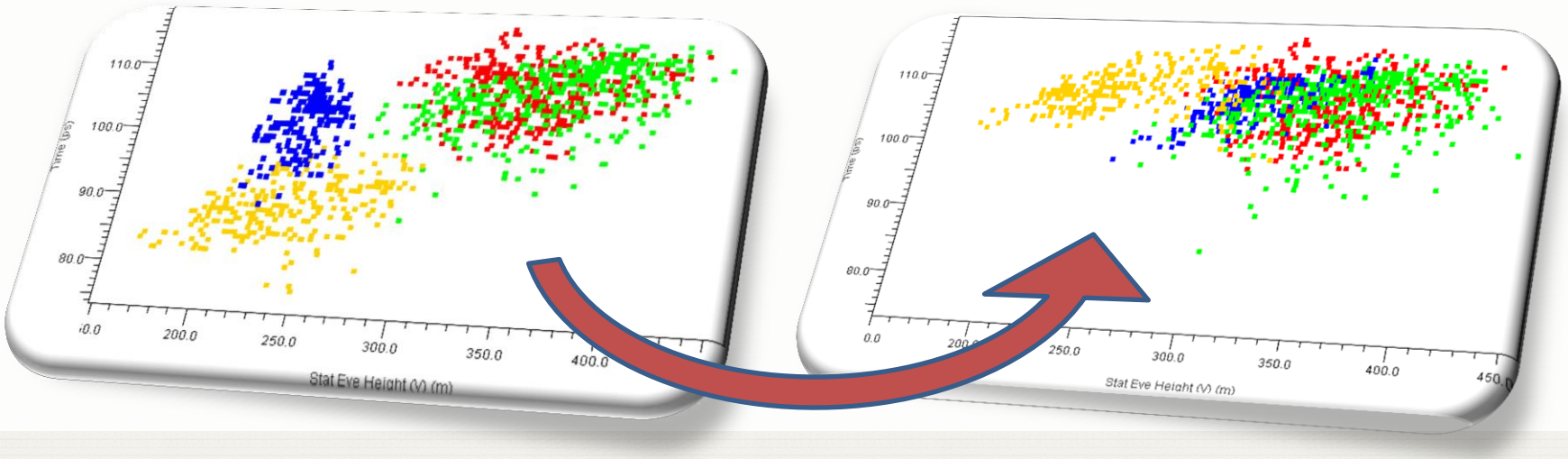






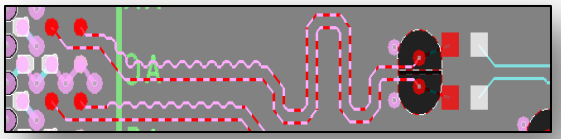
Legacy Interoperability Settings

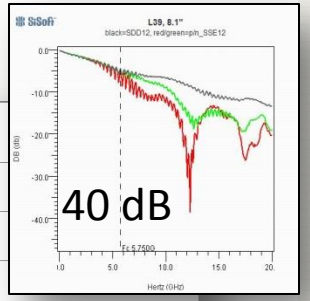
- 3rd gen interoperating with 4th gen
  - Lower data rate - can **only** adapt settings
- Long/short length link defaults, each direction
  - 4 performance groups (different colors)
  - 20+% performance improvements



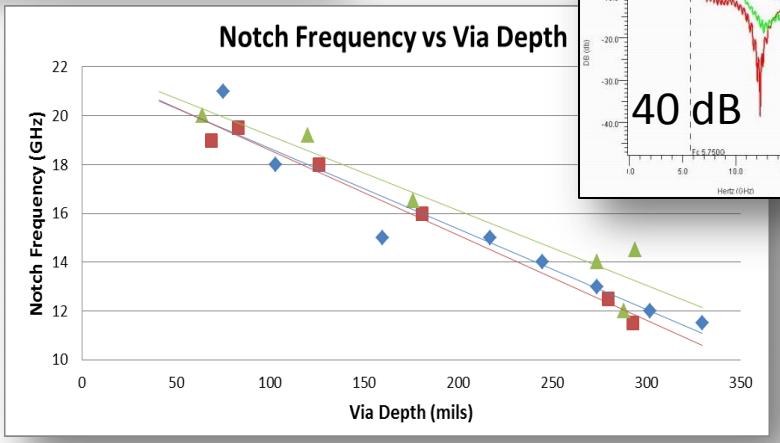
Design: Adjust Layout

- 4th generation performance influenced by layout features smaller than 30 mils
  - Via stubs, antipad traces, serpentine corrections





- Via cage asymmetries
  - Notch frequency drops 1 GHz per 30 mils of via

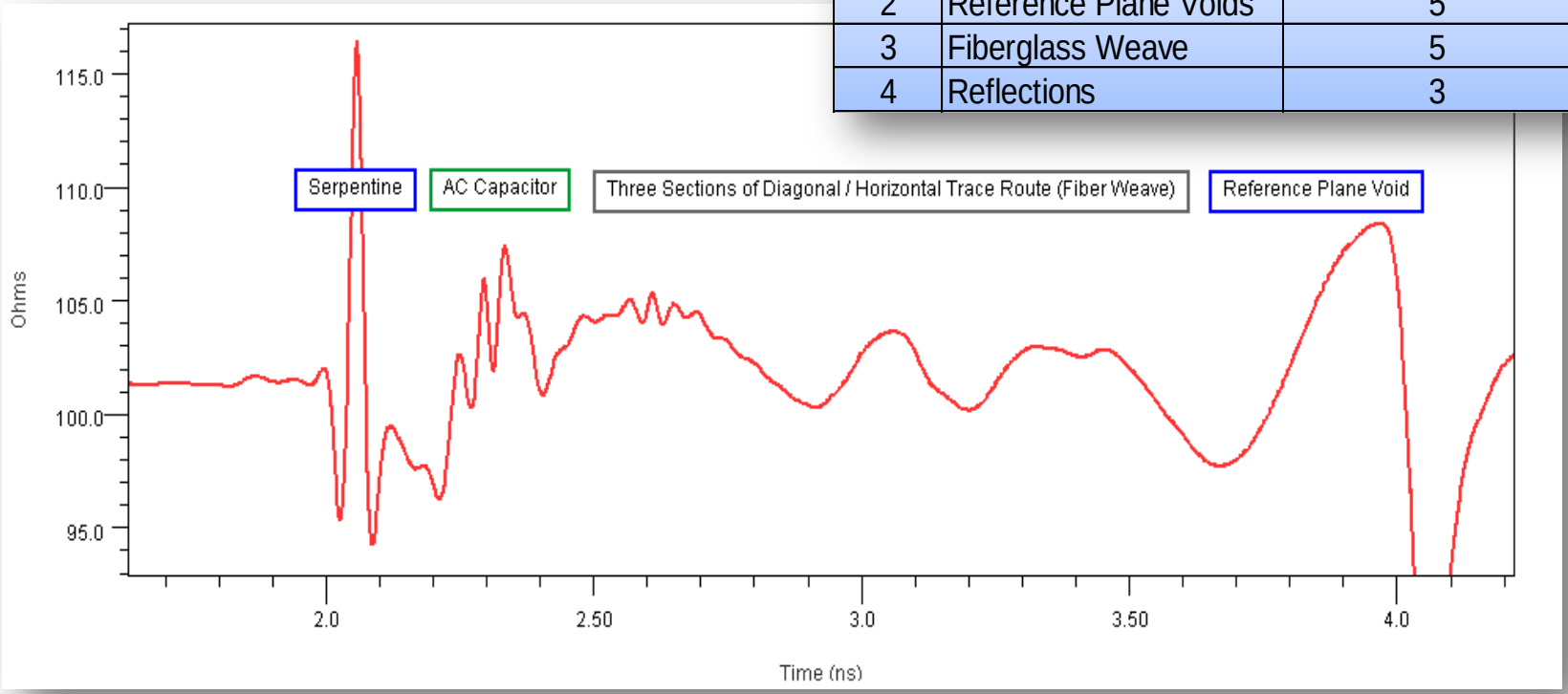


Irregular Impedances

- Features expected to show continuous impedance

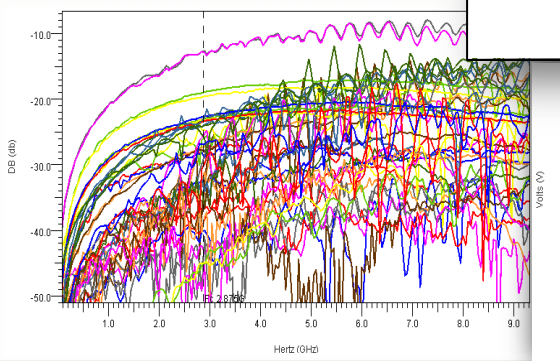
DO NOT

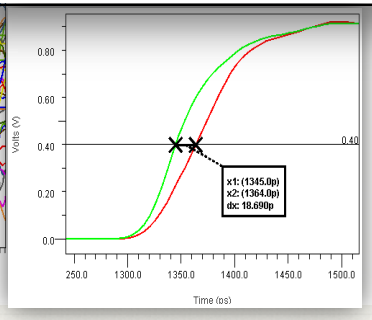
Rank	Cause	Magnitude (Ohms)
1	Serpentine Routes	15
2	Reference Plane Voids	5
3	Fiberglass Weave	5
4	Reflections	3

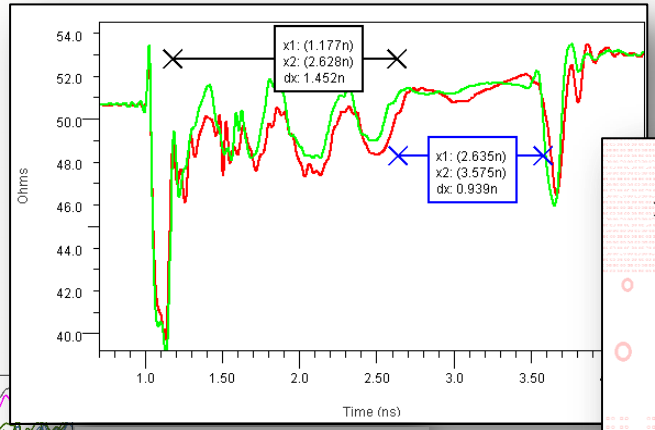


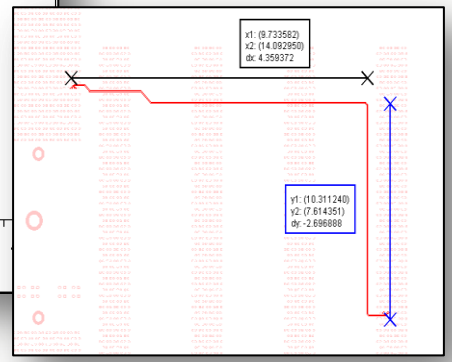
Example Measurements

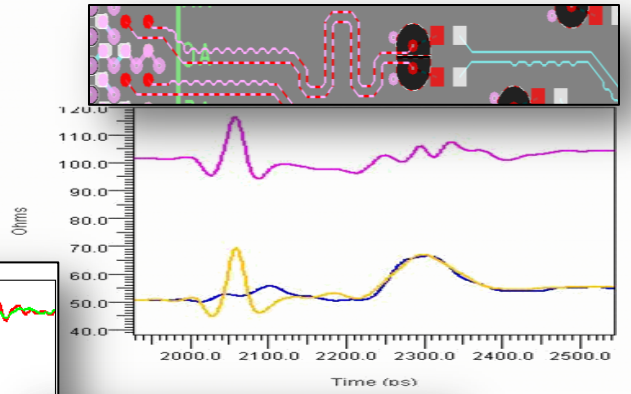
- Serpentines
- Voids
- Weave











Learn what causes irregularities and avoid

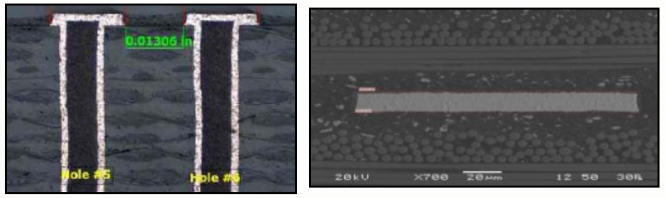
Agenda

- Introduction
- Design Improvements
- Manufacturing
  - Predictability
  - Pre-preg
  - Back-drill
- Summary

Manufacturing: Predictability

- Impedances: vias more predictable than traces

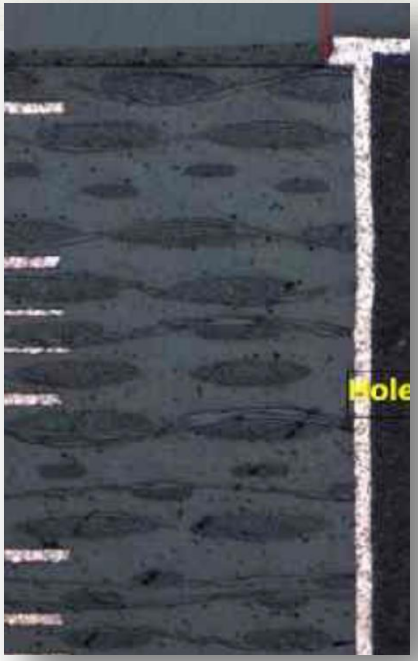
Trace Variable	Typical 4th Gen Value	Observed Variation	Unit	Impact on Impedance
microstrip				
Pre-preg height	3	1	mil	20%
Trace Width	4	0.1	mil	1%
Trace Angle	70	20	degree	10%
Dielectric Constant	3.5	5%		2%
stripline				
Pre-preg height	3.5	1	mil	10%
Trace Width	4	0.1	mil	1%
Trace Angle	80	10	degree	2%
Dielectric Constant	3.5	5%		2%
Via Variable				
Drill Size	10	0.1	mil	1%
Stub Length	10	8/4	mil	5%
Pad/Antipad Gap	10	0.1	mil	2%
Dielectric Constant	3.5	5%		2%

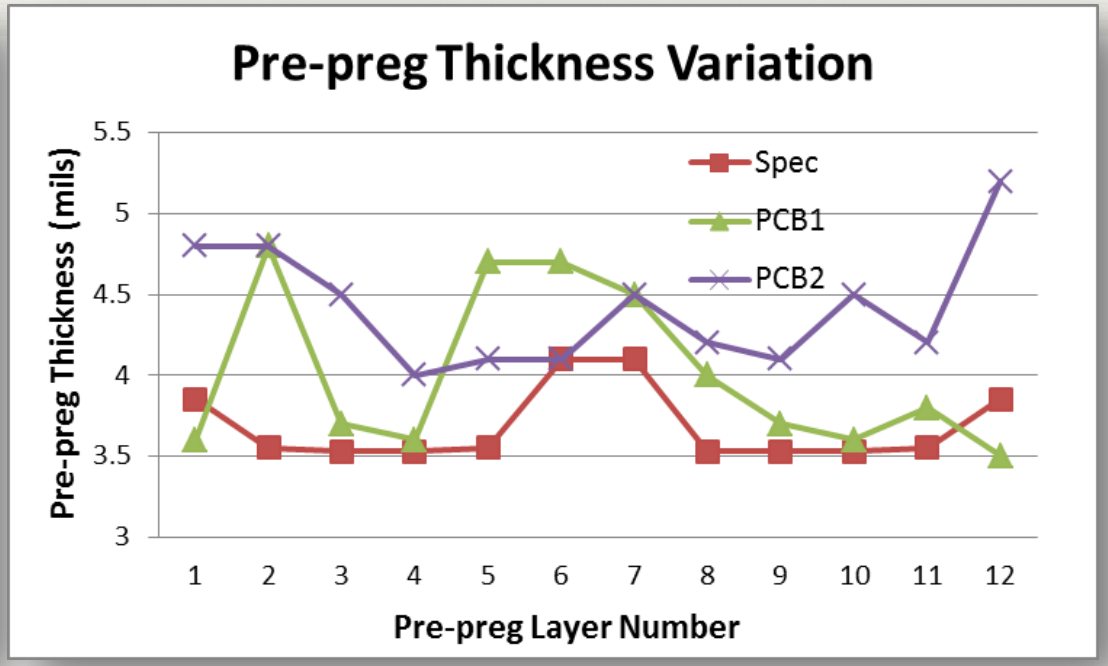


Signal	Trace Impedance (meas-sim)	Complex Via Impedance (meas-sim)	Simple Via Impedance (meas-sim)
1	-6	-3	1
2	4	-2	-2
3	4	3	0
4	-8	0	4
5	5	-5	1
6	0	6	3
7	5	-4	-2
Average	0.6	-0.7	0.7
Std Dev	5.1	3.7	2.1

(sample PCB)

Manufacturing: Pre-preg Variation

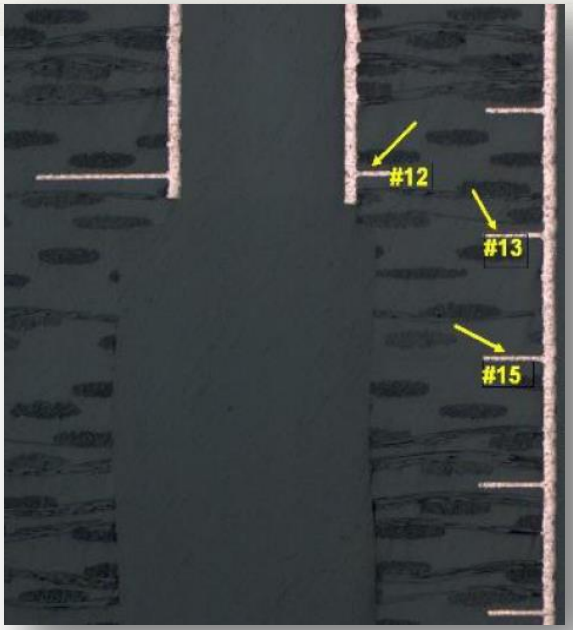


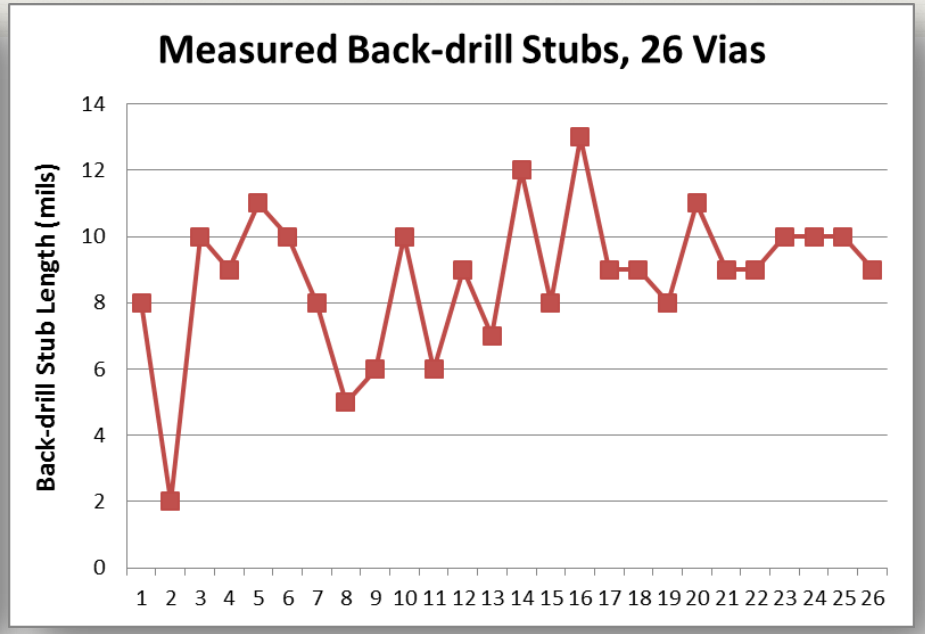


- Comparing 2 PCBs vs stackup design spec
  - Average variation is 0.53 mil, std dev is 0.46

Recommendation: use core for critical dimensions

Manufacturing: Back-drill Variation





- Photomicrographs of 26 back-drilled vias
  - Average stub length is 8.8 mils, std dev is 2.2 mils
- Causes via impedance variation of +/- 2.5 Ohm

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Summary

- Higher data rates require new techniques
  - In both Design and Manufacturing
- Discontinuities previously ignored now matter
- Default SerDes settings not optimal
- New layout concepts discussed
  - Small features can be important
- Via impedance is more reliably manufactured than trace impedance

Questions

THANK YOU

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