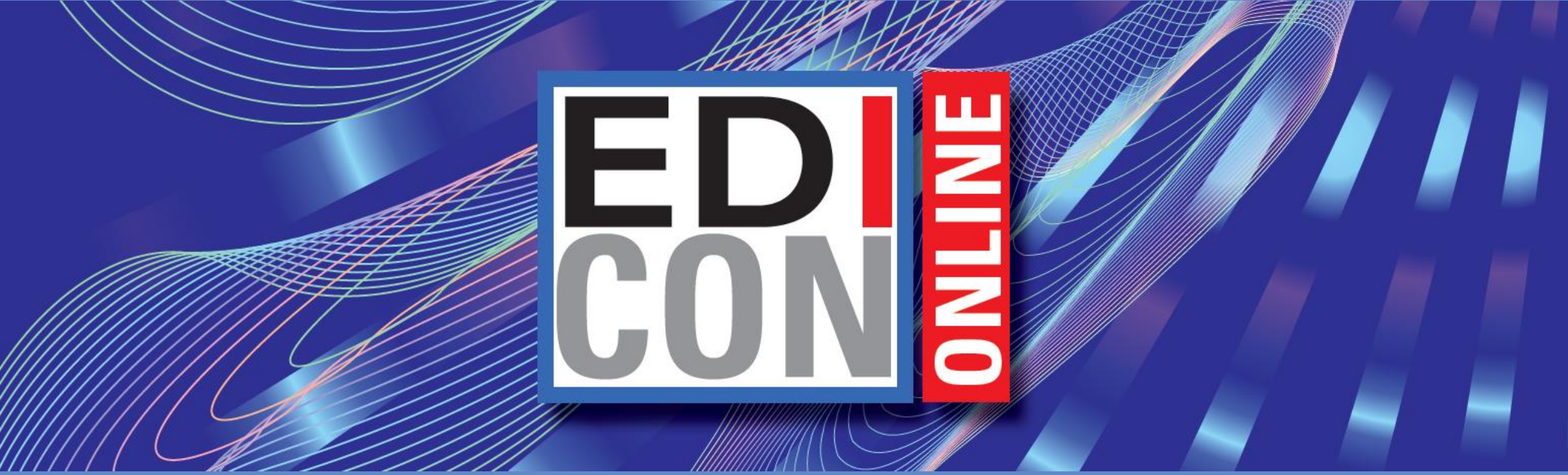


# Signal Integrity Cheat Sheet - Data-Rate Driven Design Decisions

**Presented By: Donald Telian**

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**Track: SI**

EDI CON ONLINE

**Donald Telian** is a Signal Integrity Consultant and owner of SiGuys. He celebrates four decades of SI pioneering with the publication of his new book "**Signal Integrity, In Practice**." Consulting since the beginning of the serial link revolution, he consistently helps customers migrate to next-generation data rates again and again. With tens of thousands of serial links in production spanning all types of electronic standards and products, he simplifies SI by sharing what's necessary and what isn't. Donald is widely known as the SI designer of the **PCI** bus and the originator of **IBIS** modeling and has taught SI techniques to thousands of engineers in more than 15 countries. His book "Signal Integrity, In Practice" brings fresh articulation to the practice of SI for the decades ahead.

# Signal Integrity has CHANGED

(we might even say:  simplified)

# Why do I say that?

- Signal Integrity no longer used for PCB-level timing closure
  - Serial links embed timing within signals
- DDRx SI handled with proven cut-and-paste layout examples
- Rx (and Tx) equalization increasingly powerful
  - Much of SI is now handled inside the chip, little/no signal seen on PCB
- Decreasing industry demand for SI training (staff?)
  - Comes in waves, next one is approaching
- SI skills deployed for “out-of-the-box” implementation

*Nevertheless, there’s some basic things to know. Ready?*

# Signal Integrity Cheat Sheet


| Feature | 4 Gbps | 8 Gbps | 16 Gbps | 32 Gbps | Unit | SIiP Section |
|---|---|---|---|---|---|---|
| Industry/PCIe terminology | Gen2 | Gen3 | Gen4 | Gen5 | | |
| Fundamental Frequency | 2 | 4 | 8 | 16 | GHz | |
| Relevant Feature Size<br>what's that? | 160<br>traces | 80<br>vias | 40<br>conn pads | 20<br>everything | mils | 4.1, 2.1, 4.x<br>4.2, 4.3, 4.4 |
| Max Stub<br>backdrills | 64<br>none? | 32<br>seq-lam | 16<br>2 layers | 8<br>per-layer | mils | 2.5, 1.3.3 |
| P/N Matching, static | 10 | 5 | 2 | 1 | mils | 2.3 |
| P/N Matching, dynamic | | | 10 in 1.5" | 5 in 1" | mils | 2.3, 2.4 |
| Route Style | 45° | 45° | curved | curved | | 2.4 |
| Diff-pair Spacing (XY/Z, min) | 25 | 25 | 25 | 30 | mils | 5.3 |
| Insertion Loss (max) | 16 | 22 | 28 | 36 | dB | 2.2, 3.5 |
| Min EQ: Tx_FFE/Rx_DFE taps, CTLE | 1 / 0 | 2 / 1, C | 2 / 2, C | 2 / 3, C | #taps | 3.3, 3.4, 2.7 |
| Length match method | serpentines | | irregular spaced bumps | | | 2.4 |
| Fiberglass weave | spread glass and rotate image 12 degrees on panel | | | | | 2.6 |
| GND Return Vias (GRVs) | within 30 mils of signal layer transition (see DesCon 2022) | | | | | Figure 17 |
| Solid GND reference layers | both sides of trace (don't use microstrips) | | | | | 2.3, 2.6 |

To avoid crosstalk

*that's my new book →*

# Relevant Feature Size (RFS)

- What is the smallest structure a signal will “see” at a given data rate
  - As such, need to solve/match impedance to prevent reflection (noise)
- RFS = 0.6 * UI mils (UI in ps)
  - Based on edge-rate/round-trip
- Details at Signal Integrity Journal

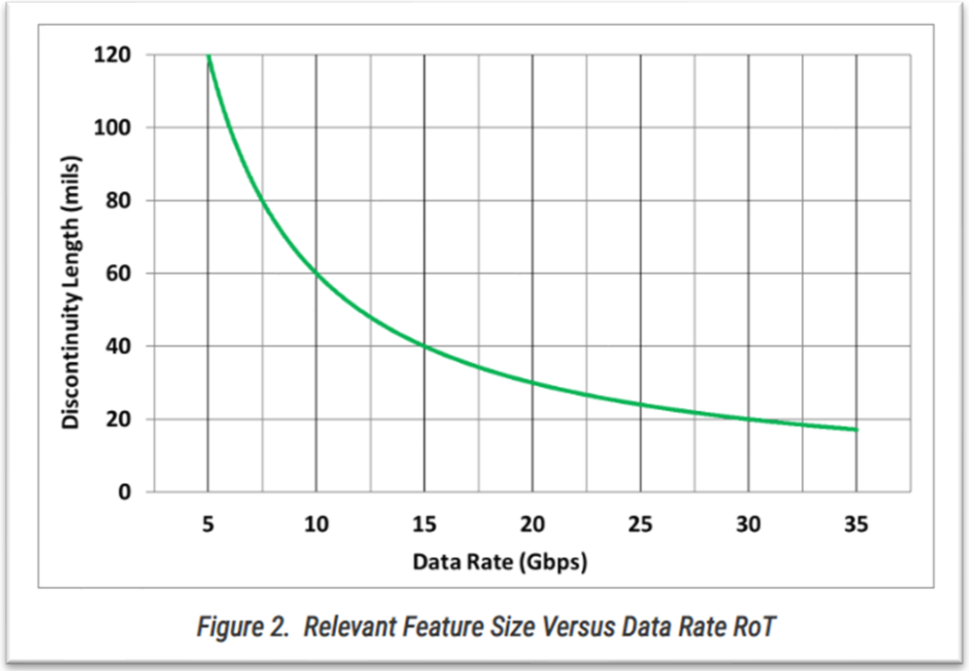
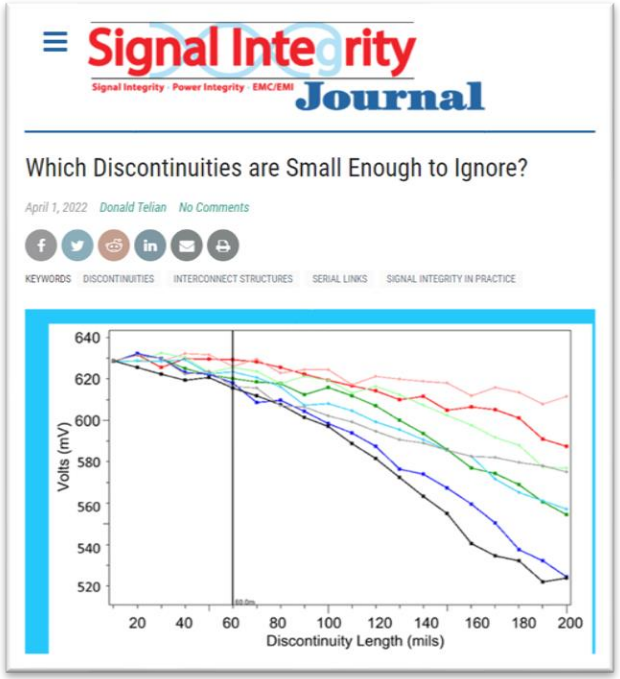
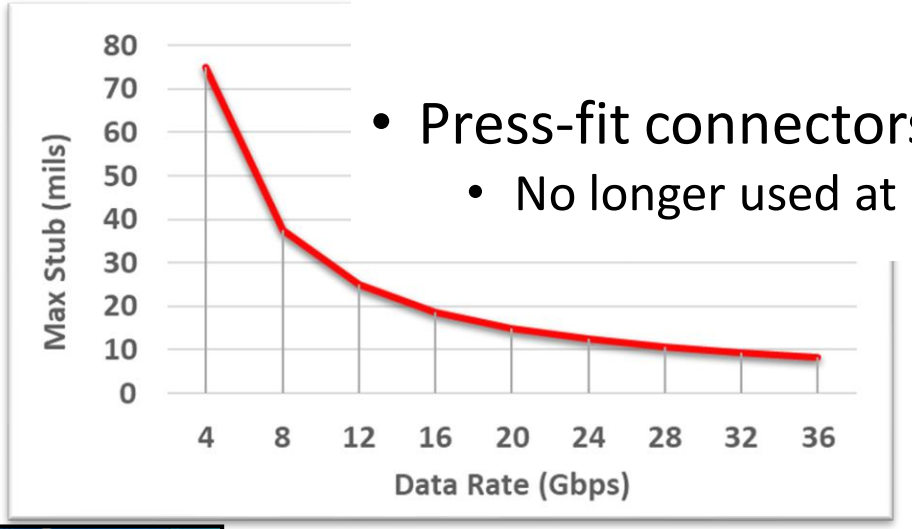


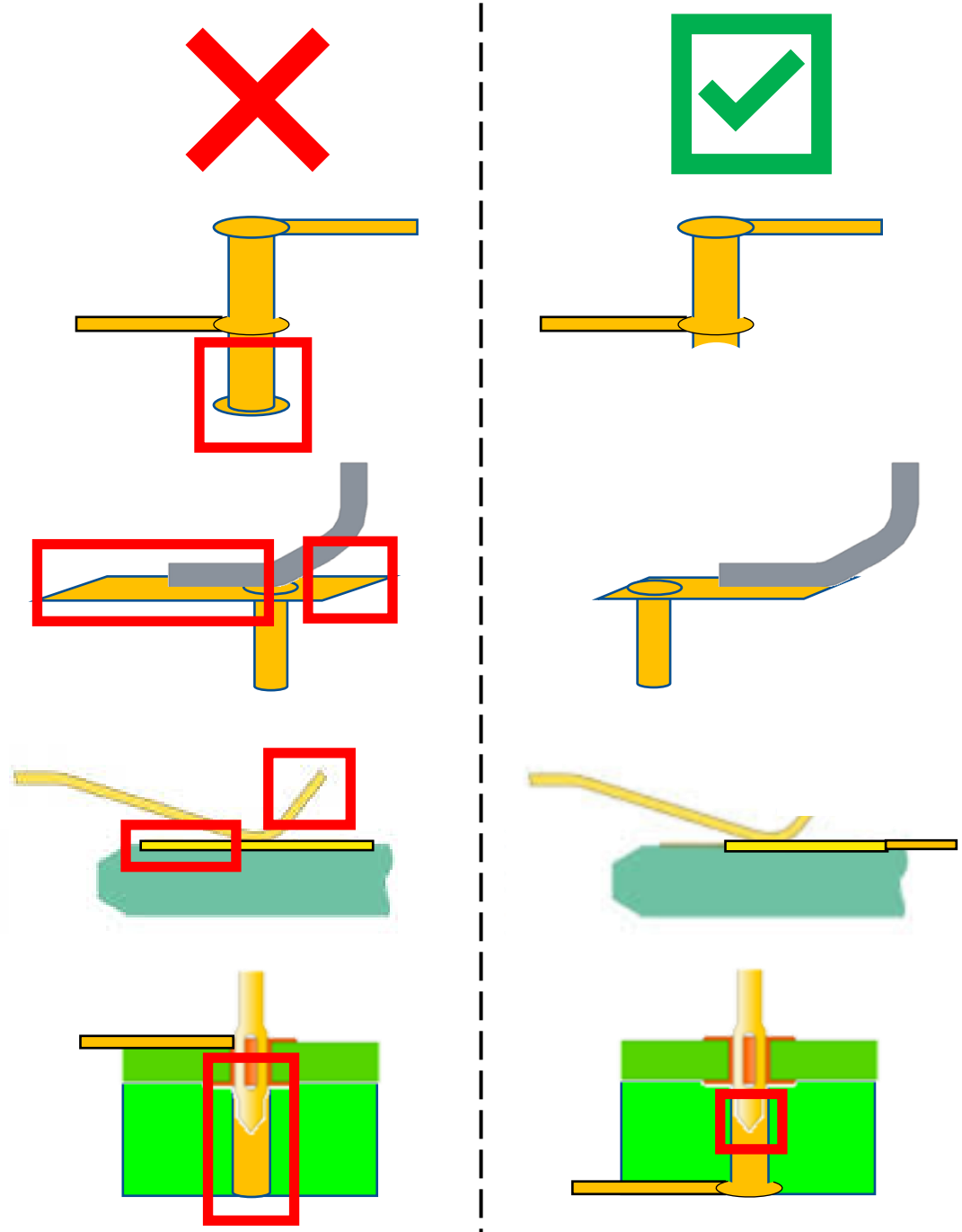

*Figure 2. Relevant Feature Size Versus Data Rate RoT*



# Must remove ALL stubs

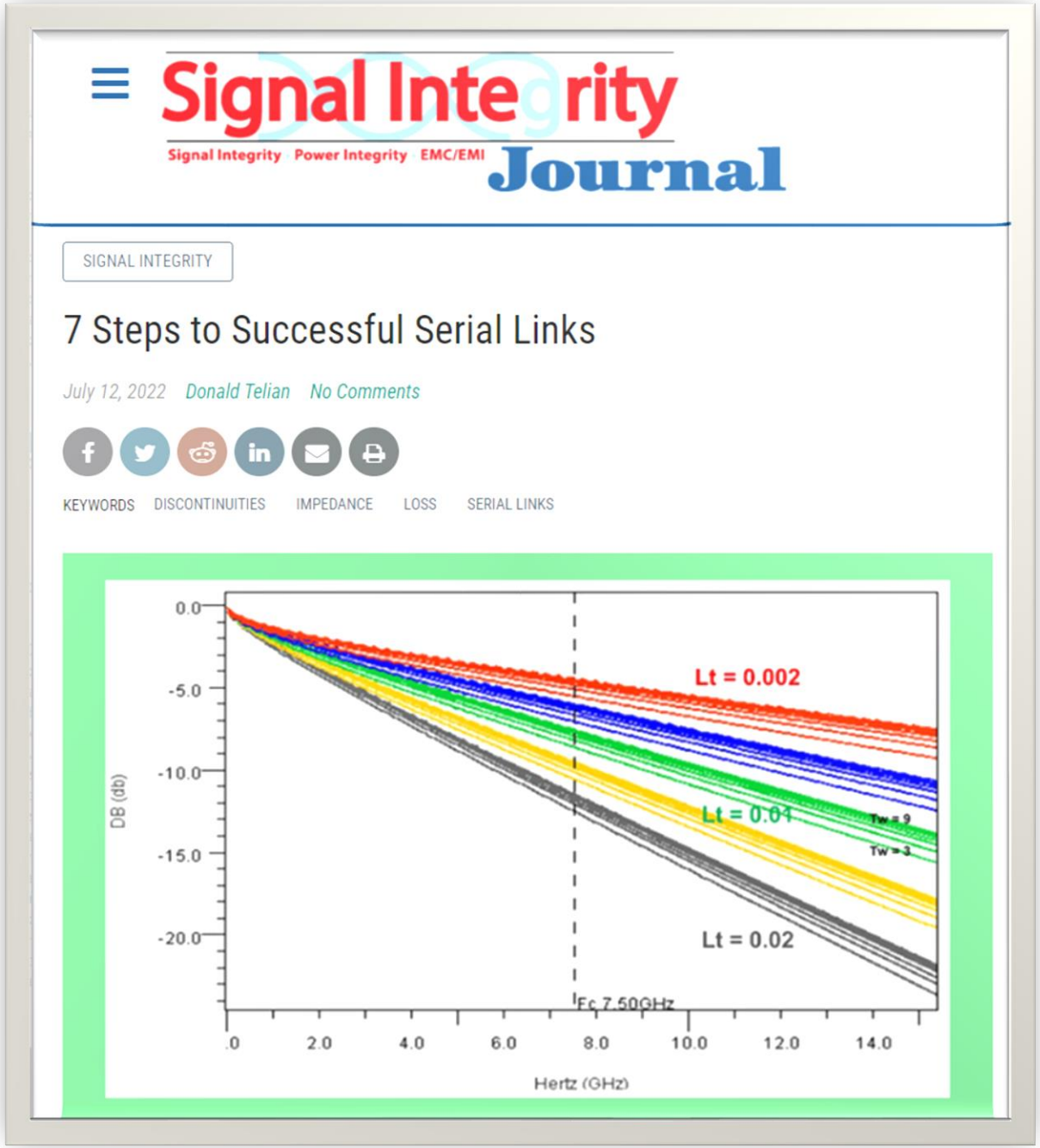
- Backdrill vias
  - Gen3/4 failures
- Remove stubs at solder pads
  - Gen5 failures
- Minimize stubs at edge fingers
  - Should be handled by standard
- Press-fit connectors are messy
  - No longer used at higher speeds



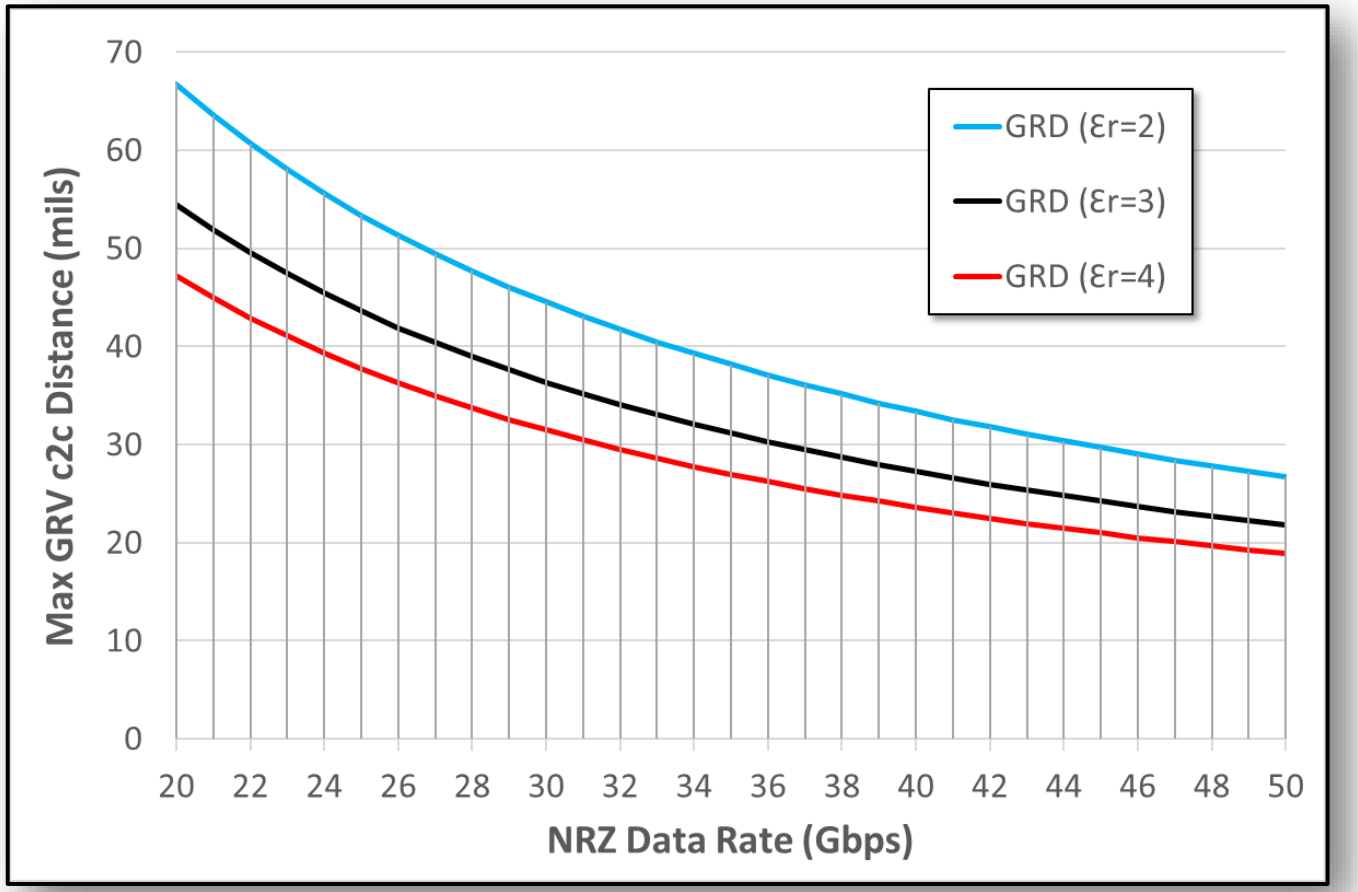
# Loss

- Can vary 4x in 12” of trace
  - Depending on construction (Lt/Df and Twidth, primarily)
- For many Gens, we’ve reduced loss by using newer materials
  - But this may be changing
- Step 2 in the “7 Steps” series
- EQ mainly handles loss



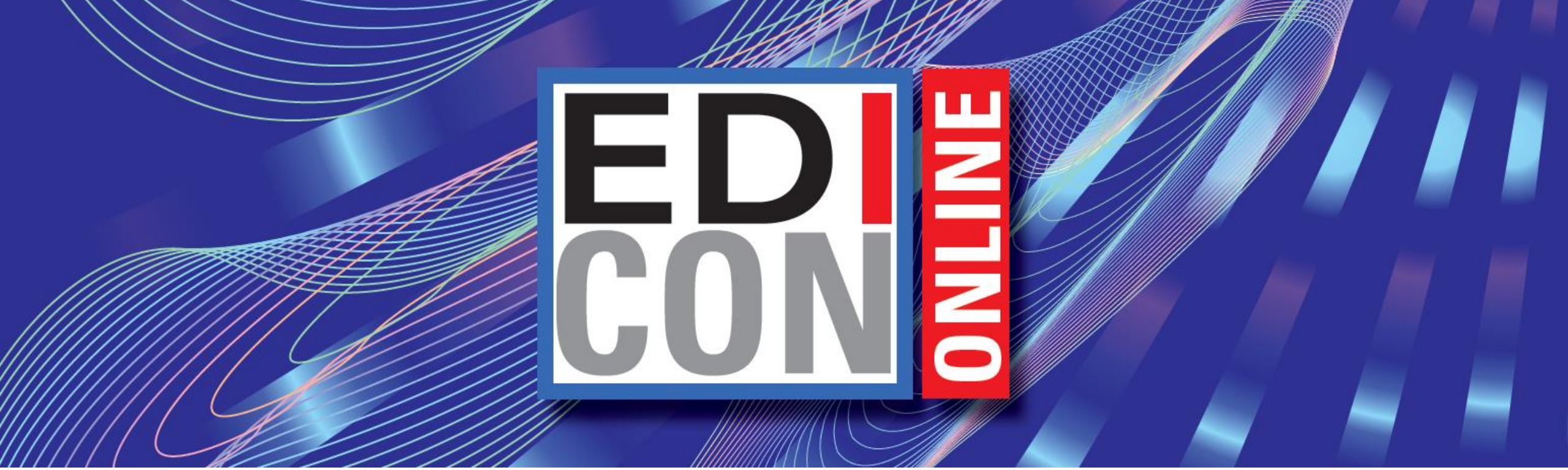
# Ground Return Vias (GRVs)

- Gap-Rate Distance (GRD)
  - Signal to GRV distance
  - Center-to-center maximum
  - Based on data rate
- DesignCon 2022 Best Paper:
  - “Proper Ground Return Via Placement for 40+ Gbps Signaling”
- Will be at Signal Integrity Journal soon



# In Summary

- Signal Integrity, in practice, has changed/simplified
- Some basic skill necessary to succeed with mainstream SI
  - Captured in the “7 Steps” and “Cheat Sheet”
- Use data rate to make good design decisions
  - Determine what works, and where to focus effort
- As data rates increase:
  - Smaller features become relevant
  - More “stubs” must be managed
  - Loss becomes harder to remove
  - GRVs must move closer




# Thank You for Attending

# Questions?