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Implementing Multi-Gigabit Serial Links in a System of PCBs

Donald Telian

April 2002

rev. 1.2

XILINX® IBM WindRiver CMP United Business Media Electronics Group

About the Author

Donald Telian

Technologist, Cadence Design Systems

Donald has been involved in high-speed PCB design for over 17 years. At Cadence, he works with industry leaders to develop next generation tools, technologies, and "Design Kits" to support advances in technology. Prior to that, Donald worked at Intel Corporation where he founded and managed the Signal Integrity Engineering group that resolved high-speed design issues for 10 Intel Architecture desktop platforms for 486, Pentium(R), and PentiumPro processor-based systems. He also led the design and validation of the PCI Bus electrical specification, co-wrote the original IBIS specification, and founded the IBIS Open Forum.

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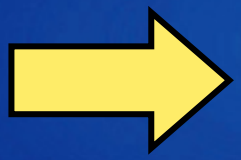
Multi-Gigabit Links on PCBs

AGENDA

- Industry Trends
- Process Overview
- Process Step Details
- Summary & Resources

Multi-Gigabit Links on PCBs

AGENDA



- **Industry Trends**
  - Data Movement
  - Analog Challenges
  - Higher Integration
  - New Solutions
- Process Overview
- Process Step Details
- Summary & Resources

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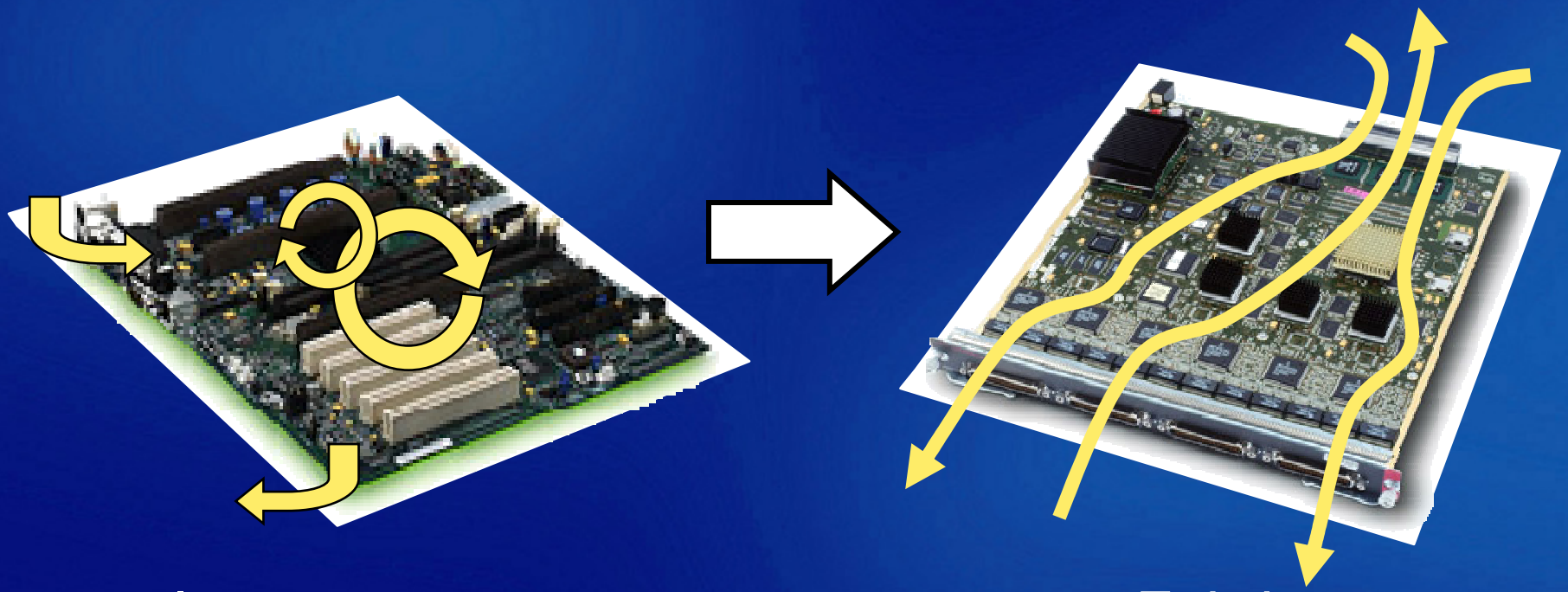
#1: Data Movement

"Data Processing" to "Packet Switching"



Interconnects

Fabrics

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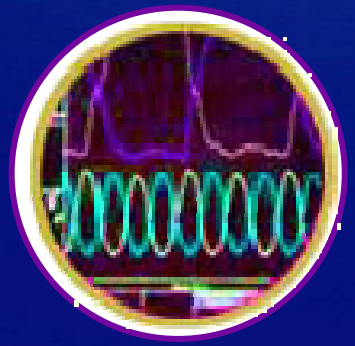
#2: Analog Challenges

"A state-of-the-art serial link can move 3.125 Gbits/s – three to four times faster than Rambus and other high-speed interfaces. ***Achieving that speed across a backplane is not easy. …fabric designers must possess high-speed analog expertise to keep pace.***"

Linley Gwennap "Fabrics make the switch", EETimes January 14, 2002 – page 37



Digital/Analog → **Analog**/Digital

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#3: Higher Integration

"We're now at the point where it's getting cheaper to put more gates behind a fast serial line than to lay down copper traces."

Jim Pappas, Intel – commenting on why 3GIO used serial technology and PCI used parallel – EETimes February 18, 2002 page 92

Traces → **Gates**

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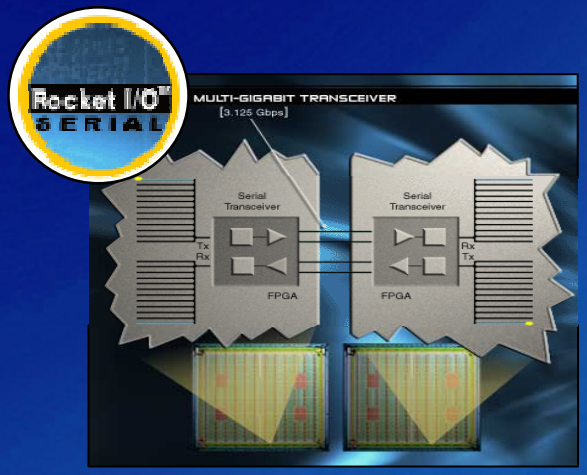
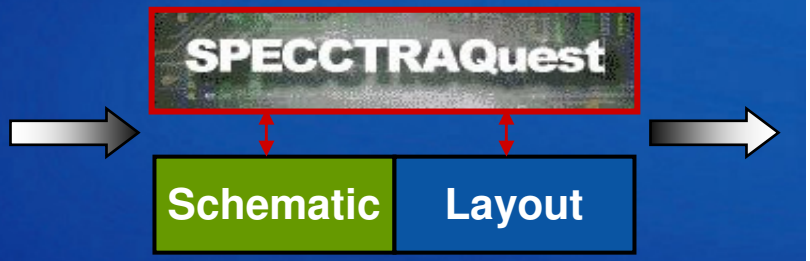
New Solutions

- Virtex-II Pro™ FPGA with Rocket I/O™ transceivers
  - Up to 3.125 Gbits/s
  - Supports XAUI, Infiniband, 3GIO, …
- SPECCTRAQuest
  - High-speed PCB constraint & analysis
  - Integrated IC and PCB simulation
- High-Speed Design Kits
  - Fastlane to implementation
  - First of its kind offering





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Multi-Gigabit Links on PCBs

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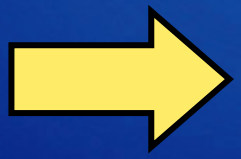
- Industry Trends
- **Process Overview**
  - Flow Diagram
  - Iterations
  - Getting Started
- Process Step Details
- Summary & Resources



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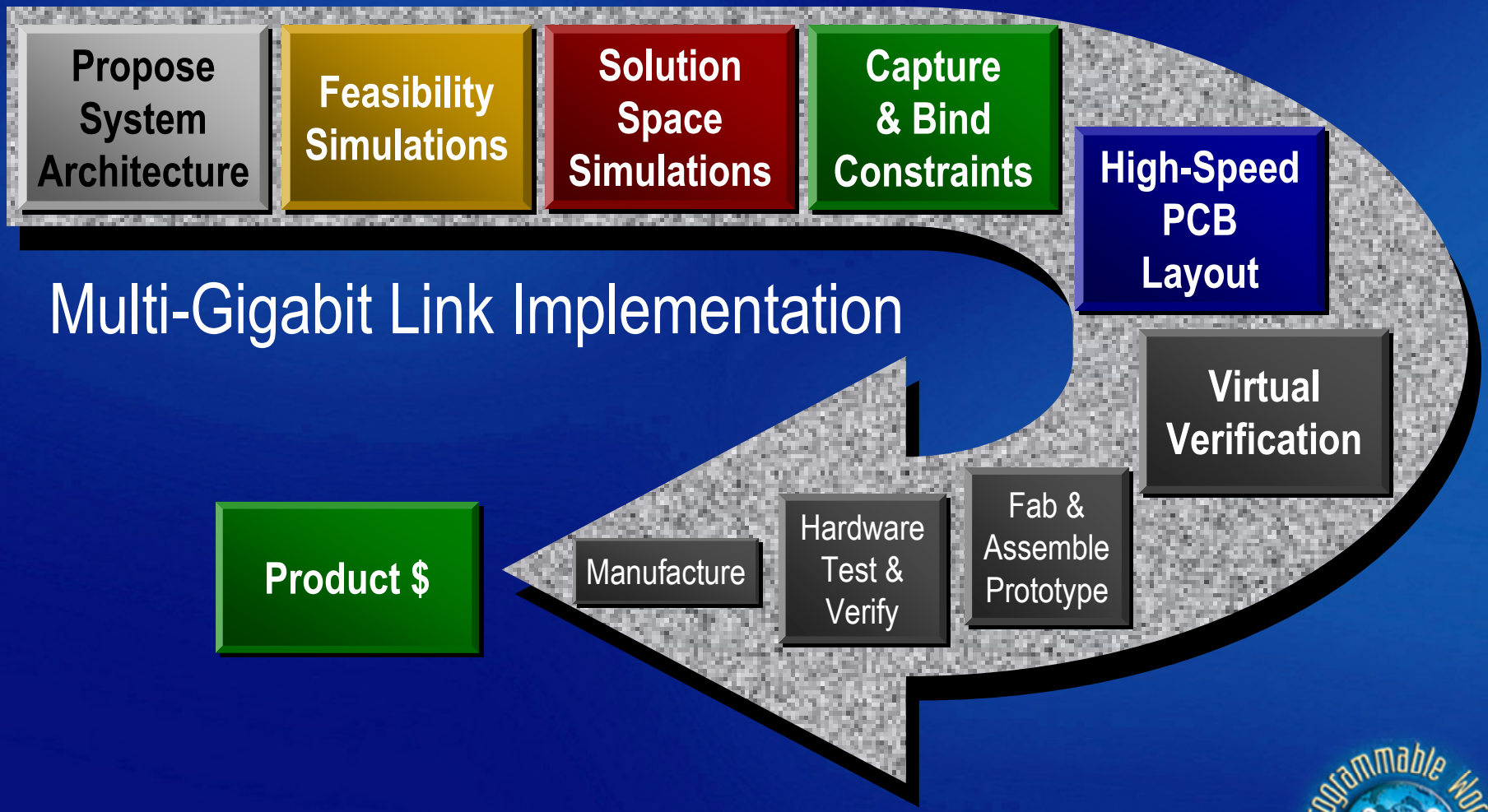
Process Overview



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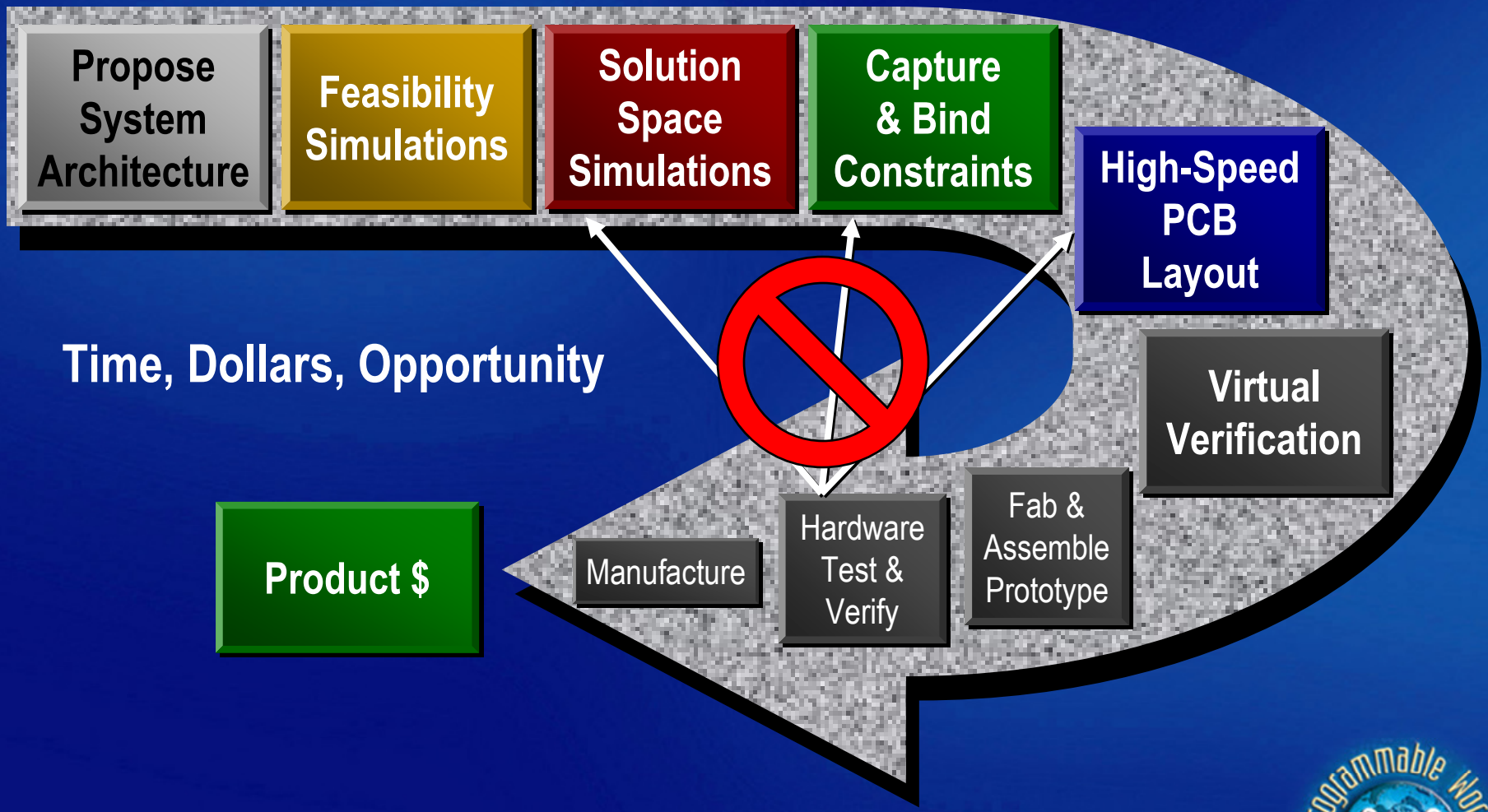
Remove Iterations



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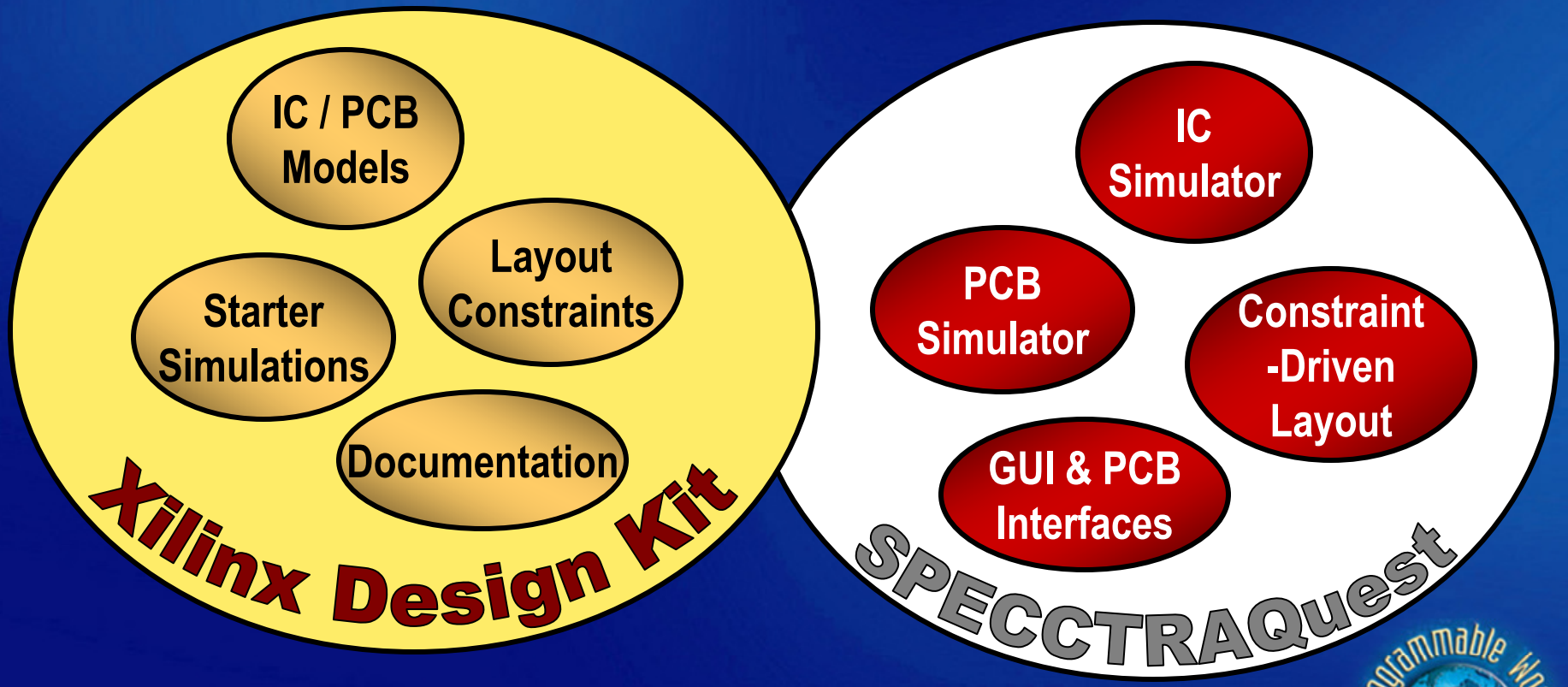
Getting Started

Start by gathering these components



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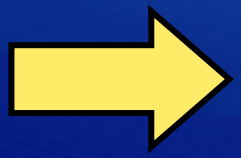
Multi-Gigabit Links on PCBs

AGENDA

- Industry Trends
- Process Overview
- **Process Step Details**
  - Challenges & solutions for each step
- Summary & Resources



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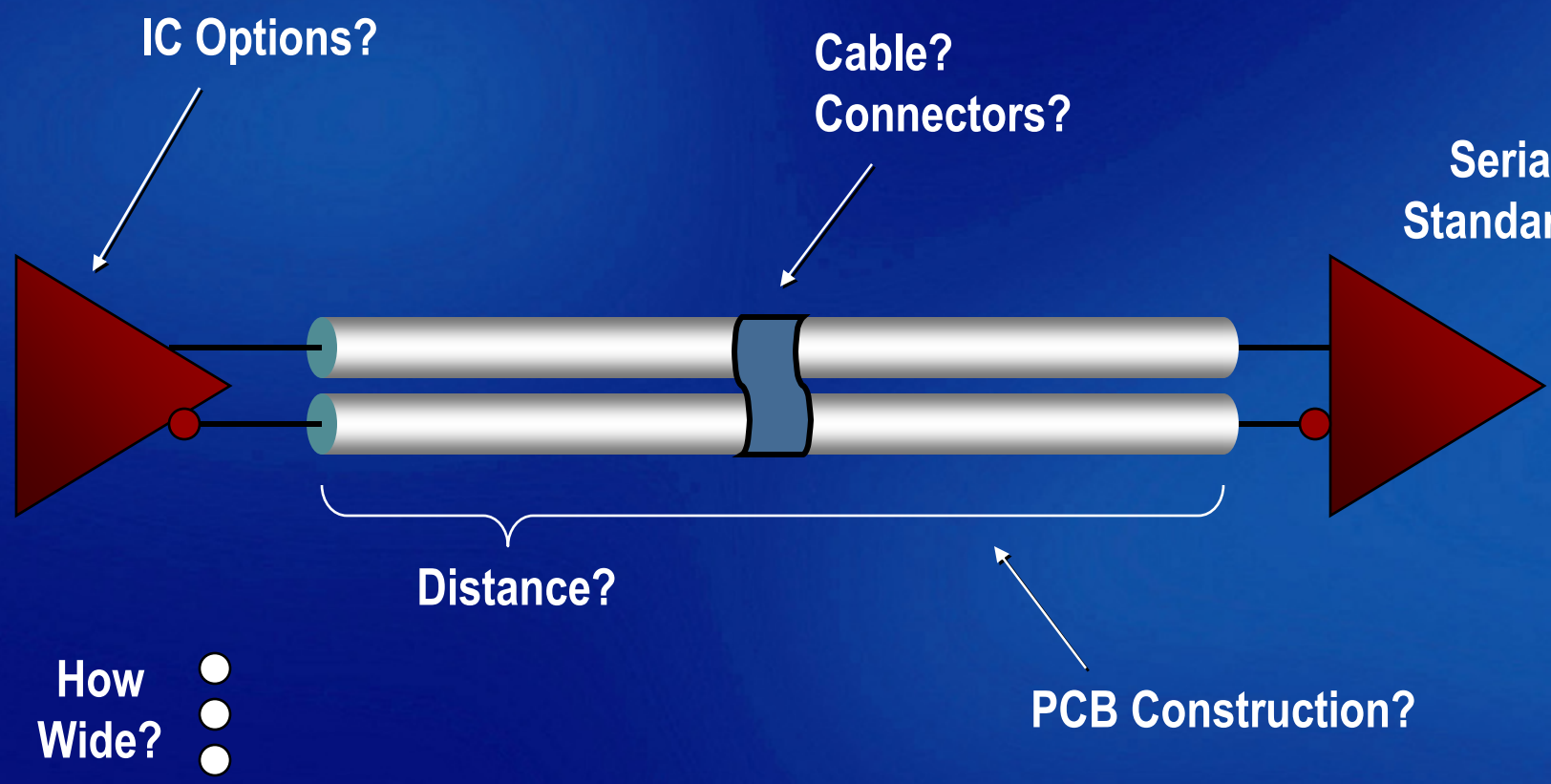
#1: Architecture

Propose System Architecture



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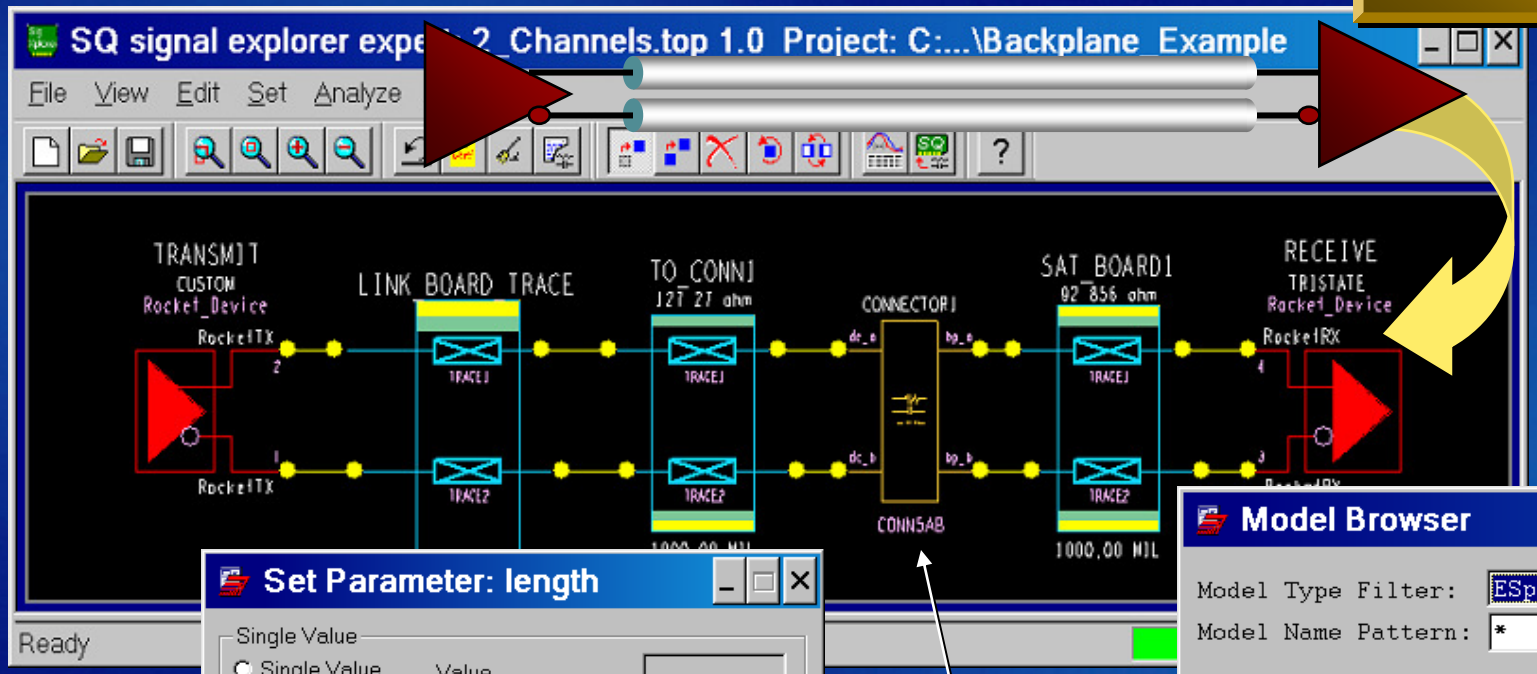
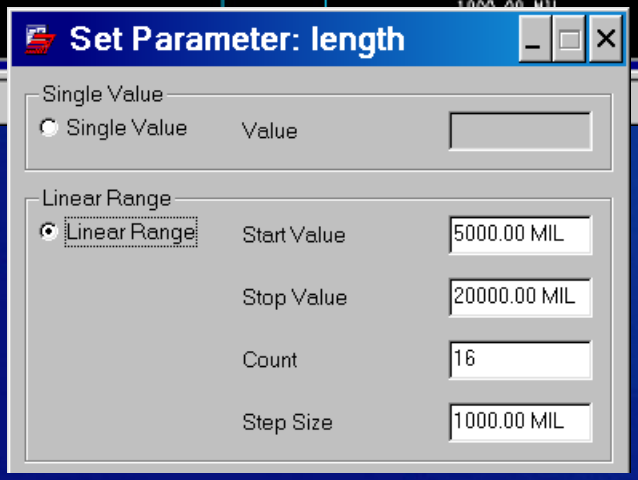
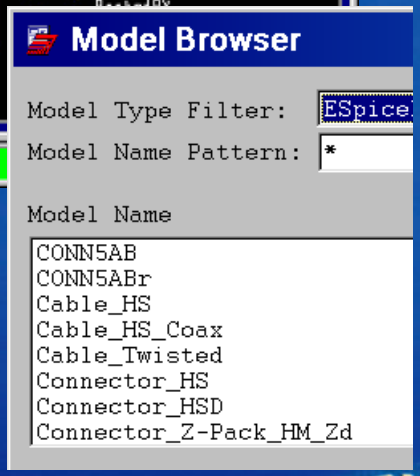
#2: Feasibility

Feasibility Simulations







Distance?

Cable? Connectors?

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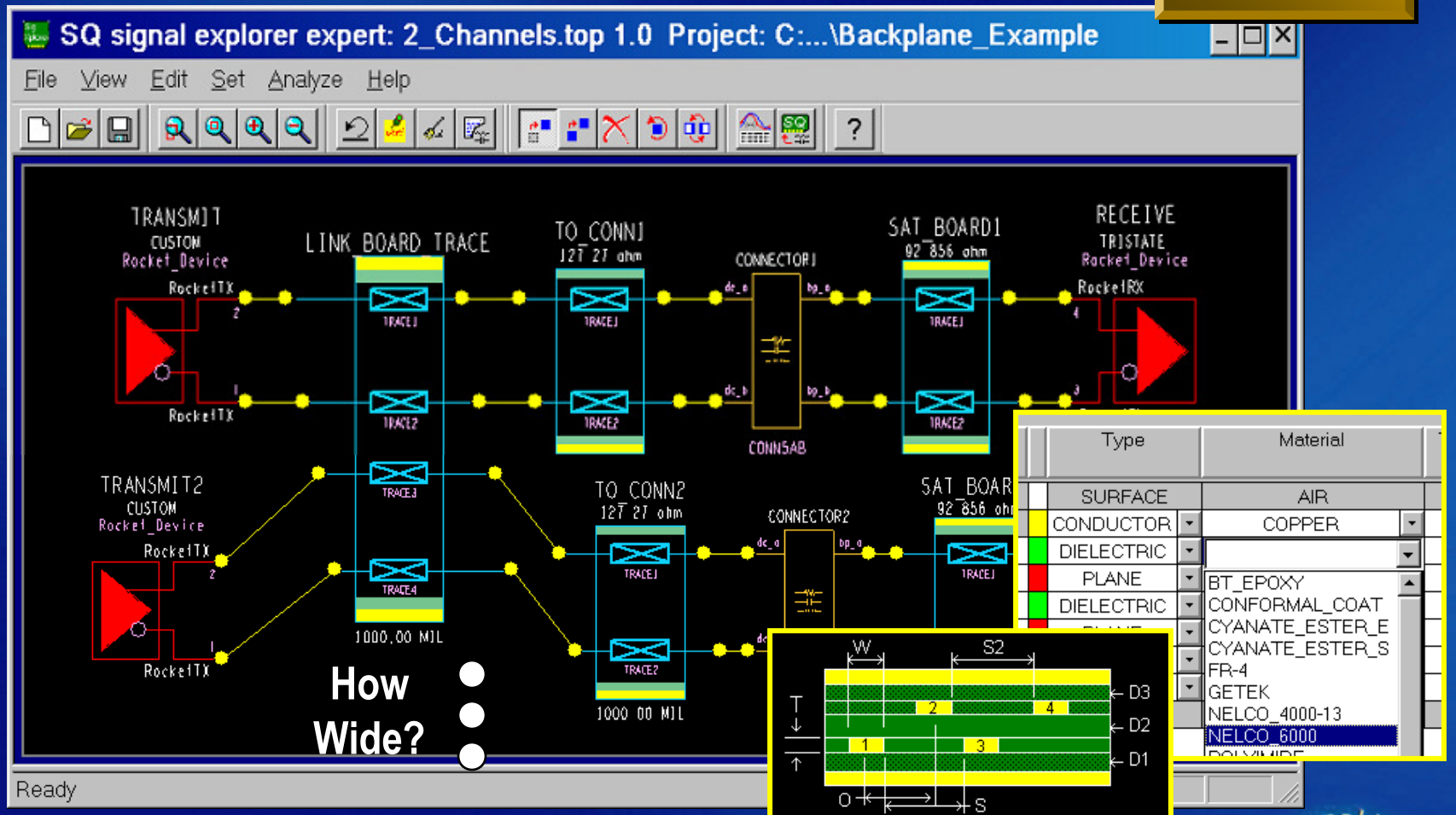
#2: Feasibility cont'd

Feasibility Simulations



PCB Construction?

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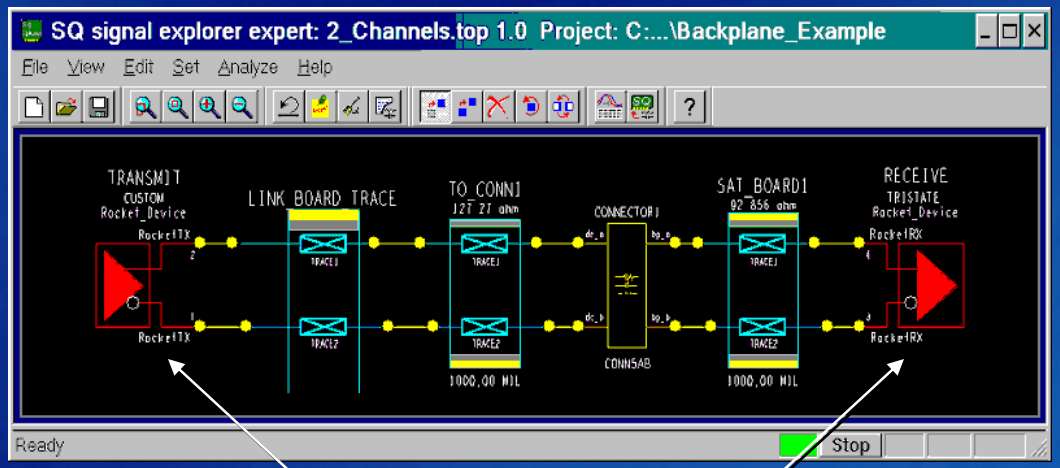
1 & 2: Concurrency

Propose System Architecture ↔ Feasibility Simulations

- Direct use of silicon model in SPECCTRAQuest
  - Encrypted too
- > 20x faster to include
  - Compared to conversion to behavioral model (data in notes)
- SPECCTRAQuest
  - Supports IBIS 3.2, Hspice, and MacroModel structures



Can use structural transistor-level (Hspice) models concurrent with IC development & test

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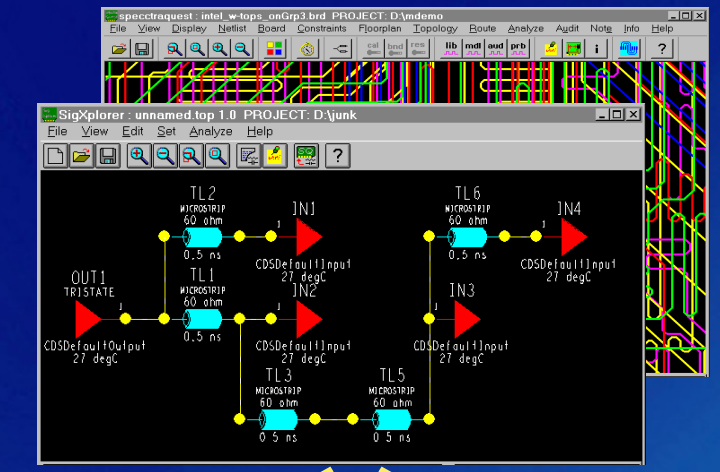
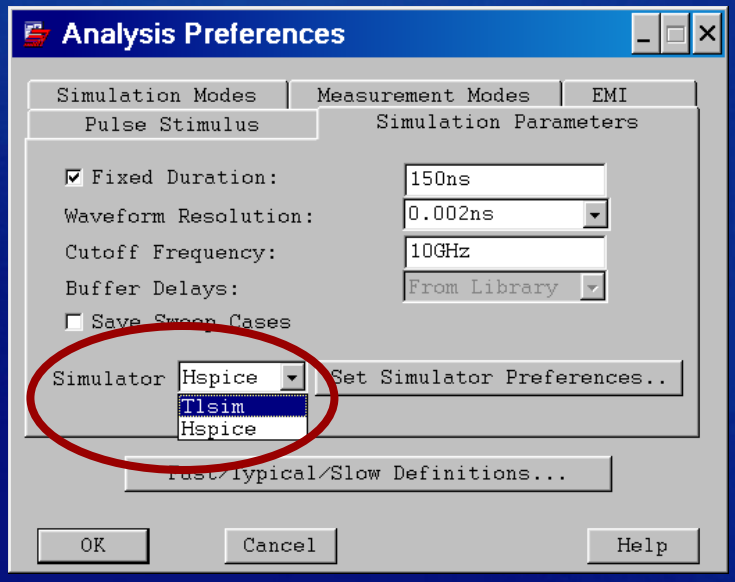
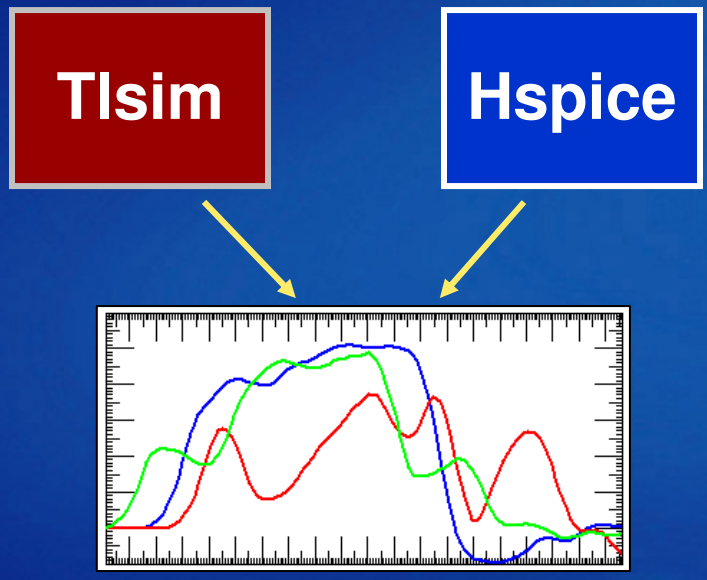
Simulator Option

Can use Hspice option for:

1. Concurrent IC/PCB Design
2. Complex Silicon Models







#3: Solution Space

Solution Space Simulations

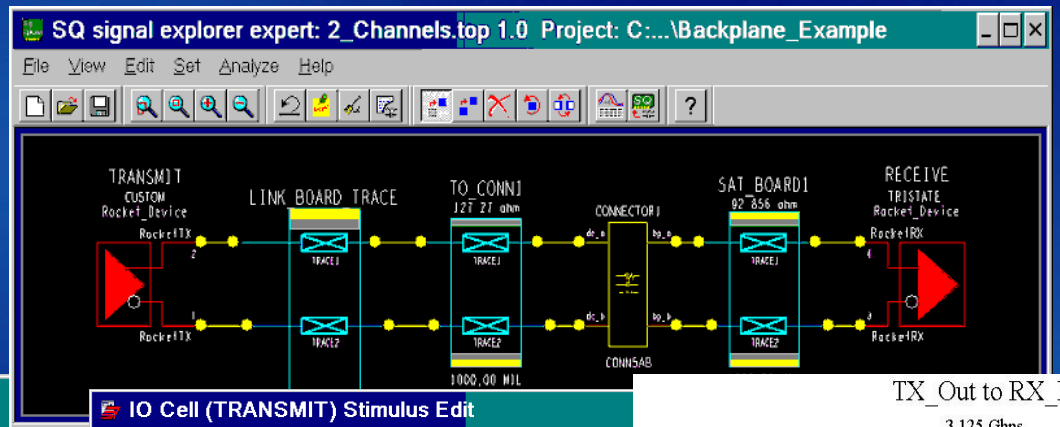
- Test / Determine
  - Voltage Swing
  - Pre-emphasis
  - AC Coupling
  - Impedance Match
  - Terminations
  - ISI, PRBS, 8b/10b
  - Jitter Tolerance
- Target / Tolerance
  - PCB Stackup
  - PCB Materials
  - Trace Geometries
  - Xtalk Spacing
  - Signal Attenuation
  - Route Mis-match
  - Power Rails

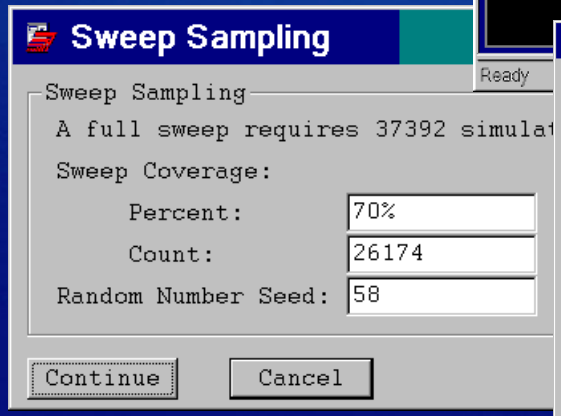
ISI=Inter-Symbol Interference, PRBS=Pseudo-Random Bit Sequence, 8b/10b=see notes

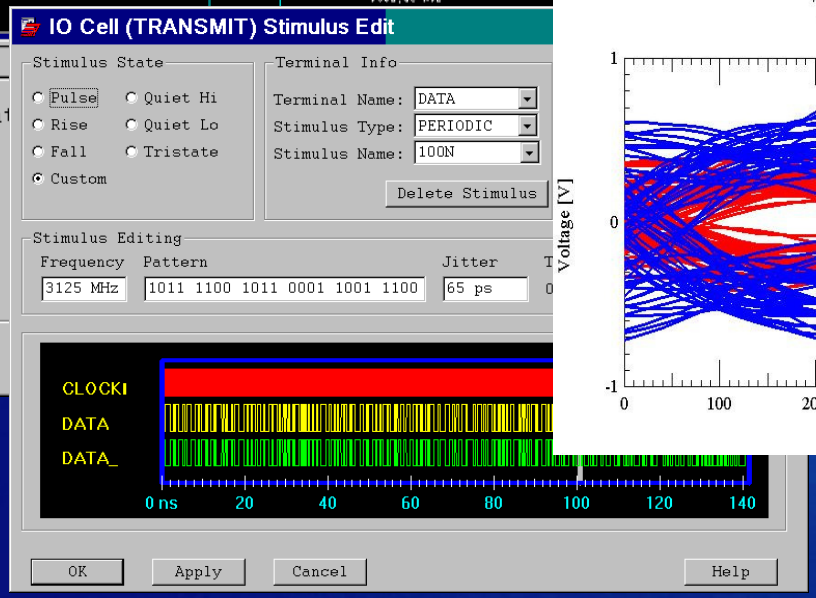
#3: Solution Space cont'd

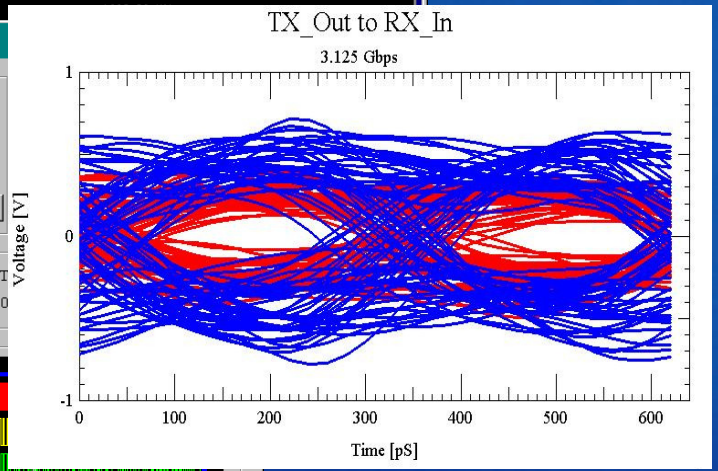
Solution Space Simulations

- Same Environment
- Sweep Simulations
- Stimulus Patterns
- Eye Diagrams
- Bound Solution









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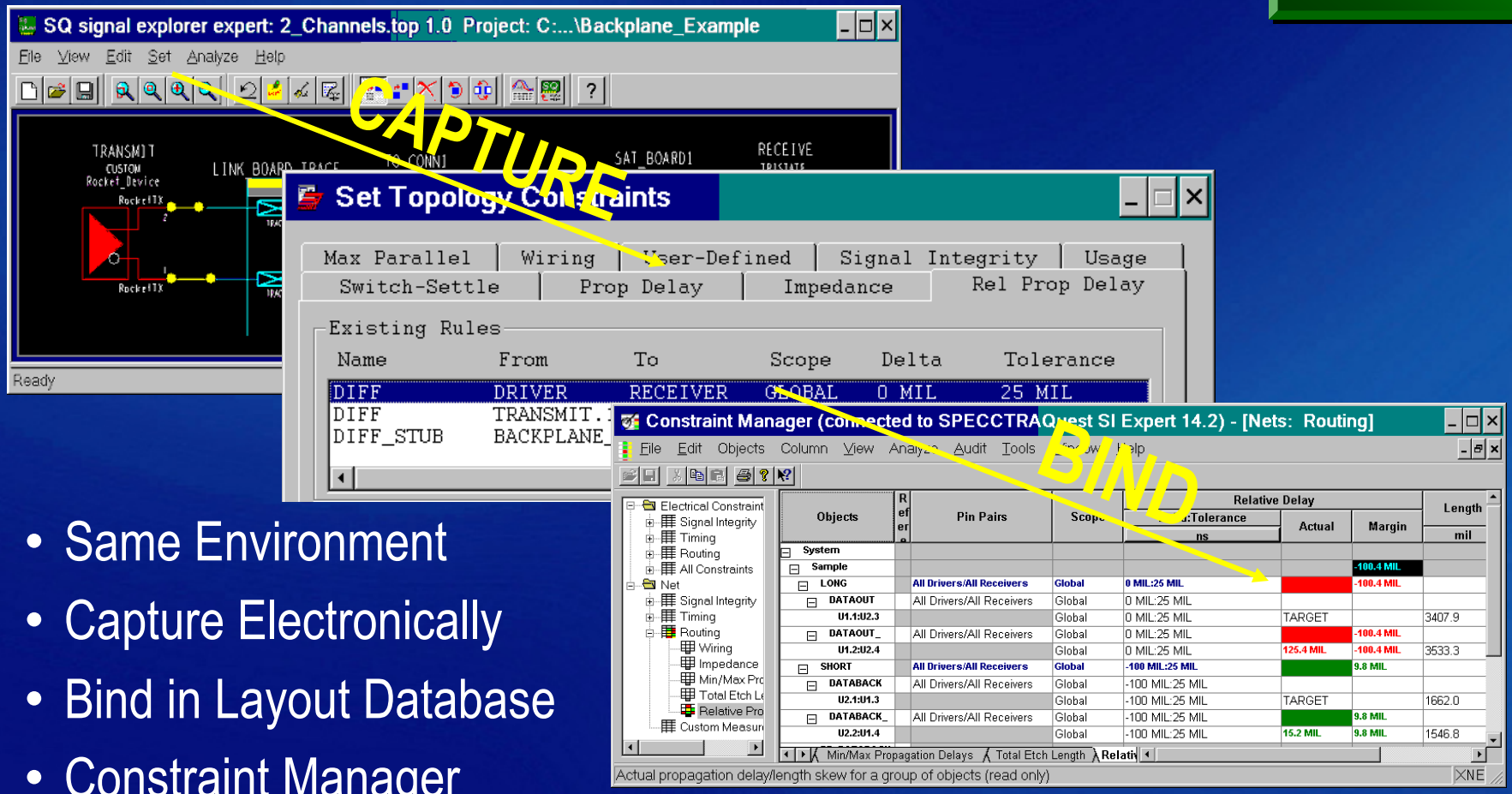
#4: Constraints

Capture & Bind Constraints



- Same Environment
- Capture Electronically
- Bind in Layout Database
- Constraint Manager
  - Schematic, Simulation, Layout Tools

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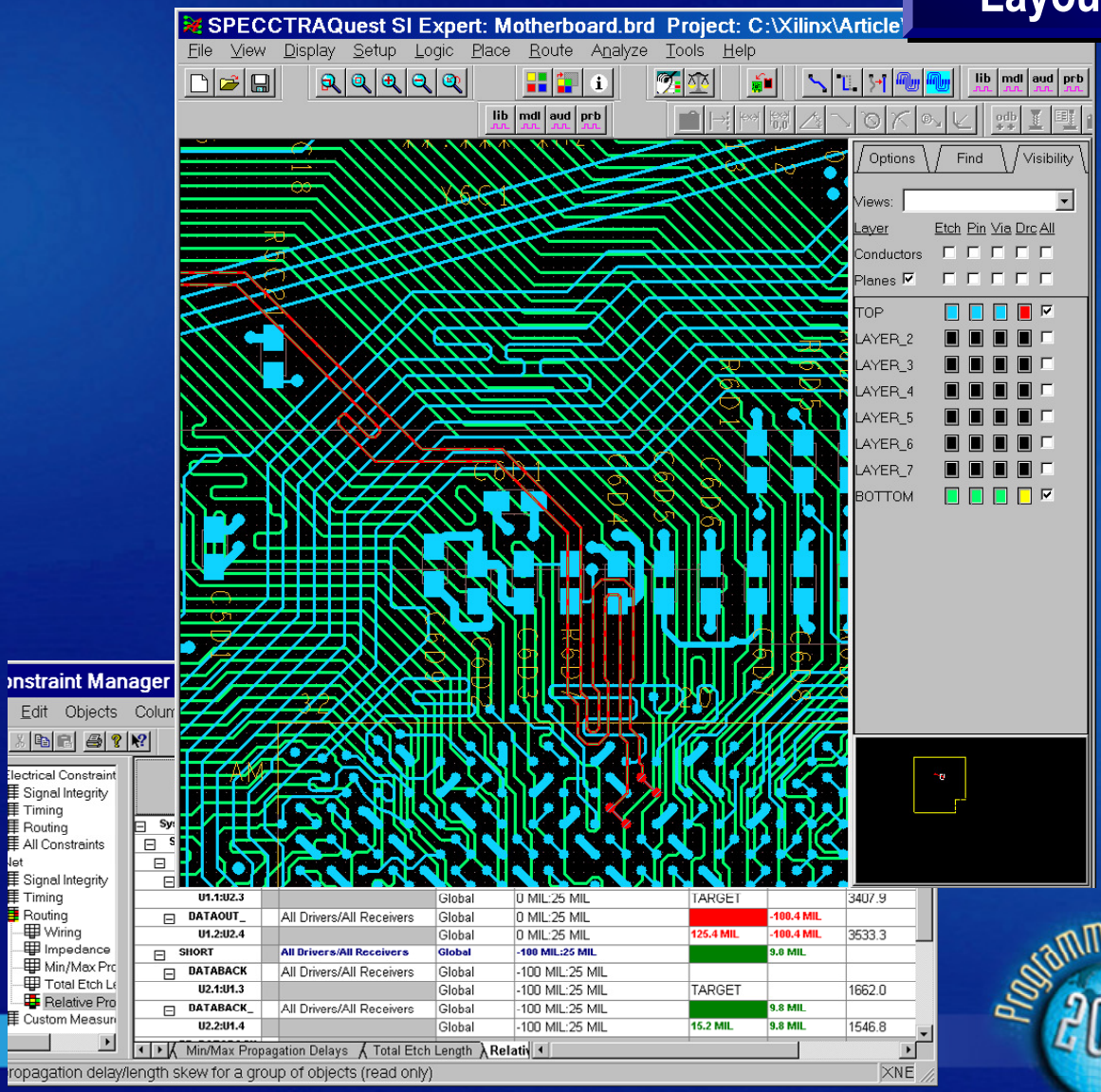
#5: PCB Layout

High-Speed PCB Layout

- High-speed constraints
  - Electrical
  - Physical
  - Timing
- Real-time margins in Constraint Manager



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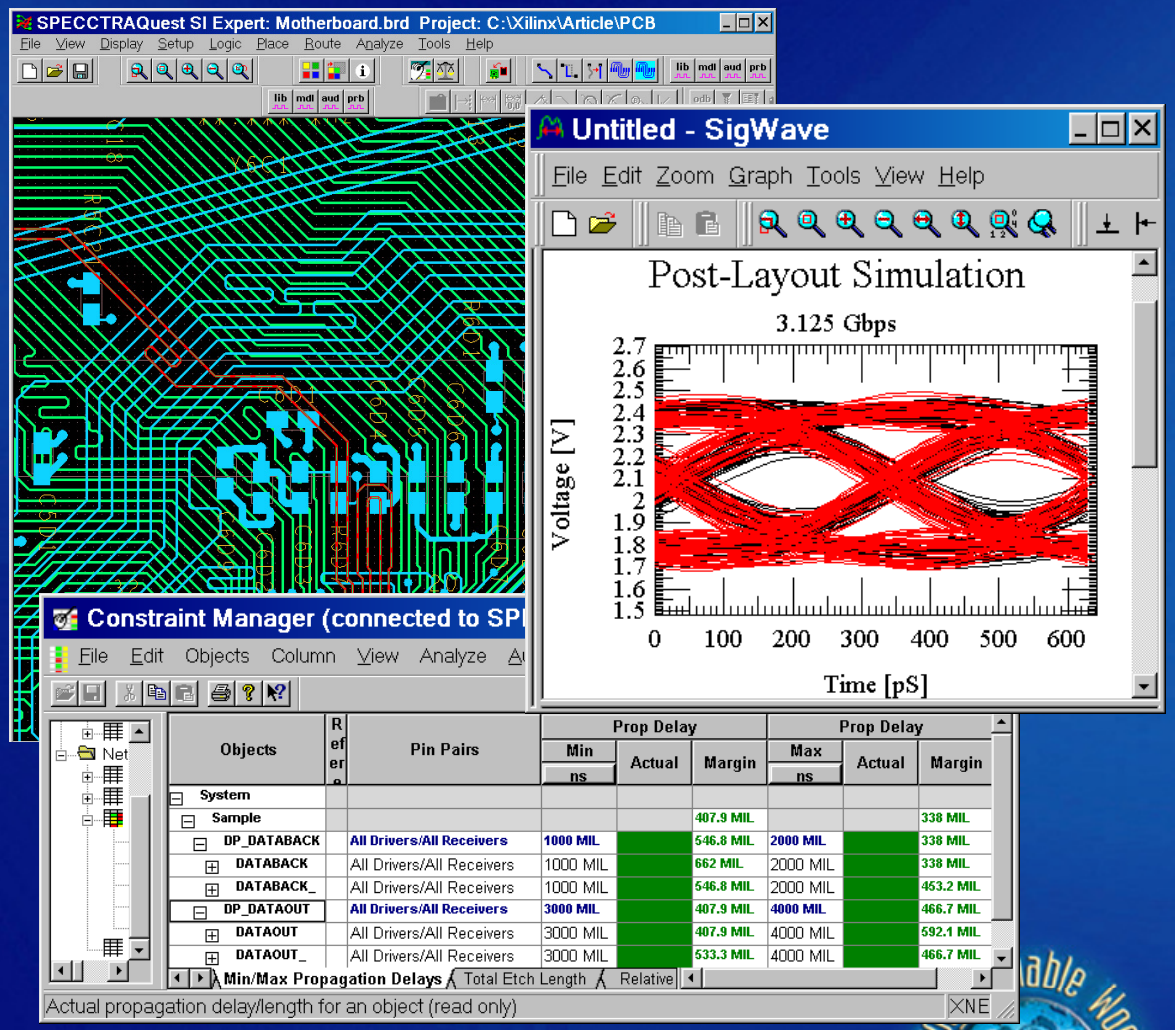
#6: Verification

Virtual Verification

- DRC Reports
- CM "Green"
- Post-Layout Simulation
  - Direct from PCB
  - Waveforms
  - Reports



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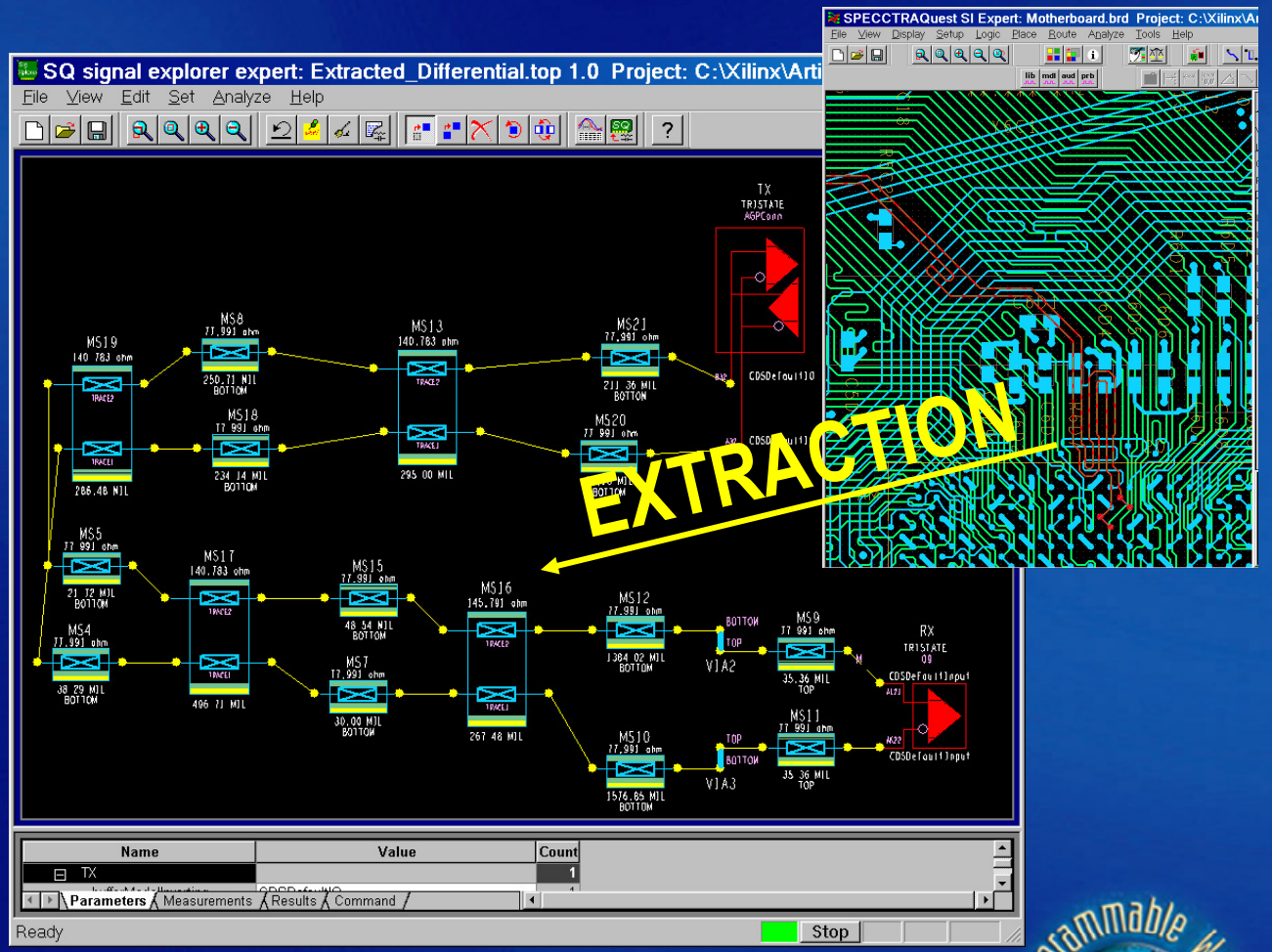
#6: Virtual Debug

Virtual Verification

1. Failure?
2. Extract differential net to electrical view
3. Examine, debug, simulate, fix



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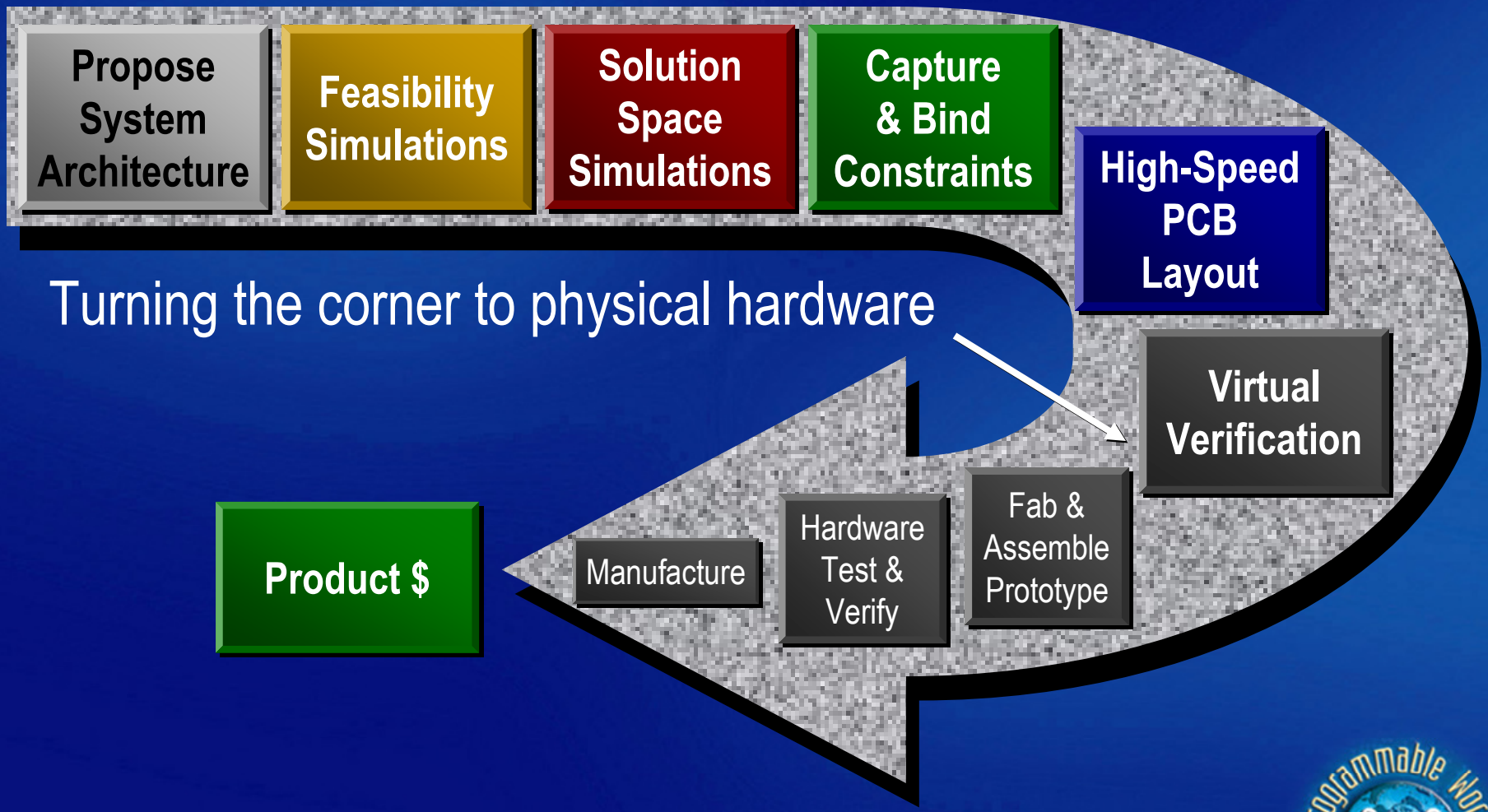
Process Review



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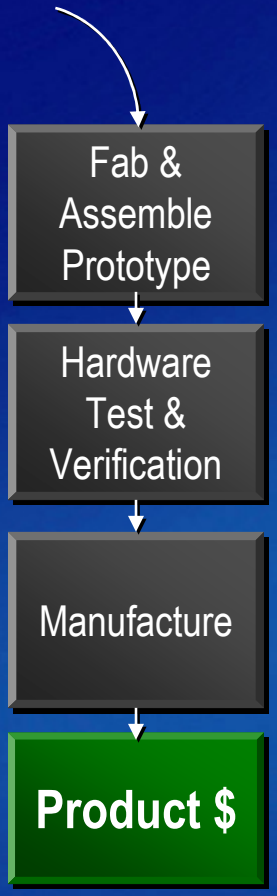
#7: Tapeout !

By using the process, simulations, and automation described, you're ready to tapeout an error-free Multi-Gigabit system design



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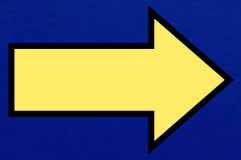

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Summary

- Multi-gigabit links are becoming mainstream
- A high-speed implementation process is needed for first-pass success
- High-speed Design Kits are available to assist
  - Xilinx Rocket I/O and Cadence SPECCTRAQuest

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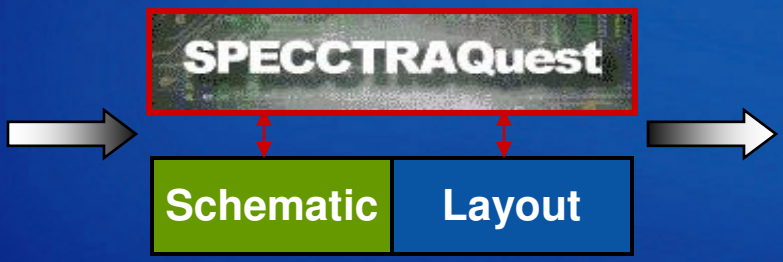
Recommended Resources

- Virtex II Pro FPGA
  - http://www.xilinx.com/virtex2pro/
- Rocket I/O
  - http://www.xilinx.com/products/virtex2pro/rocketio.htm
- Xilinx SPECCTRAQuest Design Kit
  - http://www.xilinx.com/support/software/spice/spice-request.htm
  - Click license NDA, download free Kit
  - http://www.xilinx.com/publications/xcellonline/partners/xc_speckit42.htm
- Cadence High-Speed PCB Tools
  - Visit the booth at the Conference
  - www.pcb.cadence.com
  - www.pcbhighspeed.com
  - www.specctraquest.com
  - Design Kits: http://www.specctraquest.com/Optimize/DesignKits.asp



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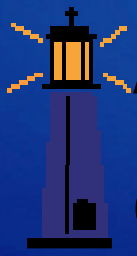
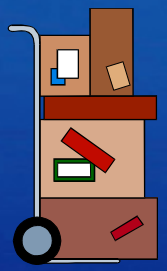
Design Kit Contents

Simulation Files
Models, Topologies, etc.



Automated
Layout Guideline
Constraint Files

Tutorial Movies



...all organized into a web-site

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