



MOVE INTO THE FAST LANE WITH GIGAHERTZ TECHNOLOGY FROM CADENCE

Understanding and Using S-Parameters for PCB Signal Integrity

Donald Telian

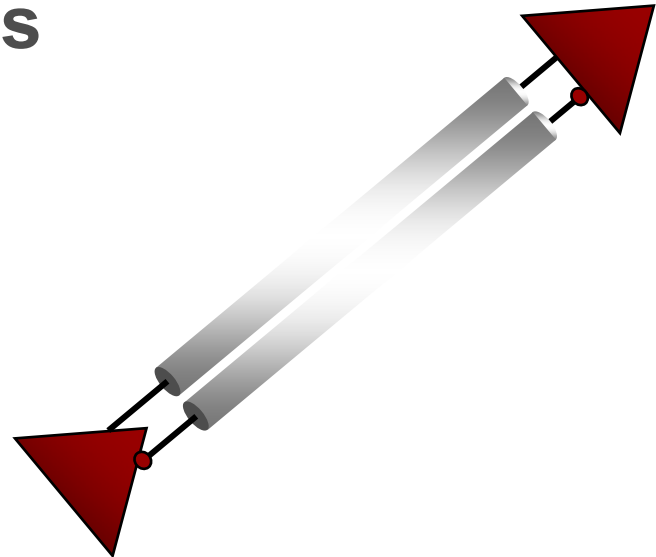
About the Author



Donald Telian has been involved in high-speed PCB design for over 19 years. At Cadence, he works with industry leaders to develop next generation tools, technologies, and "Design Kits" to support advances in technology. Prior to that, Donald worked at Intel Corporation where he founded and managed the Signal Integrity Engineering group that resolved high-speed design issues for 10 Intel Architecture desktop platforms for Pentium(R) processor-based systems. He also led the design and validation of the PCI Bus electrical specification, originated IBIS modeling, and founded the IBIS Open Forum.

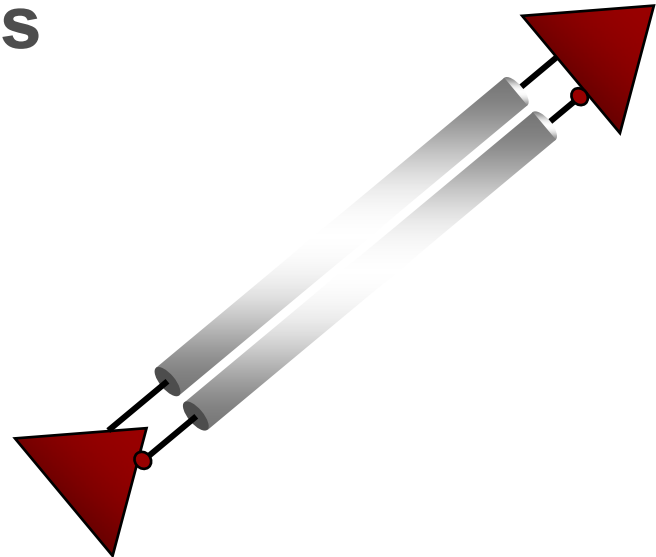
AGENDA: Understanding & Using S-Parameters

1. Introduction to S-Parameters
2. An intuitive understanding
3. Good and bad models
4. Integrated solution
5. Summary
6. Q & A

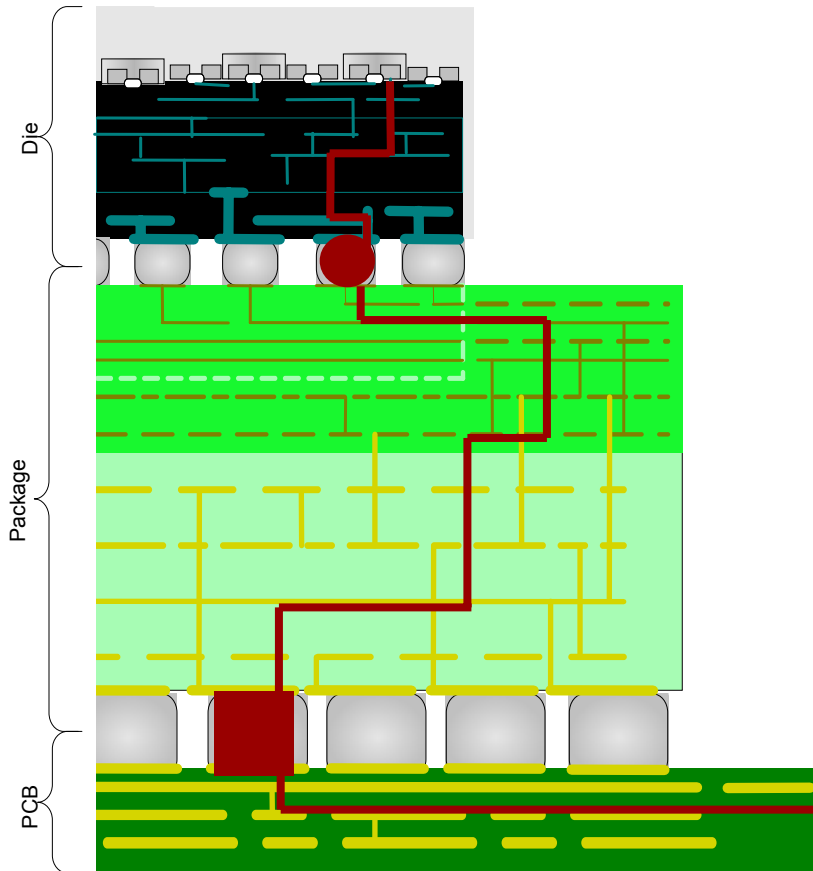


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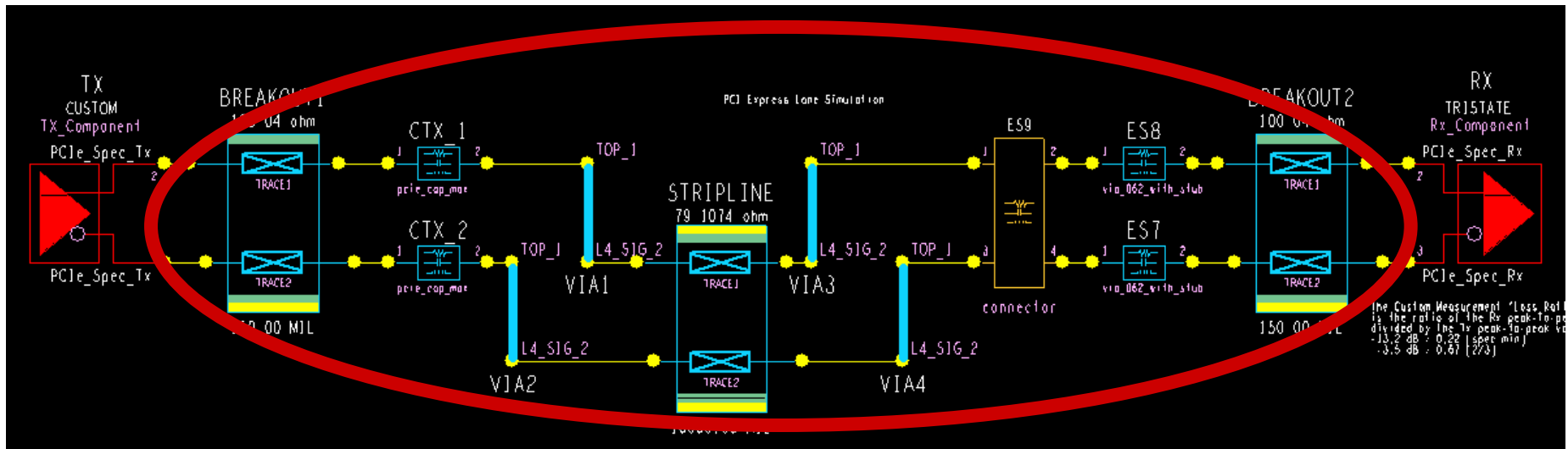
Why S-Parameters?



- Multi-GHz Interconnect behavior and discontinuities must be carefully characterized
- S-parameters have been in use for this task in RF design for many years
- They can be automatically correlated with lab measurement
- A convenient VSIC model format for co-design

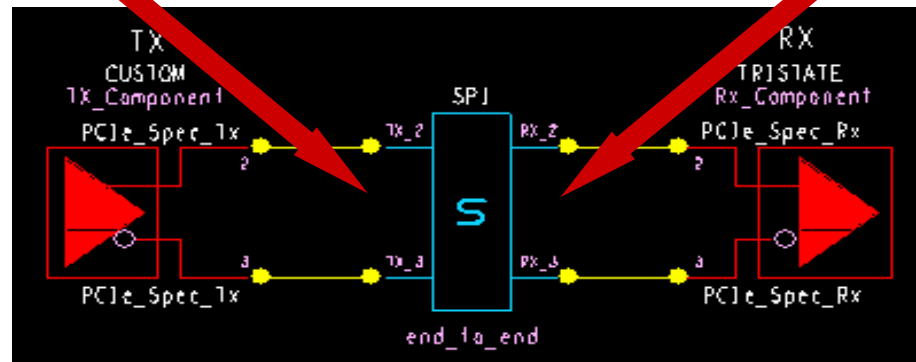
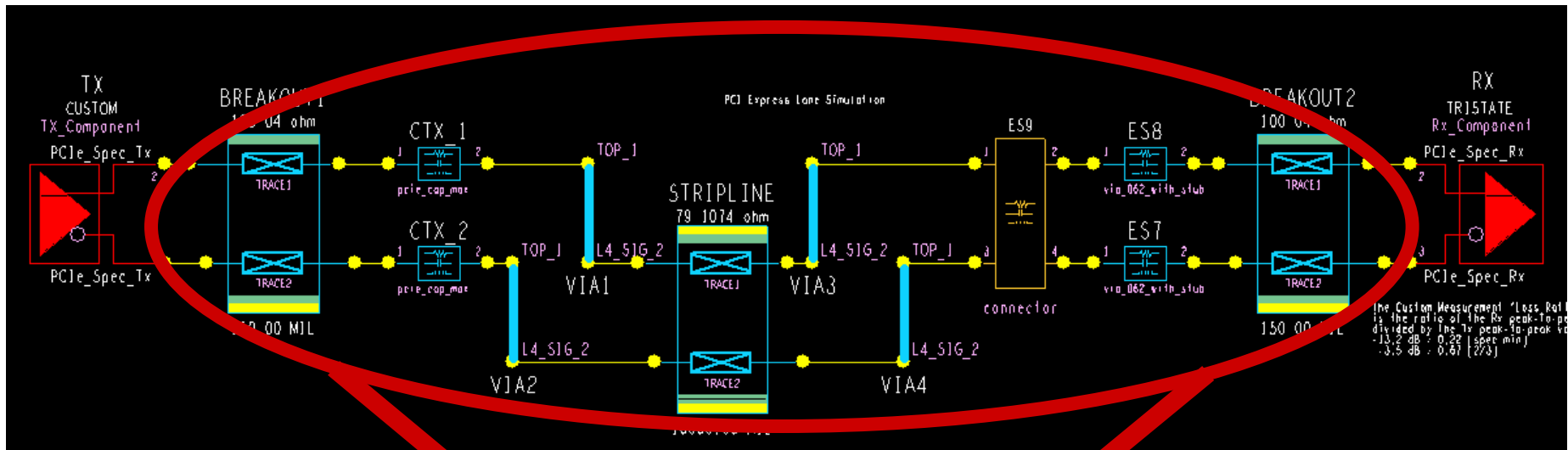
What are “S-Parameters?”

- A behavioral representation (model) of passive interconnect



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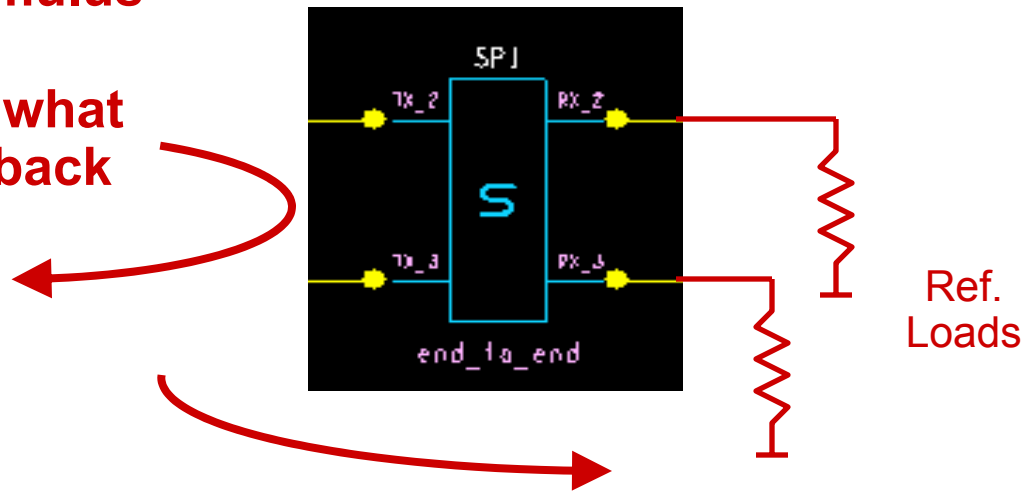
Similarly, IBIS is a behavioral representation (model) of active transistors

How is this done?

- By characterizing the interconnect into a reference load

1. Inject stimulus

2. Measure what reflects back



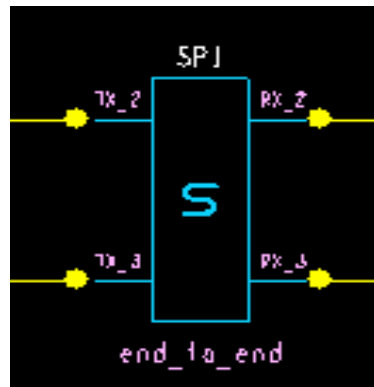
3. And combine with the measurement of what goes through

4. Into frequency-dependent S-Parameters

Similarly, IBIS data is derived by characterizing the transistors into a reference load

What can you do with the S data?

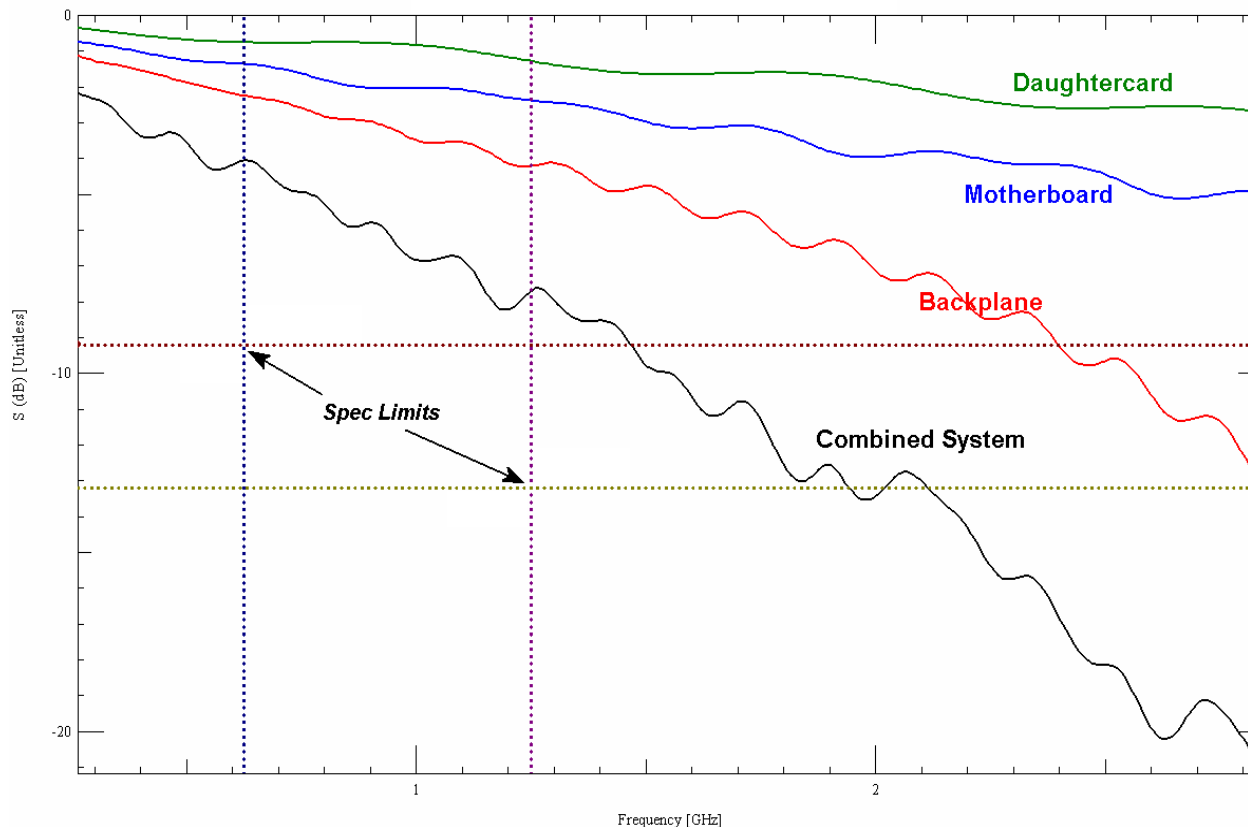
- Use it as a simplified passive interconnect model that
 - simulates faster, and
 - is easier to correlate with actual hardware, and
 - can be offered to the industry while protecting IP



*Interestingly,
IBIS models have
all the same
properties for
active devices*

What else can you do with the S data?

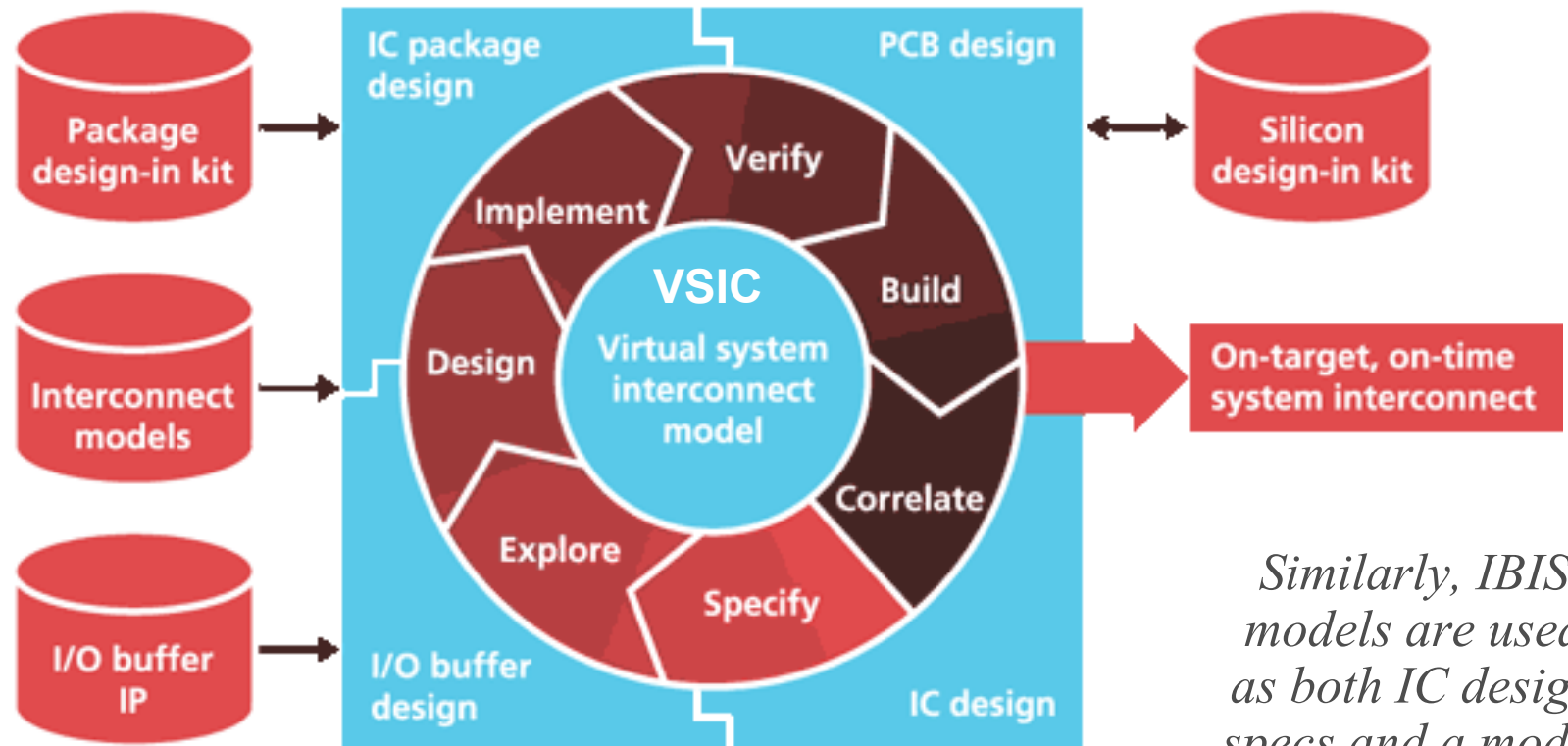
- Plot it to examine loss characteristics of the passive interconnect



Similarly, you can plot IBIS data to examine characteristics of the active devices like edge rate and drive strength

What else can you do with the S model?

- Use it as a Virtual System Interconnect (VSIC) model



Similarly, IBIS models are used as both IC design specs and a model of the IC

See: http://www.cadence.com/whitepapers/allegro_platform_wp.pdf

AGENDA: Understanding & Using S-Parameters

1. Introduction to S-Parameters

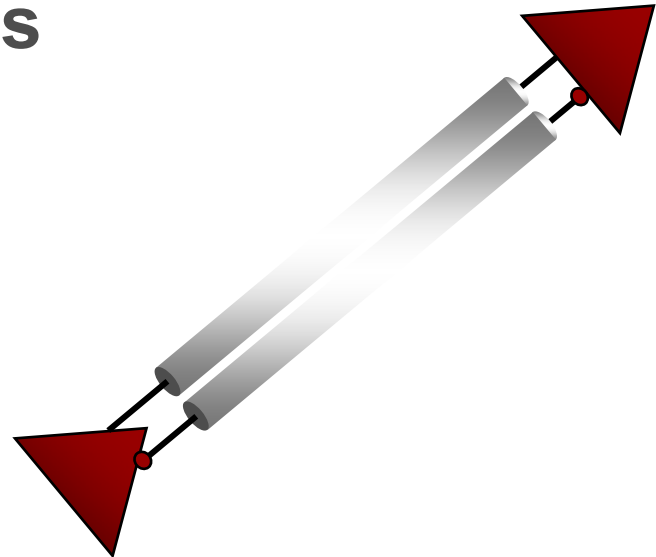
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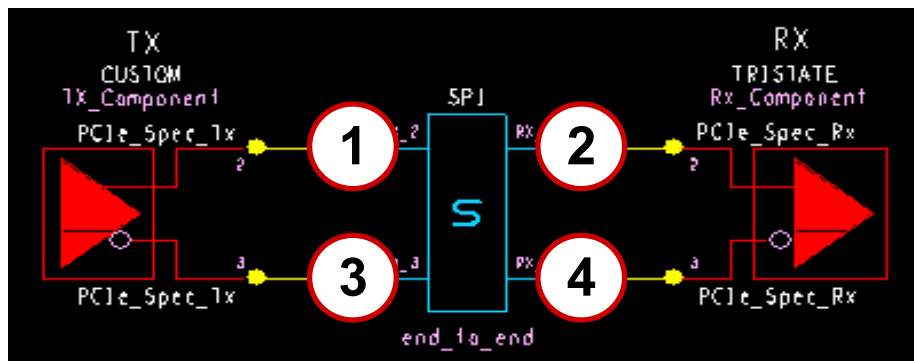
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Common S-Parameter Terminology



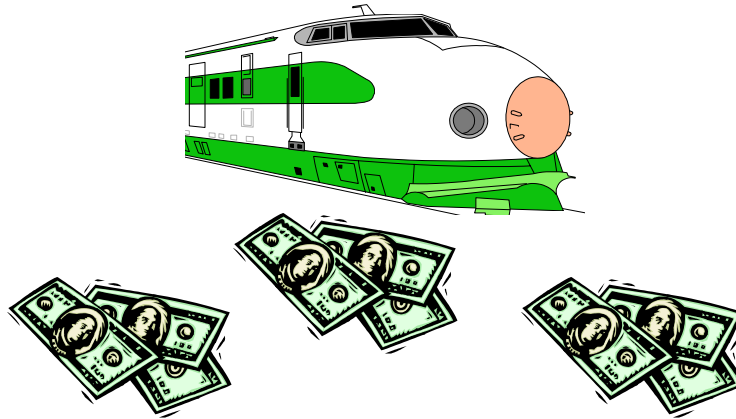
- On differential nets, nodes are typically numbered as shown
- “ S_{21} ” is what appears at (2) when stimulus is applied at (1)
- As such, for stimulus applied at (1) if you look at:
 - (1) = S_{11} = Reflection (often called “return loss”)
 - (2) = S_{21} = Transmission Loss (sometimes called “insertion loss”)
 - (3) = S_{31} = Near-end Crosstalk
 - (4) = S_{41} = Far-end Crosstalk

What is “Loss”?

- Loss is a measure of how much you lost



San Francisco



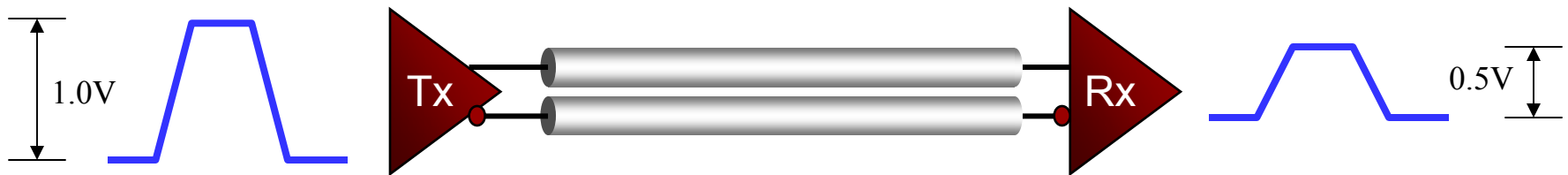
Los Angeles

For example:

1. You are in San Francisco with \$ 100.00
2. You take a bumpy train ride to Los Angeles
3. You arrive in Los Angeles with \$ 50.00

You experienced “loss” and your wallet is now $20 \cdot \log(50.00/100.00) = 6 \text{ dB}$ down

Now in Multi-GHz Terms



For example:

1. A Tx injects a 1.0V 2.5 Gbps PCIe differential signal into a PCIe link
2. The signal travels through the interconnect to the Rx
3. A 0.5V signal is measured at the Rx pins

The Tx signal experienced “loss” and is now $20\log(0.5/1) = 6$ dB down at the Rx

The deciBel

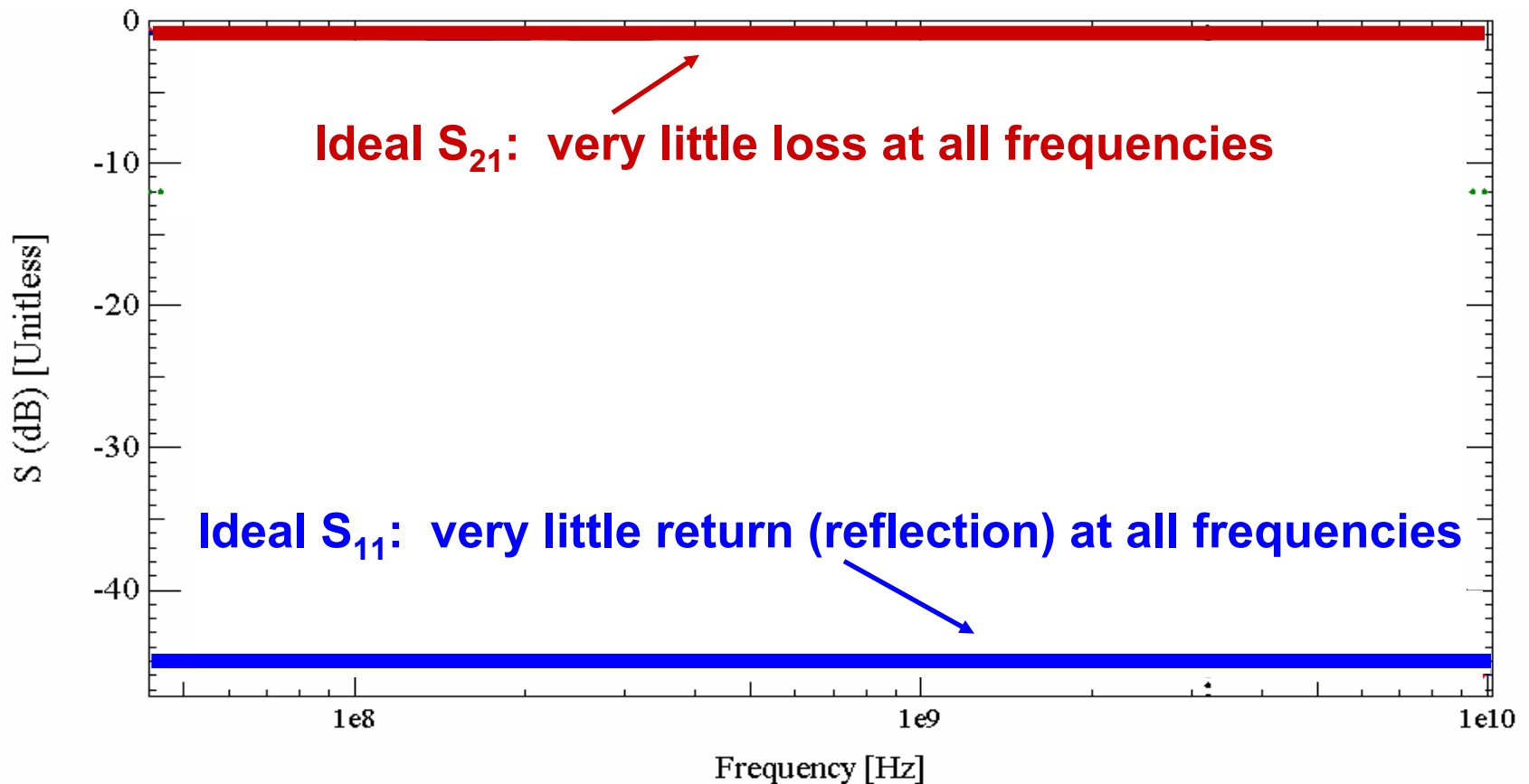
$$\text{dB} = 20 * \log_{10}(V_{\text{out}} / V_{\text{in}})$$

- The magnitude of an S_{ij} term is typically expressed in dB
- Interestingly: $20 * \log_{10}(V_{\text{out}} / V_{\text{in}}) = - 20 * \log_{10}(V_{\text{in}} / V_{\text{out}})$
- Examples:

Vin	Vout	dB
1	0.70	- 3
1	0.50	- 6
1	0.25	-12

A specification that allowed $V_{TX}(\text{min})$ of 1.0V and a $V_{RX}(\text{min})$ of 0.25V might specify an interconnect “loss budget” of 12 dB

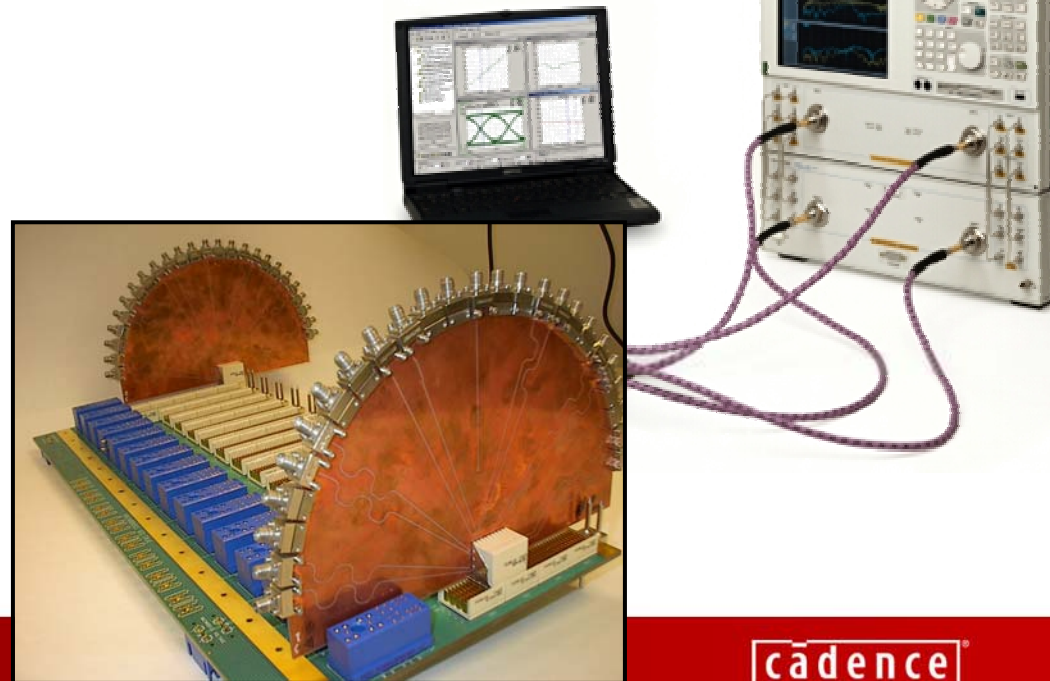
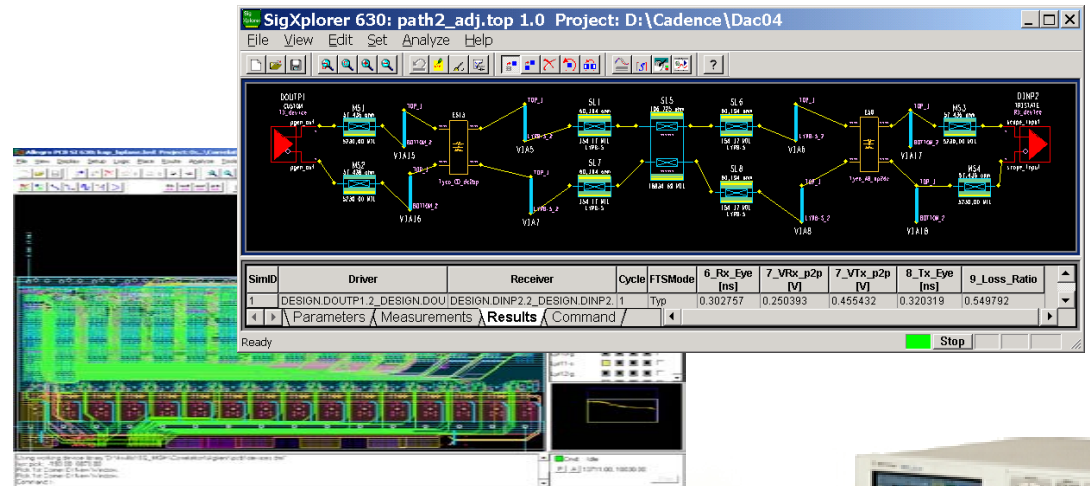
Ideal (yet unrealistic) Characteristics



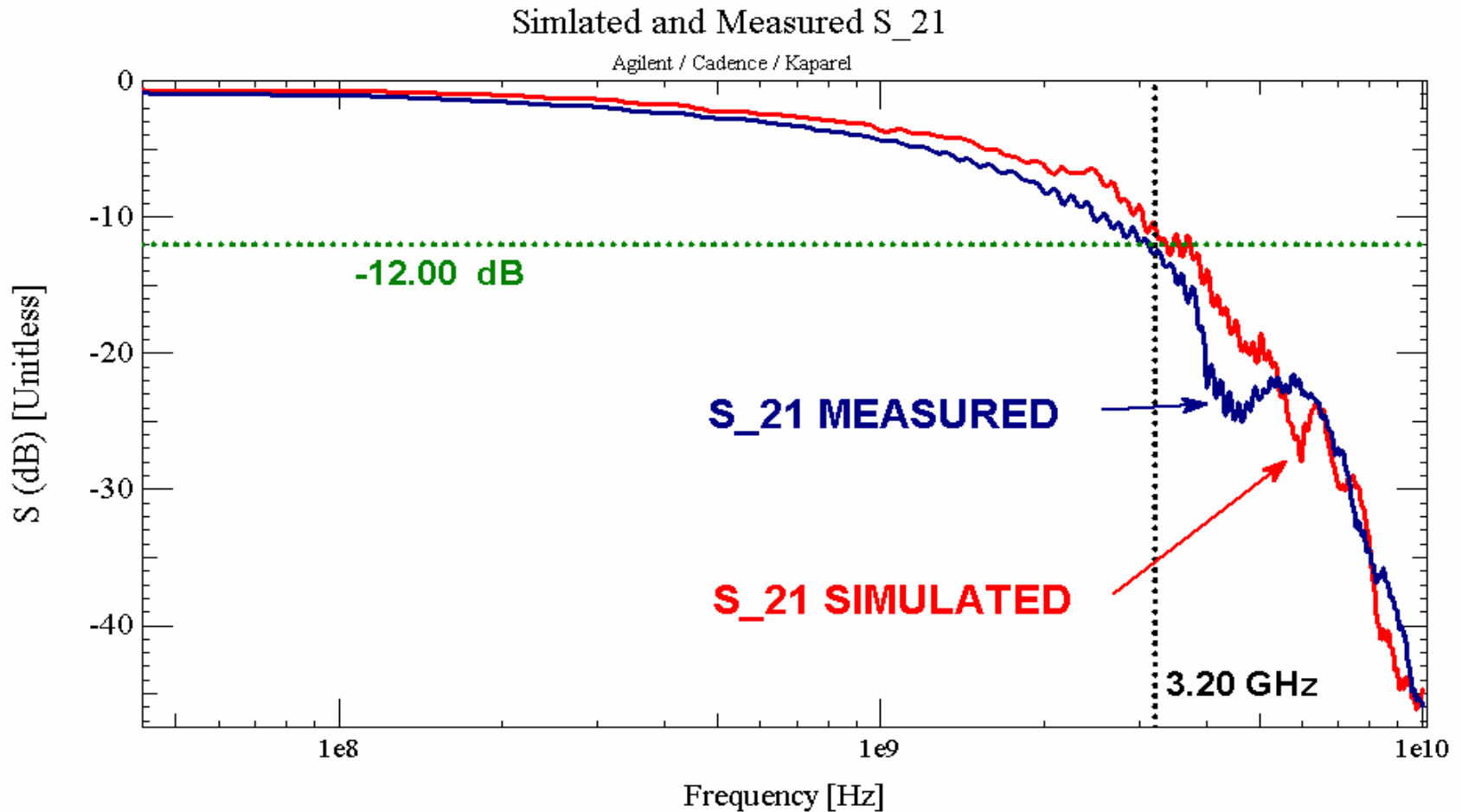
- Remember:
 - S_{21} describes the end-to-end transmission
 - S_{11} describes what reflects back based on what you put in

S-Parameter PCB SI Characteristics Example

- Kaparel Backplane
 - www.kaparel.com
- Agilent Measurement Equipment and paddle cards
 - www.agilent.com
- Cadence Allegro PCB SI 630
 - www.cadence.com
- Note: S-Parameters can be generated from both design tools and measurement equip.

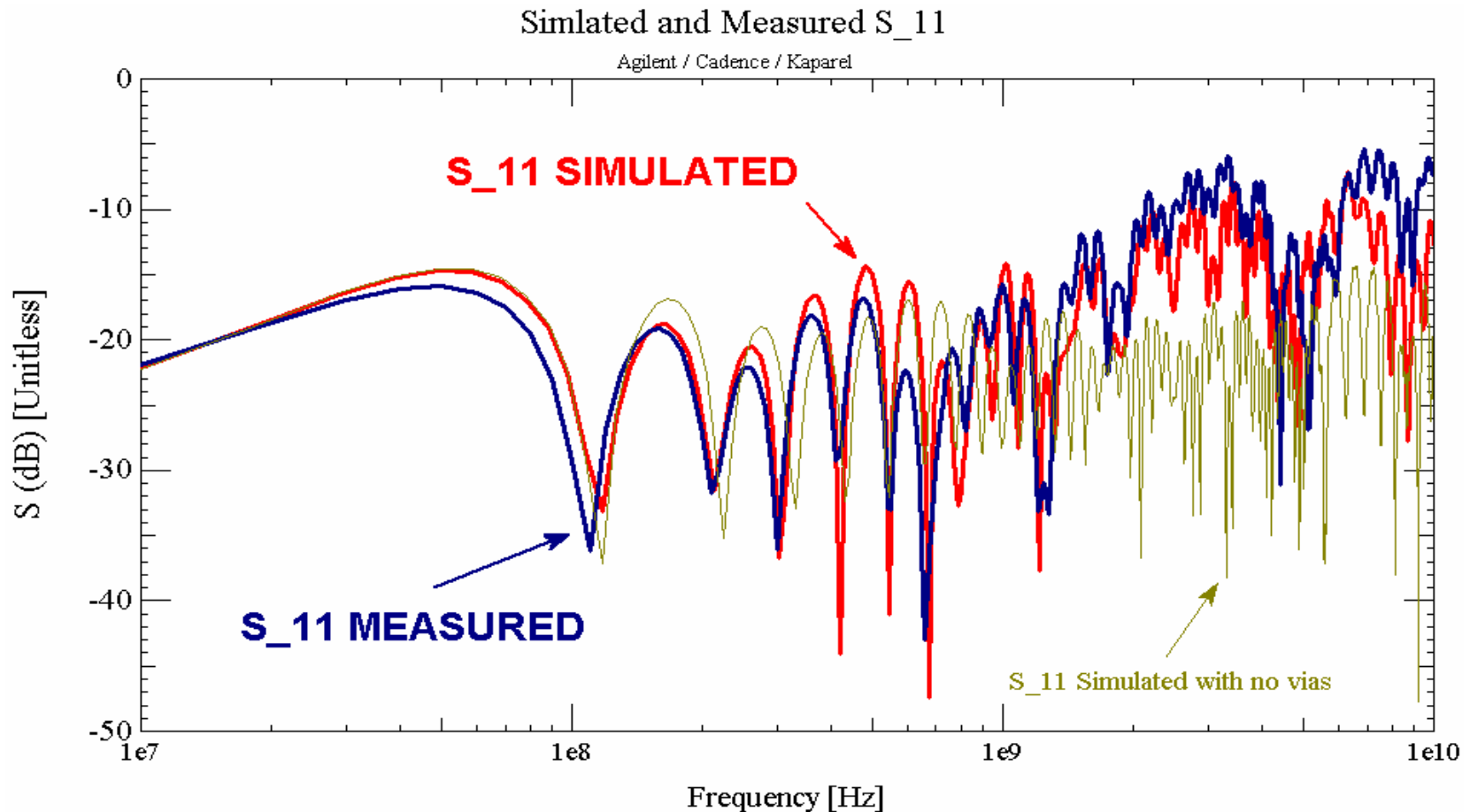


Transmission Loss (S_{21})



- A 3.2 GHz Tx signal would likely be at 25% (-12 dB) at the Rx
- Ideal Transmission Loss would be a flat line at ~0 dB

Reflection (Return) Loss (S_{11})

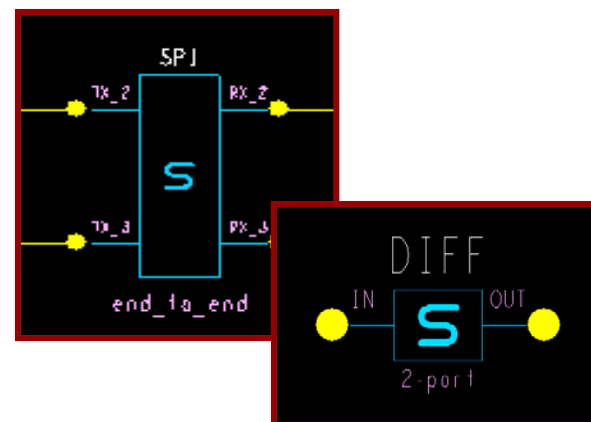
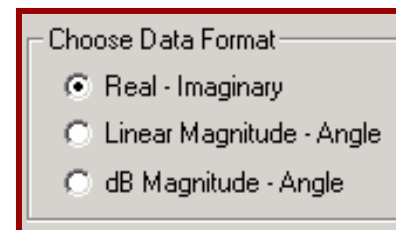


- More signal is reflected as freq increases, flatter with no vias
- Ideal (yet unrealistic) Return Loss would be a flat line at -50 dB

Looking Deeper

- A complete S-parameter behavioral interconnect model is actually a matrix of all S_{ij} data at numerous frequency points
- As such, S_{ij} also denotes that parameter's place in the matrix
- All S_{ij} values are complex numbers
 - So far, we have primarily looked at magnitude
- Be aware that there are also “Differential S-Parameters” where the nodes are referenced to each other instead of ground
 - In that case, the 4-node diff-pair becomes only 2 ports
 - A good subject for another time

S_{11}	S_{12}	S_{13}	S_{14}
S_{21}	S_{22}	S_{23}	S_{24}
S_{31}	S_{32}	S_{33}	S_{34}
S_{41}	S_{42}	S_{43}	S_{44}



AGENDA: Understanding & Using S-Parameters

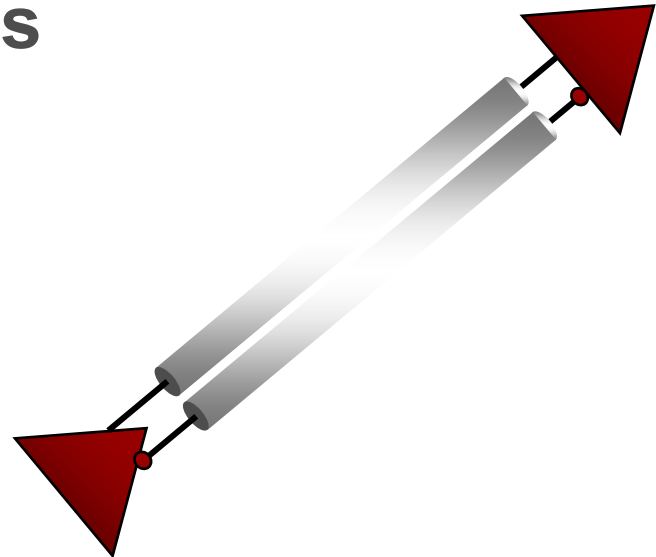
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Good & Bad S-Parameter Models

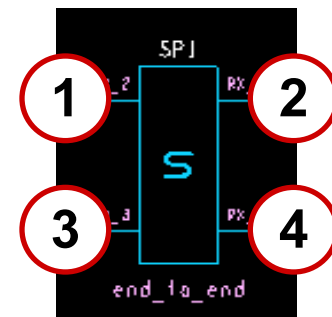
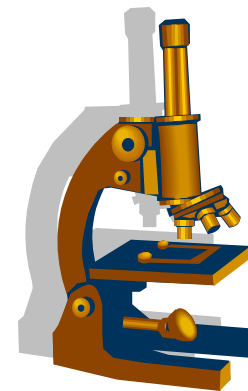
- Just as with IBIS, initially there may be a high percentage of bad models due to:
 - Incorrect measurement techniques
 - Incorrect or unavailable node definitions
 - Insufficient data to allow correct DC solution
 - Insufficient number of frequency points
 - Too many frequency points
 - Frequency range too narrow
 - Data is not passive



These problems can occur in both measured and extracted models

Common Problems

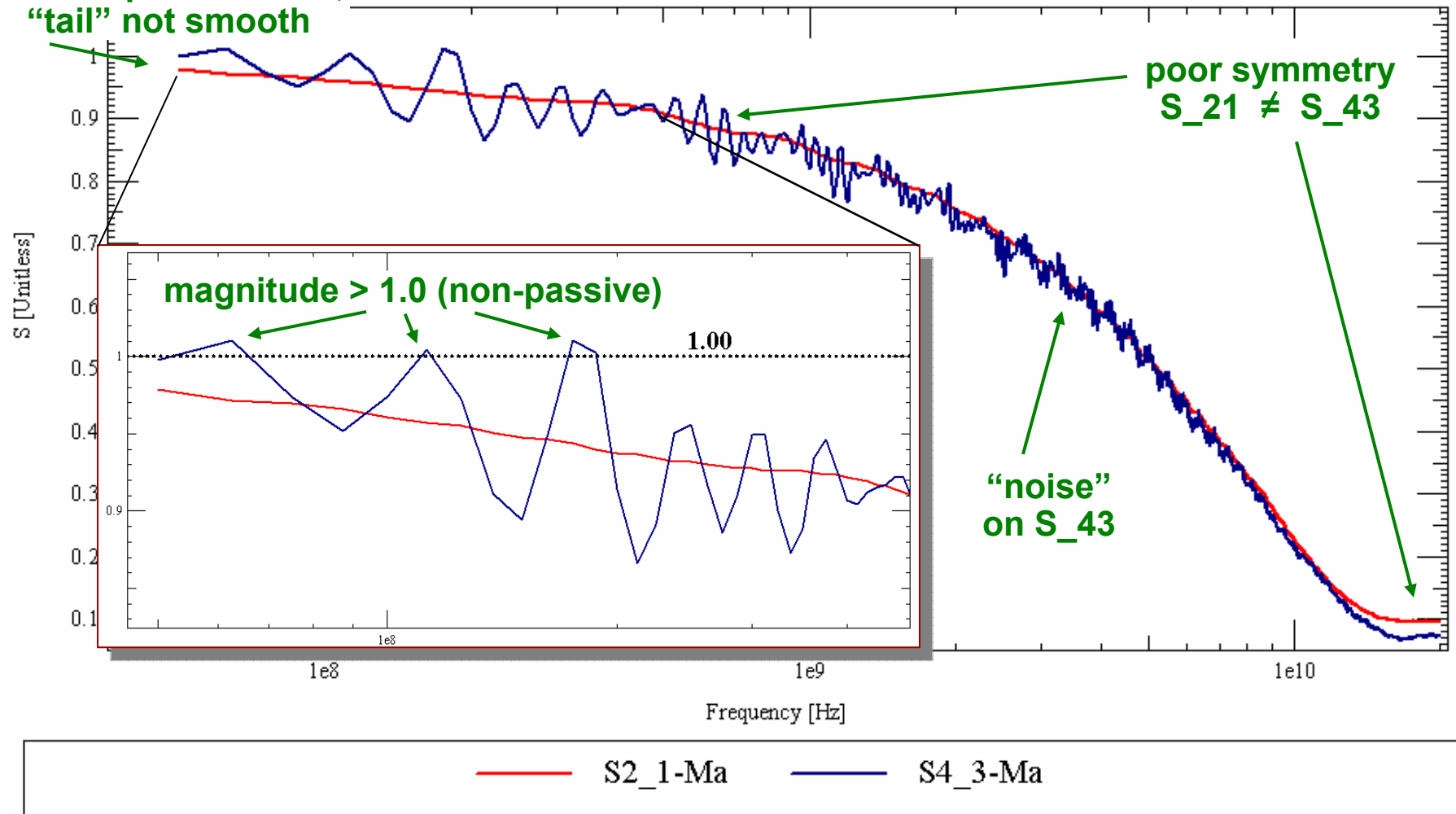
- Differential-pair models should be symmetric
 - $S_{21} = S_{43}$, $S_{11} = S_{33}$, $S_{41} = S_{23}$, and so on
 - Plot/overlay the magnitudes and zoom in to verify
- Data must be passive
 - Plot the magnitude on a linear Y axis
 - Confirm that no value is greater than 1.0
 - Would imply amplification (non-passive)
- Confirm adequate frequency range
 - End points should be “smooth” for extrapolation



Problematic S-Parameters Example

data stops at 50 MHz, "tail" not smooth

Incorrect S-Parameter Data for a Differential Net



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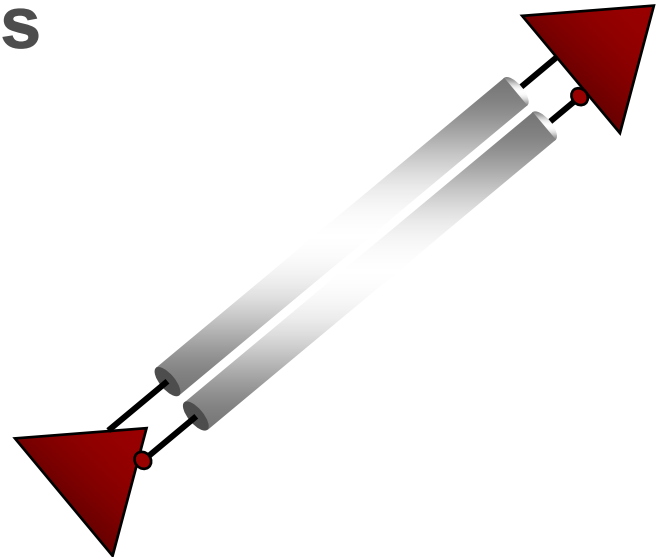
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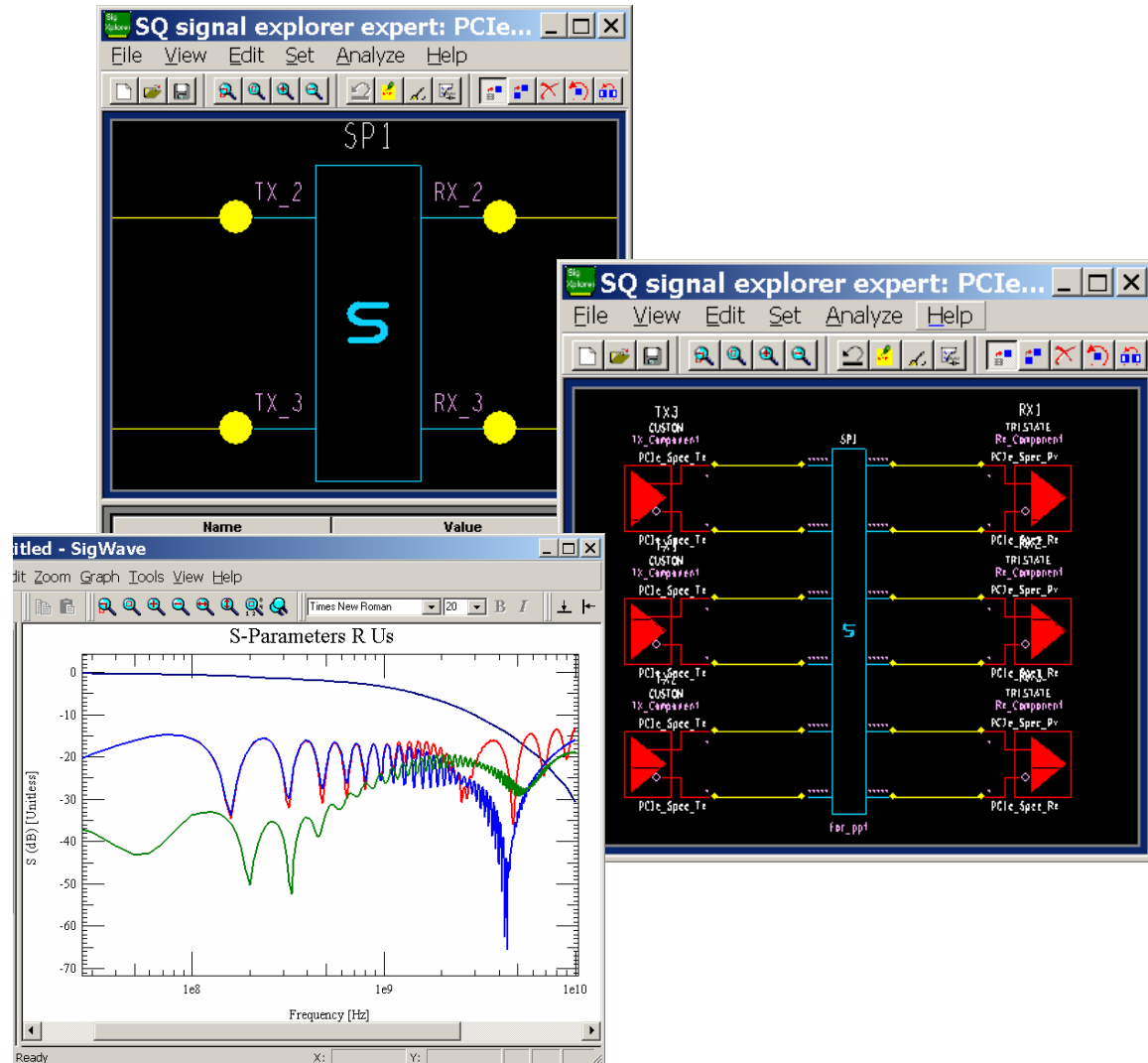
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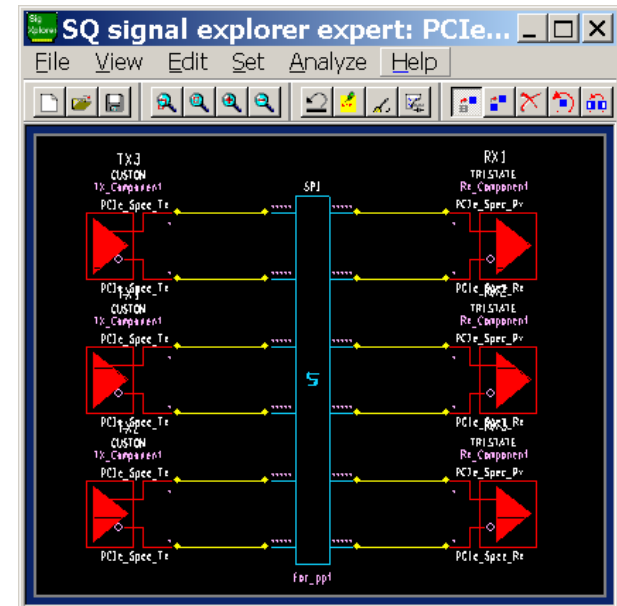
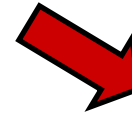
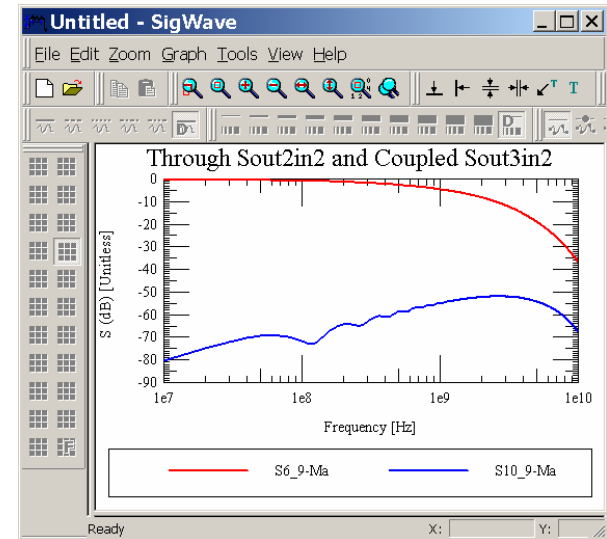
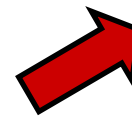
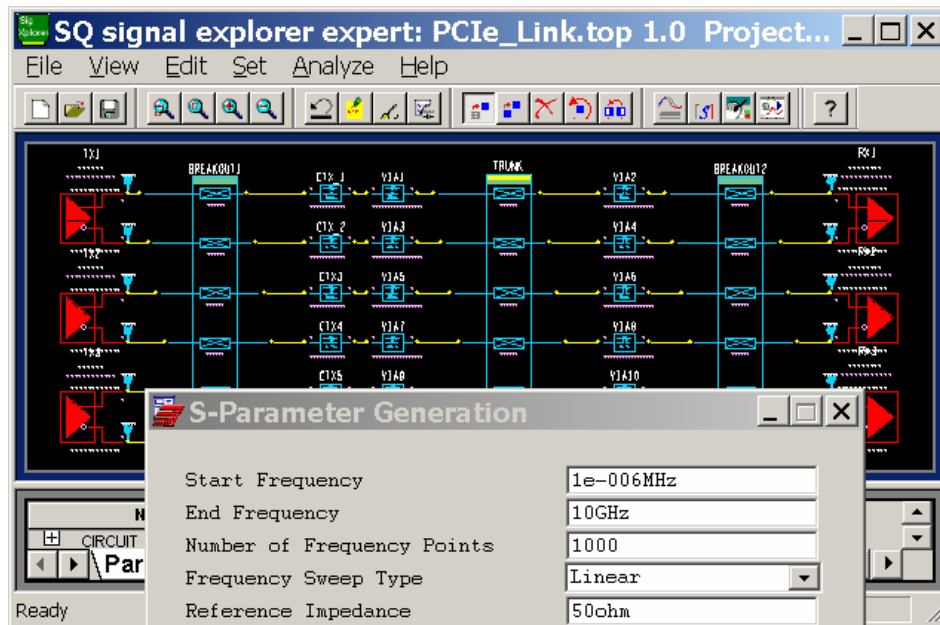
Allegro PCB SI 630 S-Parameter Solution

- Generation
- Simulation
- Plotting
- Measurement Import
- Correlation
- Library Mgmt

...a complete solution!

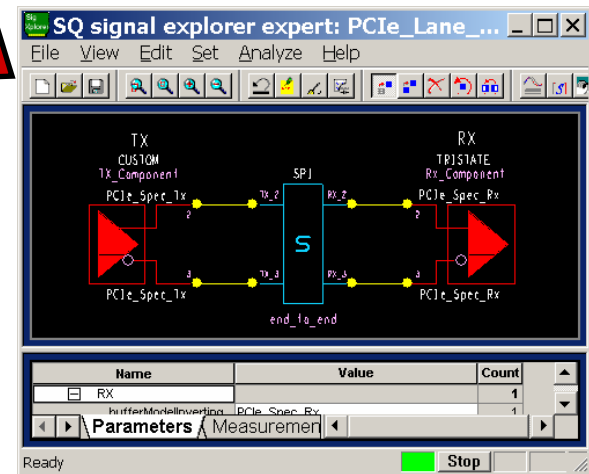
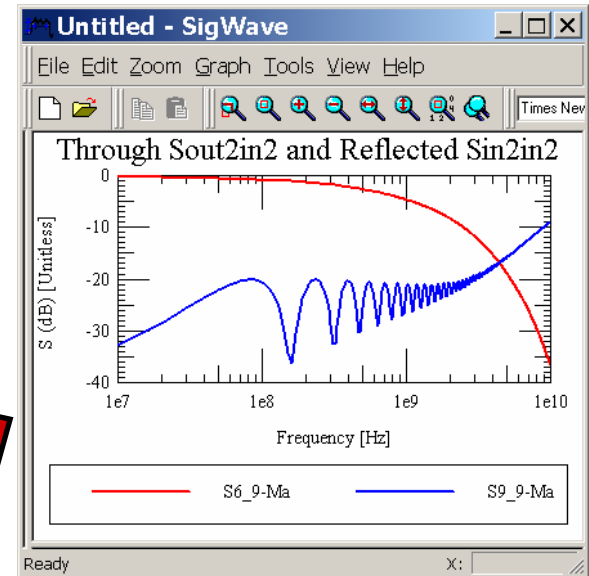
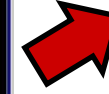
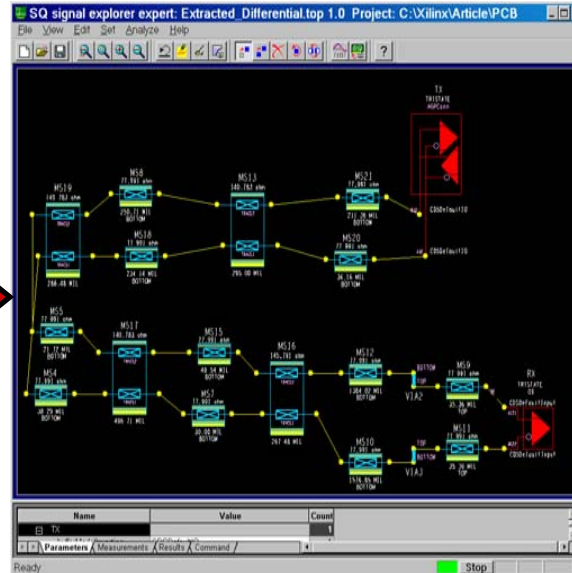
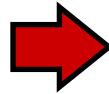
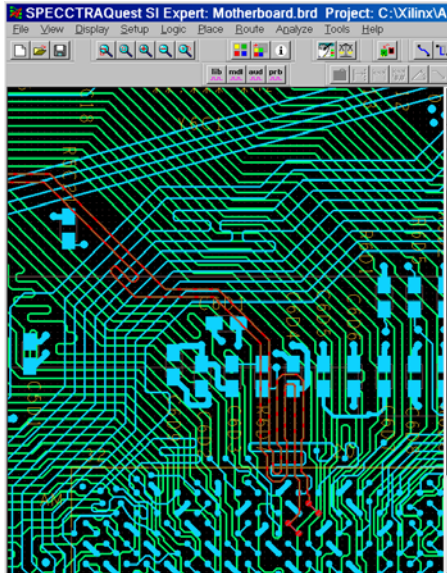


S-Parameter Generation (from Drawing)



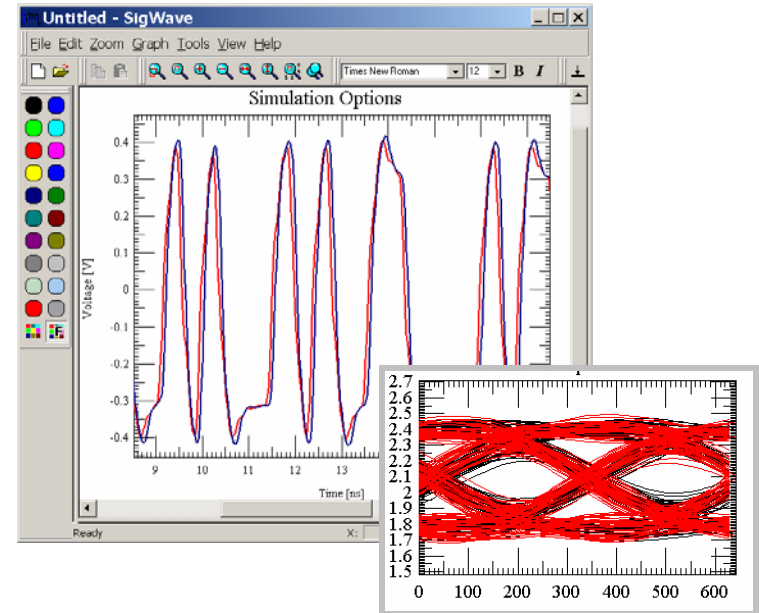
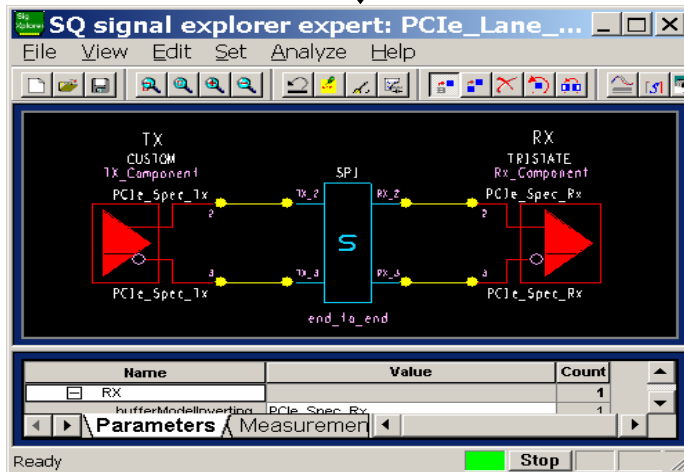
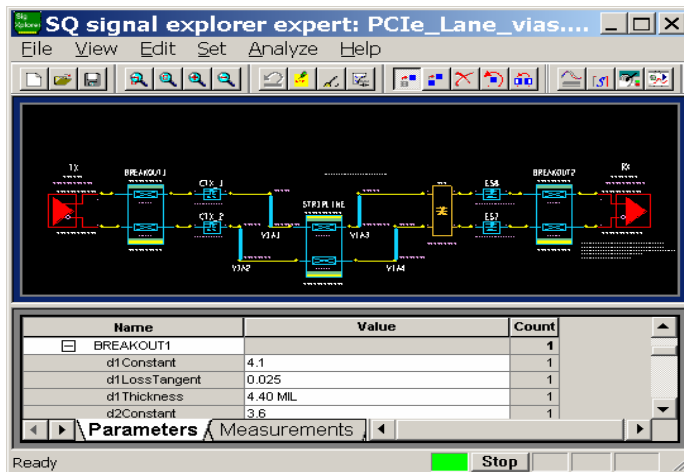
- Any portion (or all) of passive interconnect in any SigXp drawing
- Plot S_{ij} from arbitrary nodes (ports) to view the interconnect behavior over frequency
- Collapse interconnect into s-parameter model

S-Parameter Generation (from Layout)



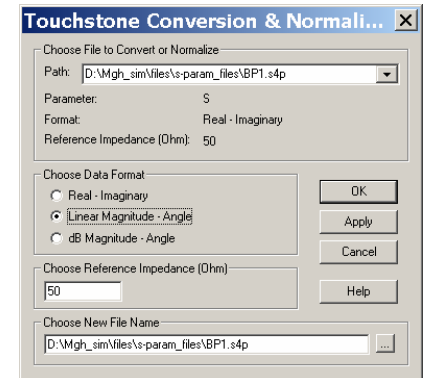
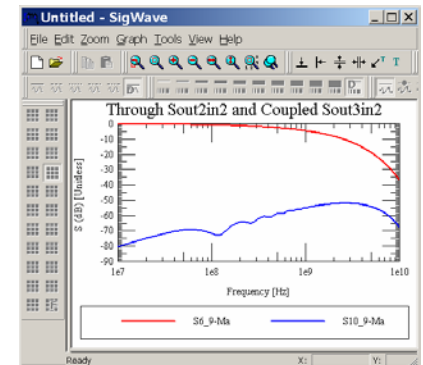
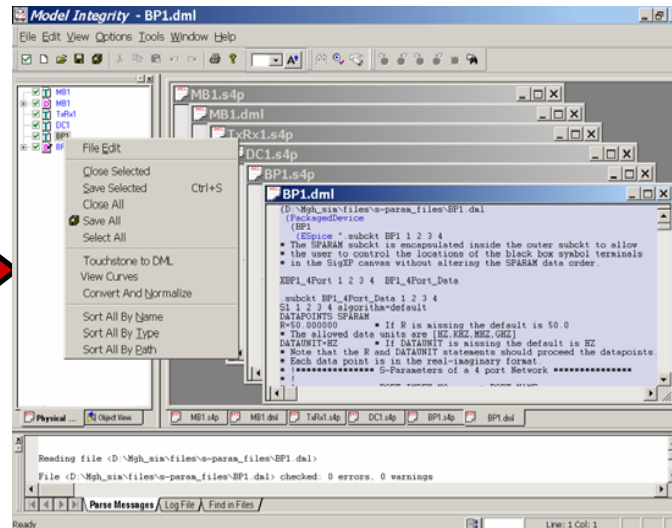
- Extract any single-ended or differential net from PCB
- Generate and/or plot S-parameter characteristics of all or portion

S-Parameter Simulation

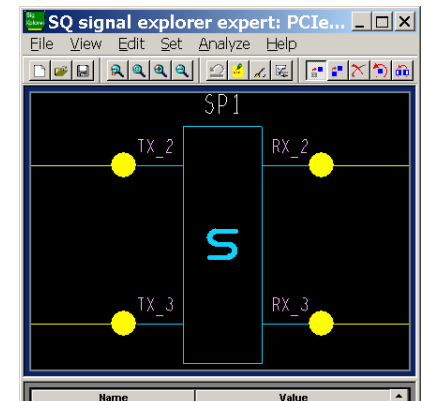


- TD simulation of S-parameters
- Various algorithms deployed

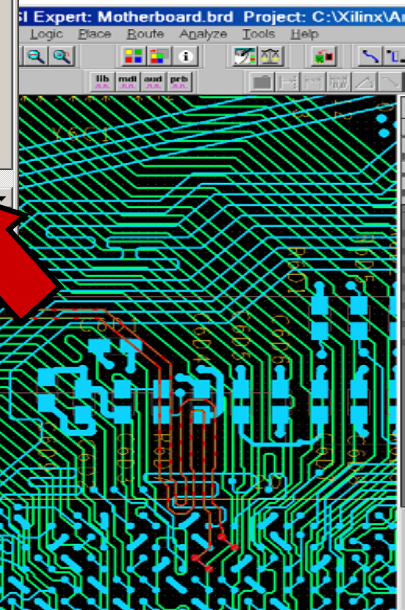
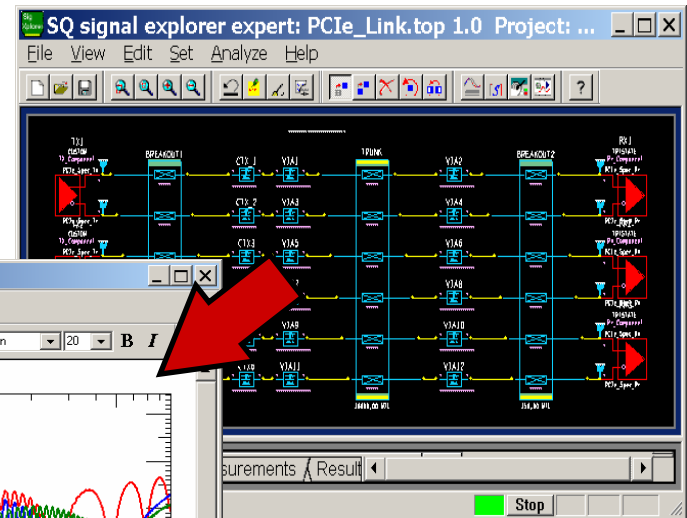
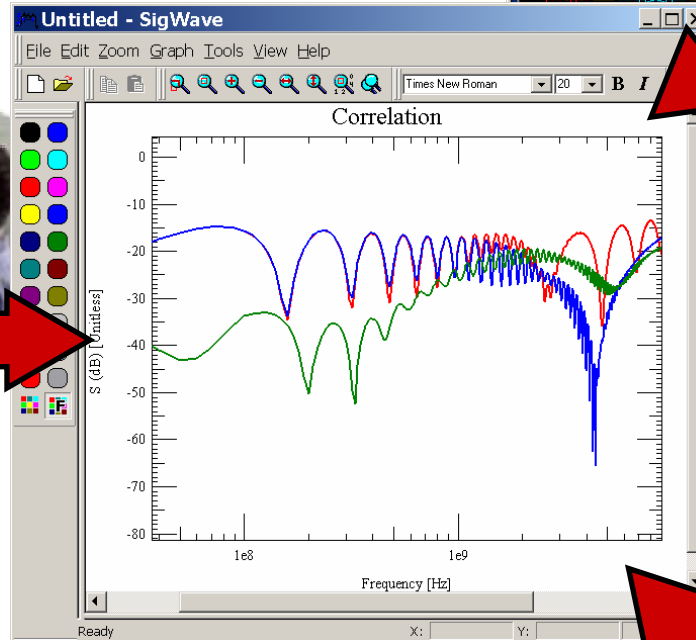
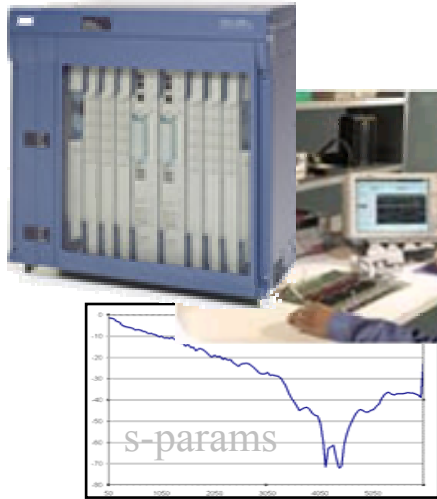
Import from Measurement



- Read Touchstone into Model Integrity
- Plot curves with single right-click
- Convert / normalize complex numbers
- Dump to model (translate to DML)



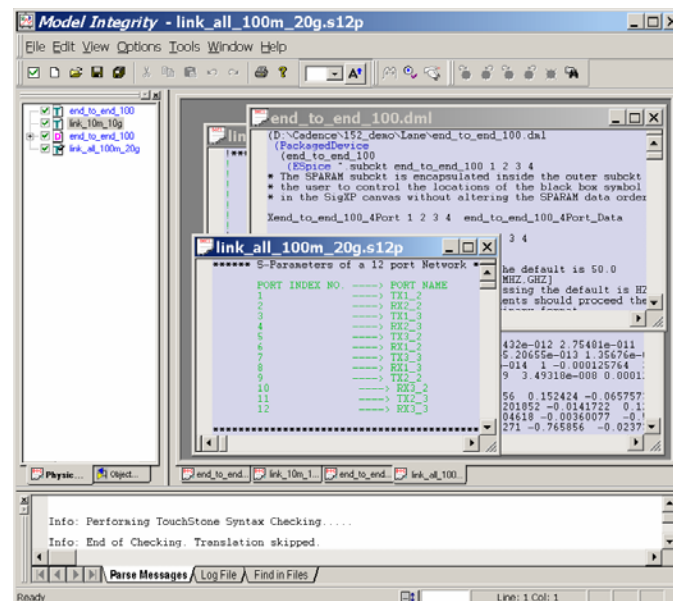
Correlation



- Correlate, overlay, compare S-Parameters from any source
- Measurement, PCB, drawing

Library Management

- Generated models added to working library
- Auto-replace and save of interconnect option
- Touchstone format (.s*p) automatically saved
- Port to node mapping logs and comments
- Bidirectional Touchstone translation
- Plot, translate, edit options
- Reference impedances
- Passivity checks



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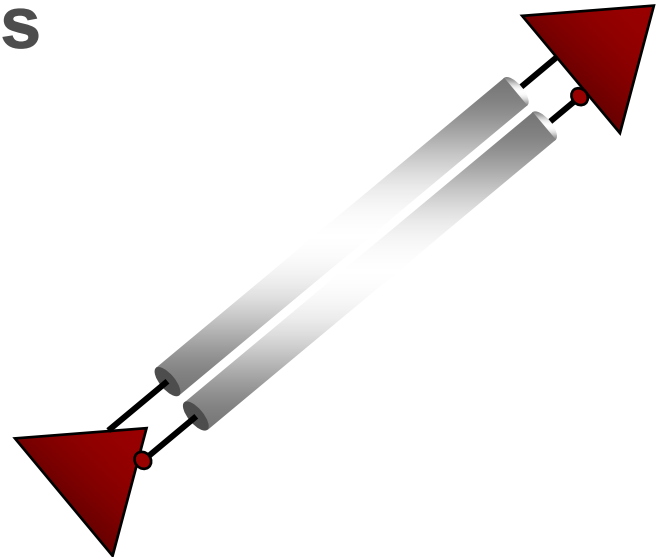
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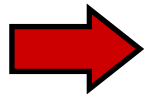
Summary

- S-Parameters are being used increasingly for Multi-GHz (MGH) PCB signal integrity
- The S-Parameters are being used to model and characterize the passive interconnect (much like IBIS represents the active devices)
- A basic understanding of S-Parameter data/models will be required
- Cadence is now offering an integrated PCB SI solution that includes complete S-Parameter support in Allegro PCB SI 630

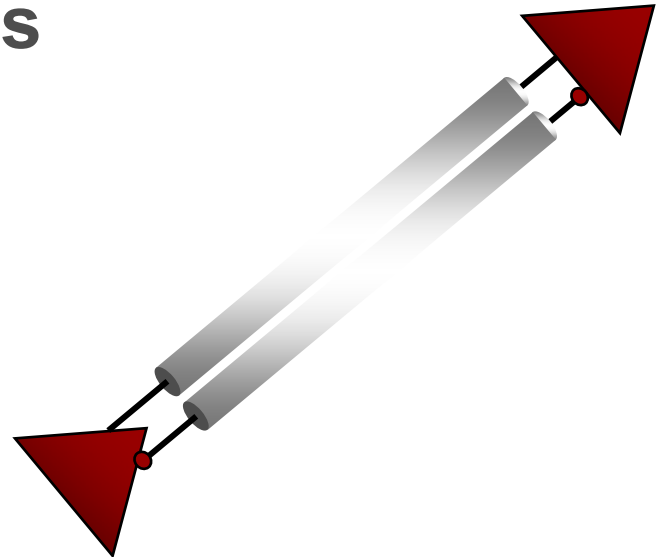


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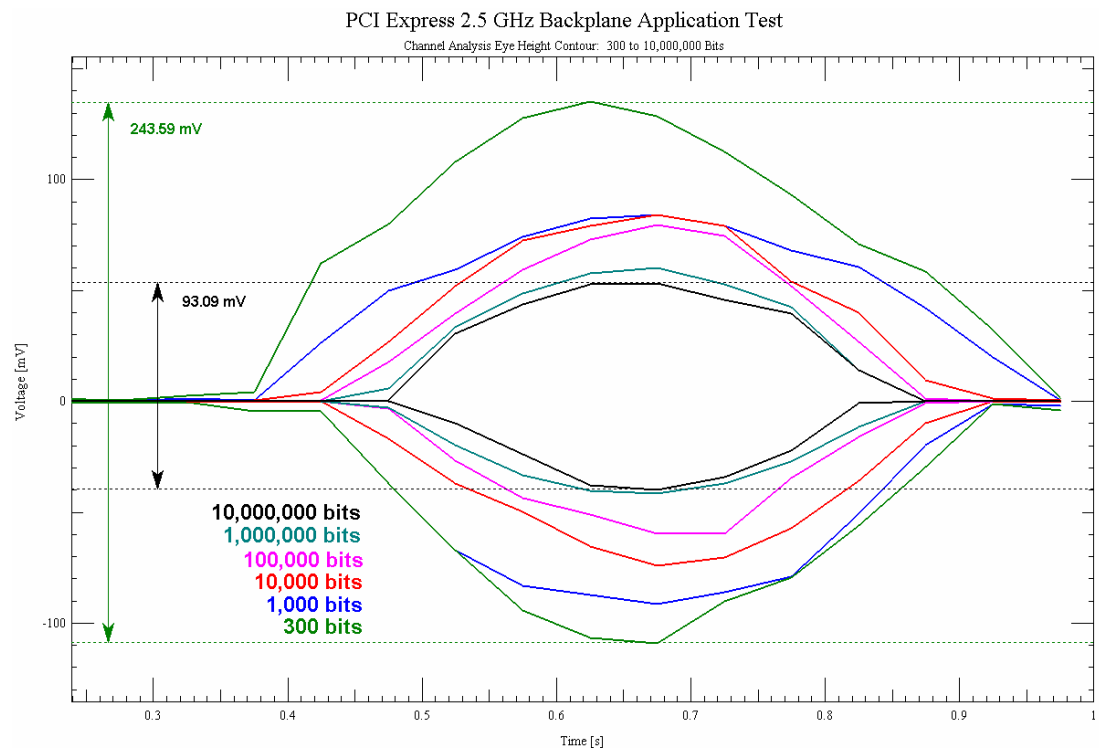


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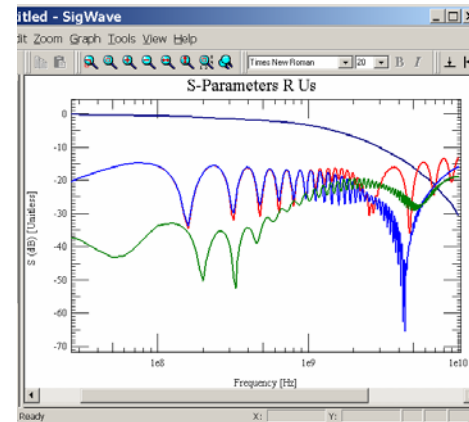
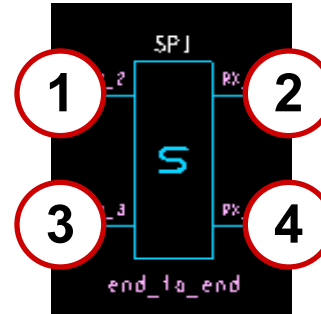
Next in the series:

- “Fast Multi-GHz PCB Interconnect Simulation”
 - New revolutionary technology
 - Simulate 10,000 bits in seconds
- July 21, 10:00 am PDT
- Watch for email invitation



Q & A

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$



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