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## New Techniques for Designing and Analyzing Multi-GigaHertz Serial Links

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## Abstract

Deficiencies in pre-hardware characterization of Multi-GigaHertz (MGH) serial links have caused a temporary return to hardware prototypes and testboards. Accurate MGH channel modeling is a challenge and, even if achieved, very CPU-intensive using current techniques. This paper details new concepts and technologies that enable a more thorough analysis of MGH serial links. Interconnect Storage Potential (ISP) is explained as a key to understanding the predictability of signal transmission, and the type of analysis required to arrive at an accurate eye diagram. The new methodology is illustrated using relevant serial interconnects such as PCI Express\* and Serial ATA\*.

## Author's Biographies

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Donald Telian has been involved in high-speed PCB design for 20 years. As a Cadence Technologist, he works with industry leaders to develop next generation tools and design methodologies. Prior to that, Donald worked at Intel Corporation where he founded and managed the Signal Integrity Engineering group that resolved high-speed design issues for 10 generations of Intel Architecture computers. He also led the design and validation of the PCI Bus electrical specification, and originated IBIS modeling and the IBIS Open Forum.

Kevin Q. Chung is an Applications Engineer for PCB and Packaging products at Cadence Design Systems. He is responsible for providing high speed methodology solutions to Cadence customers and specializes in advanced modeling and signal integrity simulation. Prior to joining Cadence, he worked at Megatest/Teradyne for eight years designing high performance analog and digital circuitry. He also worked at Juniper Networks as an SI Engineer for the T320 and T640 Core Routers. Kevin received a B.S.E.E degree from the University of California, Davis in 1990.

### **1. Introduction**

As the highest-speed digital interfaces turn serial and differential, new opportunities are created for design tools and techniques. Embedded Multi-GigaHertz (MGH) clocks define the data they are extracted from, and eye diagrams quantify successful transmission at the electrical level. To overcome losses in existing PCB materials and structures, clever pre-emphasis and equalization schemes are finding their way into a new breed of ICs. Engineers continue to wade through this dynamic environment which has been rich in discoveries.

One discontinuity that has occurred involves the efficacy of current simulation tools when applied to MGH serial data transmission. Since an eye diagram is built by superimposing multiple events rather than accurately characterizing a single event (e.g. the setup and hold relationship of two signals), more simulation must naturally be done. But the question arises: "How much more?" This is the question we will attempt to answer in this paper.

Figure 1.1 shows how the inner contour of an eye diagram becomes smaller as more bits are simulated. This concept is not foreign, since we are used to watching eye diagrams on oscilloscopes set to "infinite persistence" continue to narrow as time proceeds. The figure shows how different the eye opening is found to be when simulating 300 bits or 10 million bits (only 4 ms of data), and points in between. It's startling to observe how much the answer can be wrong, which in this case is 260%.



Figure 1.1: Eye Opening versus Number of Bits Simulated

Admittedly, the simulation of such a large bit stream using current techniques is almost inconceivable. Typical SPICE simulation for this type of interface time-steps through nodal equations and requires about 1 hour for every 100 bits. At that rate, the simulation of 10 million bits would require approximately 11 years to complete. This is obviously not an acceptable solution.

And yet, some serial links do not exhibit the behavior shown in Figure 1. In fact, in some links there may be little or no difference in eye opening between 100 bits or 10,000 bits. Why are some links more problematic than others? How can you determine how many bits to simulate? The answer to these questions can be found by examining each unique Interconnect Storage Potential, or "ISP".

## 2. Interconnect Storage Potential (ISP)

All interconnects will store bits long enough to transmit them to the other end. This is an important attribute since in a typical serial interconnect, the bit width is much shorter than the time required to transmit it down the link. For example, at 2.5 Gbps each bit is 400 ps wide while the time to transmit it down a 24-inch link is about 4 ns. Consequently, each bit is injected into the interconnect 10 bit times before it is seen at the other end.

In the ideal case, when each bit arrives at the receiver it finds a perfect termination and the energy from that bit is removed from the system. However, real systems do not operate this way. Instead, the realities of manufacturing low-cost modular systems introduce a variety of imperfections.

Figure 2.1 shows a typical differential serial link, or "channel". The transmitter (Tx) at left launches a bit into the interconnect that travels to the receiver (Rx) at the right. Discontinuities in the interconnect - such as vias, connectors, and trace impedance mismatches – cause some amount of energy to reflect back to the Tx. As the remaining energy arrives at the Rx it finds a (typically embedded) termination with tolerances that may or may not match well with the rest of the interconnect, causing additional energy to reflect back to the Tx. Since each bit's energy is not removed from the system, it will cause a disturbance to the signal integrity of the bits that follow. This phenomenon is sometimes referred to as Inter-Symbol Interference, or "ISI".



Figure 2.1: Imperfections in a physical serial link

The imperfections in real-world serial implementations give each interconnect a unique potential to store energy and have more or less ISI. This capacity can be quantified and is what we refer to as Interconnect Storage Potential, or "ISP". And, as will be shown, the ISP is directly related to the number of bits required for an eye opening to converge on its actual height and width.

The following sections detail a methodology for determining and using the ISP to design and analyze a serial link following these steps:

1) Determine the ISP

2) Determine the Relevant Preamble

- 3) Calculate the Number of Bits
- 4) Perform High-Capacity Simulation

#### **2.1 Determine the ISP**

The four steps to determine an ISP through pre-hardware simulation are as follows:

1) Model. Build an accurate model of the system that includes the relevant effects for the given frequency. This may include connectors, coupled vias, crosstalk from neighbor channels, and so on. Remember, it's the effects of the imperfections we want to capture.

2) Pulse. Use the Tx to inject a single pulse into the system. The pulse width is not critical, yet should be one bit time or narrower. Simulate the pulse with 10-20 leading zeroes to stabilize the system, and 80-100 trailing zeroes.

3) Plot. Plot the waveform at the Tx. From this plot, there are two possible ways to arrive at an ISP. (1) Measure the time from the trailing edge of the pulse to the time when the signal has decreased to less than 5% of the pulse's peak-to-peak voltage. This rule-of-thumb approach is illustrated in Figure 2.2. (2) Alternatively you can calculate a tolerance, in milliVolts, that would be acceptable in your final eye diagram result and measure the time from the trailing edge to the point where the waveform stays under that limit. This technique is based on superposition principles, and is illustrated in section 5. Given the plot in Figure 2.2, it is likely that both techniques would yield the same measurement for this particular waveform. Note also that while it may be effective to measure the same quantity at the Rx, this may yield a smaller and incorrect value. Overall, the Tx is the best measurement point since any perturbation seen there will be superimposed on future bits.

4) Measure. The time measured in step 3) is the ISP. If the data rate is known, you may want to round this up to the nearest multiple of the bit interval. In Figure 2.2, the ISP is found to be 9.6 ns.



Figure 2.2: Plotting and Measuring to Determine an ISP

#### **2.2 Determine the Relevant Preamble**

For any bit transmitted there are previous bits in the system that will affect its signal integrity. We refer to the quantity of previous bits that affect the current bit as its relevant "preamble". To adequately characterize an MGH serial link, we need to comprehend the potential preamble variations.

Recalling that the ISP measures the interval of time in which significant energy remains in the system, we calculate that relevant preamble as:

(1) preamble = 
$$ISP / bit_time$$

A 2.5 Gbps system with an ISP of 9.6 ns would have a (9.6 ns/400 ps =) 24 bit preamble. That means that various permutations of the 24 previous bits will affect the eye height and width of the present bit. Assuming the channel is a linear time-invariant (LTI) system, bit variations occurring before the preamble will have no effects.

#### 2.3 Calculate the Number of Bits

Once the preamble size is known, a system that allows the transmission of any combination of bits would require the following number of bits to be simulated:

(2) # bits = (preamble)\*(2 <sup>preamble</sup>)

Substituting equation (1) into equation (2) we find that the number of bits is exponentially related to the ISP and the data rate in Gbps in the following equation:

(3) 
$$\#$$
 bits = (ISP / bit time)\*(2 (ISP / bit\_time)) = (ISP\*Gbps)\*(2 (ISP\*Gbps))

Using the final (ISP \* Gbps) term, note that when the ISP is given in  $10^{-9}$  seconds (ns) and the Gbps in  $10^{+9}$  1/seconds (GHz) the exponent is a simple multiplication since the ns and GHz cancel each other. Using the example from section 2.2: (ISP)\*(Gbps) =

 $(9.6)^*(2.5) = 24$ . So in this case, it is theoretically relevant to simulate  $(24)^*(2^{24}) \sim = 400$  million bits. However in practice we find fewer bits can be used, as will be illustrated in section 4.2 and Figure 4.6.

While equations (2) and (3) have a clear theoretical explanation, they are actually pessimistic due to the occurrence of numerous redundant preamble patterns, or "overlapping". For example, the equations suggest that a 3-bit preamble would require 24 bits to cover all possible bit combinations. This might be tested by sequencing through the possible patterns, such as 000 001 010 011 and so on. Focusing on the six bits 010 011, it's easy to see that there are actually 4 different preambles covered in these six bits: 010, 100, 001, 011. So in this case, overlapping has halved the amount of bits required to test 4 different preambles. As such, intelligent algorithms could be derived to decrease the #bits value suggested by equations 2 and 3 while still maintaining complete coverage.

#### 2.3.1 Adapting the equation for encoding schemes

The previous section assumed that any combination of bits would be allowed. However, in most serial links this is not true so it's important to see how the equation changes when an encoding scheme is used.

As an example, consider the popular 8b/10b encoding scheme. 8b/10b uses 10 bits to transmit 8 bits of information while ensuring adequate transitions for DC balancing and clock recovery. As such, even though it uses 10 bits only half of the potential combinations are allowed, or 512 unique characters (further divided into 256 positive and 256 negative disparities).

Said another way, 8b/10b removes one power of 2 from the potential combinations for every set of 10 bits. Using this attribute to adapt equation 3, we can calculate the approximate #bits assuming 8b/10b encoding using:

(4) # bits = (ISP\*Gbps)\*  $2^{[(ISP*Gbps)-INT((ISP*Gbps)/10)]}$ 

...where the INT(.) function rounds off the result to the nearest integer. This equation is approximate since rounding causes some inaccuracy in how the preamble bits beyond the 10-bit intervals are allowed to vary. Continuing the 9.6 ns ISP and 24-bit preamble example, if this link was confined to 8b/10b patterns the #bits reduces from 400 million to  $(24*2^{24-2}=)$  100 million.

## 3. High-Capacity Simulation and Channel Analysis

Though the procedure in the previous section is logical, there is no practical value in it unless there is a simple and fast way to perform high-capacity (i.e., millions of bits) simulation of an MGH channel. As calculated earlier, typical transistor-level SPICE analysis would require 11 years to complete a 10-million-bit simulation.

In the examples that follow, we achieve efficient high-capacity simulation using a new capability called "Channel Analysis" available in Cadence's Allegro\* PCB SI 630 product [1], [2], [8]. Applying new mathematical techniques, Cadence has built analysis engines that can produce accurate eye diagrams hundreds of thousands of times faster than SPICE. This analysis can be performed on any drawn pre-route or extracted postroute PCB interconnect, including crosstalk. Integrated field solvers automatically create lossy frequency-dependent models of the PCB traces, and SPICE (including HSpice) models of connectors and ICs can be included as well as arbitrary S-Parameter models [4]. The tool automatically supplies PRBS, 8b/10b, or user-provided patterns as stimulus to the channel.

# bits	CA *	CA bits/sec	SPICE +	x faster
1,000	5 sec	200	10 hours	7,200
10,000	7 sec	1,400	4 days	51,000
100,000	20 sec	5,000	1.4 months	180,000
1,000,000	2.5 min	6,300	1 year	225,000
10,000,000	24.5 min	6,800	11 years	245,000

Table 3.1 provides simulation times when using Channel Analysis for various amounts of bits as contrasted with using SPICE analysis at the typical 100 bits/hour rate.

Table 3.1: Channel Analysis Simulation Times, Contrasted with SPICE

\* The Channel Analysis data is based on the PCI Express topology in section 5, using an IBM T41 laptop, with Microsoft Windows\* XP OS, 1.6 GHz Intel® Pentium® M processor (proceeded by 7.5 min "characterization")

+ Typical SPICE simulation time of 100 bits/hour (0.03 bit/sec) based on transistor-level SerDes model in a typical 3.125 Gbps channel

From the Table, note that Channel Analysis can simulate roughly 7000 bits/sec on a laptop. Note that this requires first capturing a 7.5 minute characterization, or "fingerprint", of the interconnect. However once the fingerprint is stored in the library, Channel Analysis can be performed iteratively with any number of bits at any data rate, jitter setting, or crosstalk pattern without requiring a new characterization.

The technique of simulating all possible bit combinations within the preamble may seem suboptimal since a subset of "worst case" bit patterns are likely to produce the worst case eye contour. And some have suggested techniques for determining these worst case bit patterns [3]. However, with the fast computation capability of channel analysis, this optimization becomes less important at present. But these, and other acceleration techniques, may be included in later versions particularly as data rates continue to climb.

## 4. PCI Express Case Study

To illustrate the concepts presented thus far we will use the example PCI Express topology shown in Figure 4.1. This topology includes: spec-level Tx/Rx MacroModels [5], [7], differential microstrip and stripline traces, S-Parameter via models for 8- and 32-layer PCBs, and SPICE connector subcircuits. The end-to-end interconnect length is roughly 24 inches.



Figure 4.1: Example PCI Express Topology

Figure 2.2 shows the ISP for this configuration, which was determined to be 9.6 ns. Once the ISP is known, we could go directly to Channel Analysis (section 4.2), but first we perform some time domain simulation to illustrate the "preamble" concept.

#### 4.1 PCI Express Topology Preamble

From the 9.6 ns ISP, using equation (1) we can calculate the expected preamble size of 24 bits. To verify this in practice, we simulate the initialized topology with a consistent Test Pattern preceded by zero to four 8b/10b preambles as shown in Figure 4.2. Note that the 8b/10b characters are consistent in each preamble.

The question to answer is: "Is the Test Pattern only affected by the previous 24 bits, and nothing prior to that?" To answer this question, Figure 4.3 superimposes a zoom in on the Test Pattern produced by the 5 scenarios in Figure 4.2.



Figure 4.3: Superimposed Test Pattern Waveforms

Examining Figure 4.3 closely, we can observe the following:

1) At the start of the Test Pattern (about 29 ns) there are only 4 waveforms visible. This means that the 40-bit preamble and the 30-bit preamble produce the exact same Test Pattern. This is what we would expect, since changes in the 25th and previous bits should have no effect.

2) At the vertical red cursor (about 30.5 ns) there are only 3 waveforms remaining. This means that the 20-bit pattern has now converged with the 30- and 40-bit patterns. Note that this occurs 4 bits into the test pattern, or after they have been exactly the same for the previous 24 bits (the calculated relevant preamble size).

3) At the vertical blue cursor (about 34.5 ns) there are only 2 waveforms remaining. At this point the 10-bit pattern converges with the 20 = 30 = 40-bit patterns. This occurs 14 bits into the Test Pattern after the 10-bit pattern has been the same as the others for 24 bits. This is again the calculated preamble size.

We offer this to show the practical validity of the relevant preamble derived directly from the ISP determined in Figure 2.2. The results match the linear time-invariant channel assumption very well.

### 4.2 High-Capacity Simulation Using Channel Analysis

Performing high-capacity simulation on the topology, we plot the convergence of eye height versus the number of bits simulated in Figure 4.4. Although PCI Express is specified to operate at 2.5 Gbps, we use the interconnect's "fingerprint" characterization within Channel Analysis to quickly determine the eye height at other common data rates and add them to the plot.



Figure 4.4: Eye Height vs. #bits for Common Data Rates and #bits(ISP)

From this plot, we can make the following observations:

1) Eye height decreases as more bits are simulated, as expected, and appears to approach an asymptotic value.

2) The required number of bits suggested by the ISP, as calculated for each data rate using equation 2 and plotted by the red "ISP" circles, appears to represent a point well beyond the knee of the curve at which the eye height converges (or, becomes linear).

3) There is significant error in the simulated eye height if the # bits as a function of the ISP is not reached. For example, at 2.5 Gbps the eye simulated using 100 bits (~400 mV) is almost 2 times wider than if the ISP is reached (200 mV). Unfortunately, many current MGH methodologies simulate in only the 100 to 1000 bit range and can suffer a large amount of inaccuracy.

Exploring the last observation further, in Figure 4.5 we plot the error factor in terms of eye opening for the different data rates that would occur when simulating 100 bits compared to the # bits calculated using the ISP in equation (2).



Figure 4.5: Eye Height Error Factor Using 100 bits or #bits(ISP)

From the Figure 4.5 observe that the error increases exponentially with data rate, as would be expected based on equation (2). This suggests that a change in methodology is essential as we move to even higher data rates.

While it is important to point out the inaccuracies of using short ~100 bit time domain simulations, the data also shows that it may not be necessary to simulate the complete number of bits calculated by equation (2). Plotting the 2.5 Gbps data from Figure 4.4 another way, Figure 4.6 shows how the amount of error in eye height measurements increases as we move orders of magnitude away from the #bits calculated from the ISP. This plot reveals that getting within 3 orders of magnitude of the #bits (ISP) yields only a 2.5% error, which may be acceptable in most applications.



Figure 4.6: %Error versus orders of magnitude from #bits(ISP)

## **5. Serial ATA Case Study**

In this section, the Channel Analysis feature will be demonstrated with a case study of a Serial ATA (S-ATA) interface. Eye contour results obtained from Channel Analysis (CA) will then be correlated with contours from traditional HSpice time-domain (TD) simulations.

#### **5.1 Serial ATA Channel Topology**

S–ATA is a high-speed industry-standard data link specification commonly used for disk drive interfacing. The topology used for Serial ATA is shown in Figure 5.1. This is a sixline topology, which includes three differential pairs capable of being driven from either end. Only one transmitting pair is active in this simulation and dummy terminations are used for the other two. Transmit pre-emphasis techniques are used for the S-ATA interface. As such, the transmitter is implemented as a MacroModel [5], [7] that includes both a main buffer and a boost buffer. The topology includes driver, package, break-out trace, motherboard trace, via, connector, and cable. AC decoupling capacitors are not included in the simulation to reduce the simulation time, but this should not affect the results.



Figure 5.1: Serial ATA specification topology

Figure 5.2 shows the topology configuration under SigXp. The transmitter is implemented as a DML MacroModel, and all the interconnect models were translated from various SPICE and RLGC models and implemented as black box models in SigXp.



Figure 5.2: S-ATA channel configuration under SigXp.

#### 5.2 S-ATA Topology ISP Analysis

Using the techniques outlined in section 2.1, determining the ISP for this topology leads to some interesting engineering judgment. Consider the topology's pulse response shown in Figure 5.3.



Figure 5.3: Pulse response for S-ATA channel

In this case, the ISP end point is not as obvious as in Figure 2.2. Instead, we see decreasing amplitude noise at intervals related to the round-trip delay on the interconnect. This type of response is common.

Using the first technique (found in step 3 in section 2.1) we would determine the ISP to be about 4.5 ns. However, if we believed that 7 mV of accuracy is relevant (~3% of the expected eye height) we might be inclined to choose the second noise pulse (at ~1.075 us) and set the ISP at 9 ns. This decision brings up an important point: knowing the data rate, we might pragmatically choose the longer ISP (and hence greater accuracy) if we calculate that the number of bits from equation 3 can be simulated with little extra compute time. As such, we might choose ISP = 9 ns at 1.5 Gbps (#bits = 150k) but an ISP = 4.5 ns at 3.0 Gbps (#bits is still 150k) with a potential inaccuracy of 3% in the final result. Note that a 3% tolerance is typically acceptable (and often expected) in both simulated and empirical measurements.

#### 5.3 Results and Correlation Using CA and HSpice Simulation

Two different sets of comparisons were conducted in this case study. First, the worst-case eye contours predicted by CA with long pseudo-random bit sequence (PRBS) patterns are compared with the eye contours generated from traditional time-domain HSpice simulation results. Second, the accuracy of the CA tool is validated against HSpice simulations by comparing the eye contours from CA and HSpice based on the same input stimulus pattern.

#### **5.3.1 Eye contour comparisons using both methodologies**

In this section, we demonstrate CA by overlaying its eye contour predictions with timedomain HSpice simulation results. The input stimulus patterns for the TD simulations are either empirical worst case input patterns (based on industry-standard test patterns, such as K28.5), or random input patterns, as shown in Figure 5.4, 5.5 and Table 5.1. Data in Figure 5.4 are based on 1.5 Gbps data rate (S-ATA Gen. I) simulation and Figure 5.5 on 3 Gbps (S-ATA Gen. II). In this comparison study we are interested in observing the general trends, so both sets of simulations were based on Gen. I models and only the data rate was adjusted.

Figure 5.4 and Table 5.1 show that a 1-million-bit PRBS CA simulation at 1.5 Gbps reports an eye contour that is 115 mV worse than the one reported by a traditional TD simulation based on a 75-bit random input pattern (406 mV inside height and 652 outside height, versus 443 mV inside height and 574 mV outside height). It should be noted that, due to computing capability constraints, using short random input patterns is a widely adopted methodology when empirical worse patterns are not available. In this case, this methodology presents approximately a 20% error when compared with the data available from CA simulation even though both techniques require a similar amount of simulation time.

Considering that only 8b/10b patterns are allowed in S-ATA interface, a difference of 70 mV can still be seen (427 mV inside height and 627 mV outside height, versus 443 mV inside height and 574 mV outside height). In both cases, CA reports results that can be considered more accurate than empirical worst case input patterns (e.g., K28p5 and lone-bit patterns).



Figure 5.4: 1.5 Gbps eye contours generated from CA and HSpice simulations

Data Rate	Tool	Stimulus Pattorn	Worst Case Inside	Worst Case
		Stillulus Fatteri	Eye Height	Outside Eye Height
1.5 Gbps	CA	1000-bit PRBS	428	627
		10000-bit PRBS	412	644
		100000-bit PRBS	408	650
		1000000-bit PRBS	406	652
		100000-bit 8b/10b	427	627
	HSpice	K28p5 (repeat for 75 bits)	437	604
		Lone-bit (repeat for 75 bits)	433	599
		Random (repeat for 75 bits)	443	574
3.0 Gbps	CA	1000-bit PRBS	320	521
		10000-bit PRBS	305	543
		100000-bit PRBS	298	550
		1000000-bit PRBS	290	556
		100000-bit 8b/10b	319	517
	HSpice	K28p5 (repeat for 75 bits)	336	486
		Lone-bit (repeat for 75 bits)	325	506
		Random (repeat for 75 bits)	340	448

TABLE 5.1. Eye measurements using CA and HSpice simulations. (Note: worst case inside eye height is the minimum eye open on the inside contour between 0.4 UI and 0.6 UI and; worst case outside eye height is the maximum eye open on the outside contour between 0.0 UI and 1.0 UI.)



Figure 5.5: 3.0 Gbps eye contours generated from CA and HSpice simulations

The trend becomes more obvious as the transfer rate increases. At 3 Gbps, Figure 5.5 and Table 5.1 show that the eye margins from 1-million-bit PRBS CA simulation varies 158 mV from a 75-bit random pattern (a 28% discrepancy). If only 8b/10b patterns are considered, the difference is 90 mV. Similar to the 1.5 Gbps case, CA reports data that is expected to be more accurate than empirical worst case input under both assumptions.

Comparing the data presented in Table 5.1 against the ISP discussion in section 5.2, it is not surprising to note that the 1.5 Gbps eye height converges around 100k bits, while the 3.0 Gbps data converges later (closer to the million-bit range). Note that the use of PRBS patterns does not ensure complete coverage of all possible patterns, thus making the eye convergence and the use of equation 3 more approximate. For more discussion on the probability of covering all patterns when using PRBS stimulus, refer to section 5.4.

#### 5.3.2 Eye contour comparison using the same stimulus pattern

In this section, the accuracy of CA is illustrated by correlating eye contours generated by CA and HSpice TD simulations using the same input pattern. The comparison was again performed at two transfer rates: 1.5 Gbps and 3 Gbps. Figure 5.6 and Figure 5.7 show very good correlation of eye contours between CA and HSpice TD simulation at 1.5 Gbps at 3 Gbps on a K28p5 pattern (the pattern was repeated for 75 bits for the 1.5 Gbps case and 150 bits for the 3 Gbps case).







Figure 5.7: 3.0 Gbps eye correlation using CA and HSpice with the same stimulus

#### 5.4 Bit Pattern Coverage Probability

The duration of ISI effect, and hence the ISP, varies significantly from one interface implementation to another. According to peak distortion theory [3], if a channel can be approximated as a linear time-invariant system, there exists worst case input stimulus patterns that likely lead to the worst case eye margins. Attempts can be made to either derive and use these patterns, or exhaustively cover them if the simulator is fast enough – as in the case of Channel Analysis. However, a question arises as to the probability of simulating a supposed "worst-case pattern" given various preamble and pseudo-random bit sequence (PRBS) simulation lengths. Note that PRBS patterns do not necessarily cover all possible patterns.

A simulation-based statistical analysis has been performed to calculate the probability of pattern coverage. Here "pattern coverage" refers to the likelihood that a long sequence includes a certain short sequence (e.g., "worst-case pattern"). In Figure 5.8, probability curves based on pattern match experiments are shown. The figure shows the probabilities of long PRBS including a certain n-bit long worst case pattern ( $n \le 20$  here). The simulation is not an exhaustive experiment, so the resulting curve approaches the exact solution but is not the exact solution. The figure shows that users should have fairly high confidence (> 98.09%) using a 1-million-bit random pattern, if the length of worst case pattern (preamble) is shorter than or equal to 18 bits. Based on these curves, users can easily determine how long they need to run the random pattern simulation in order to cover a potential worst case pattern.



Figure 5.8: Probability of long random pattern covering worst-case patterns

## 6. Conclusions

As MGH serial links find their way into mainstream digital designs, it is not surprising that new characterization techniques have come with them. Over the past five years, much of this has been hardware oriented. This paper has introduced new pre-hardware concepts, tools, and methodologies, and illustrated the same using two industry-standard configurations: PCI Express and Serial-ATA.

Serial links have redefined timing requirements to focus on the integrity of eye openings. Eye height and width can not be properly analyzed without comprehending the storage and decay of energy in the system. The Interconnect Storage Potential (ISP) is a useful measure of an interconnect's capacity to store charge, and provides insight into the types of bit streams required to develop a meaningful eye diagram. Ignoring the ISP's guidance can cause simulation inaccuracy to increase exponentially with data rate.

Channel Analysis (CA) is a new publicly available tool that offers fast simulation of very long bit streams. Since it is hundreds of thousands of times faster than SPICE, engineers can characterize serial link design trade-offs in ways not possible previously. We expect this will enable the discovery of new interfacing techniques at even higher data rates.

Channel Analysis has been shown to improve the quality of pre-hardware simulation. On the links considered, improvement has ranged from 20% to 260%. Insight into the range of improvement expected on an interconnect can be gained by quantifying the ISP and running some quick simulations.

We have deliberately focused on introducing concepts and contrasting design methodologies, leaving the quantification of the accuracy of CA to other papers cowritten by Cadence with Agilent Technologies [9], [10], [11]. These papers show correlation with physical measurement and other tools at various data rates. Some comparisons have been offered showing CA simulation output with time domain HSpice simulation on short bit patterns. Due to computational time differences, comparison with the extensive data streams that CA is designed to handle is not possible.

### **Reference Materials**

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