cadence

New IBIS Techniques for Modeling Complex IO

Cadence Webinar

March 23, 2005

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About the Presenter

Donald Telian

- 20+ years in high-speed PCB and SI
- Engineer at Cadence, Intel, HP
- Originated IBIS modeling
- Designer of PCI bus
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Other Helpful Webinars

- Go to www.cadence.com/webinars to view:
  - How to build fast and accurate **multi-gigabit transceiver models** (Jan '04)
  - Understanding and Using **S-Parameters** for PCB Signal Integrity (June '04)
  - Introducing **Channel Analysis** for PCB Systems – high-capcity simulation for Multi-GHz design (July '04)
  - Designing multi-gigahertz **serial interconnects** using frequency, time domain analysis, and lab measurements (Feb '05)

This is the 5th webinar in the Multi-GigaHertz (MGH) webinar series

Agenda

- Current Situation
- Industry Polling
- New Solutions
- Summary
- Q & A

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The Current Situation

CMP United Business Media

EETIMES ONLINE

Need for simulation models is not being met

Rick Merritt
EE Times
(12/20/2004 9:00 AM EST)

Many chip and connector vendors are failing to deliver the detailed component simulation models that enable engineers to design in those parts in an accurate and timely way. The problem sometimes forces engineers to rework their systems at a late stage of design, which can cost thousands if not millions of dollars, including lost time-to-market.

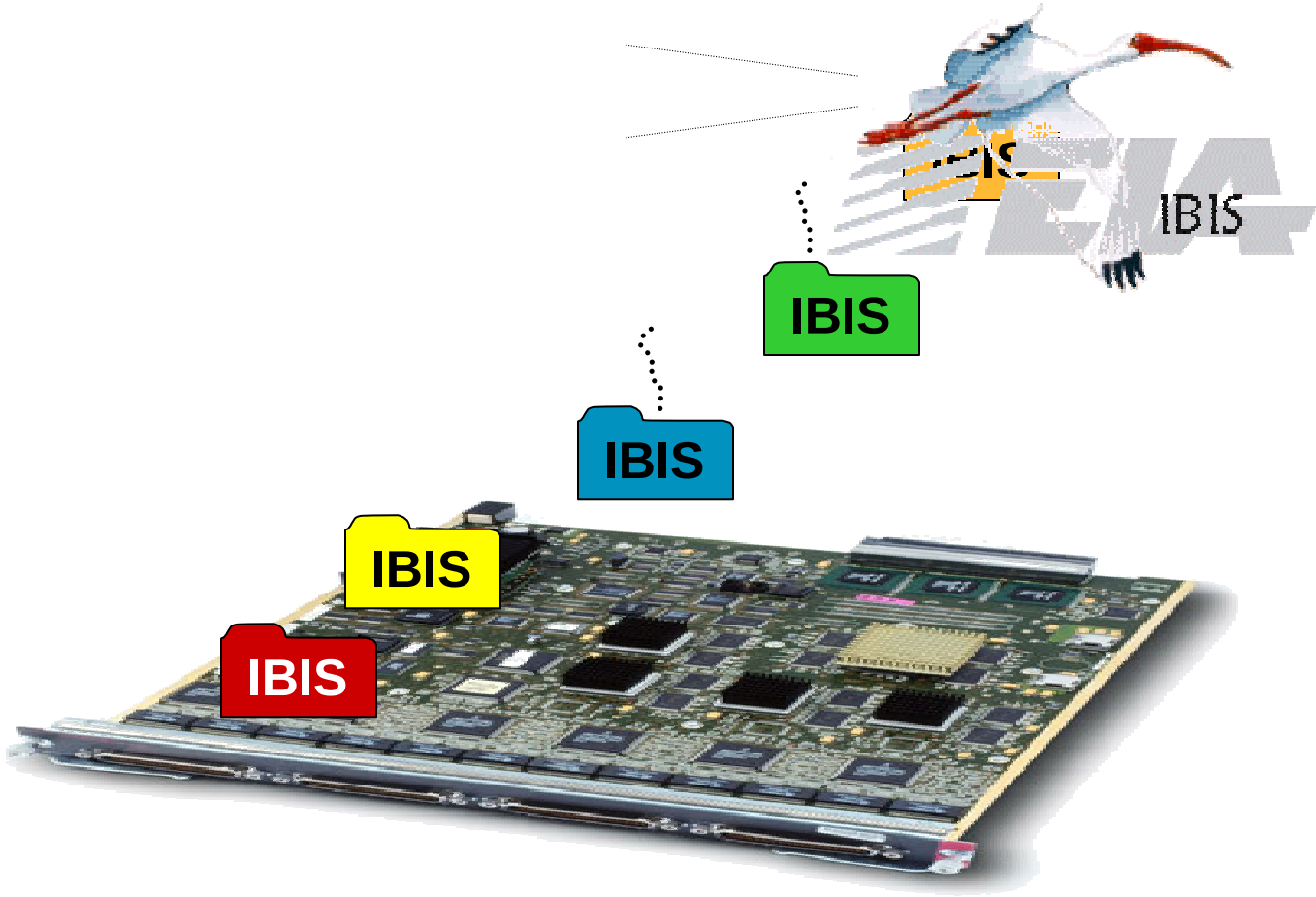
An Emulex Corp. engineer said that today's Ibis models are no longer adequate and that OEMs must demand more thorough HSpice models. "We have to drive it," he said.

http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=55800427

Industry Challenge Project: "Choosing the Right Interconnect"

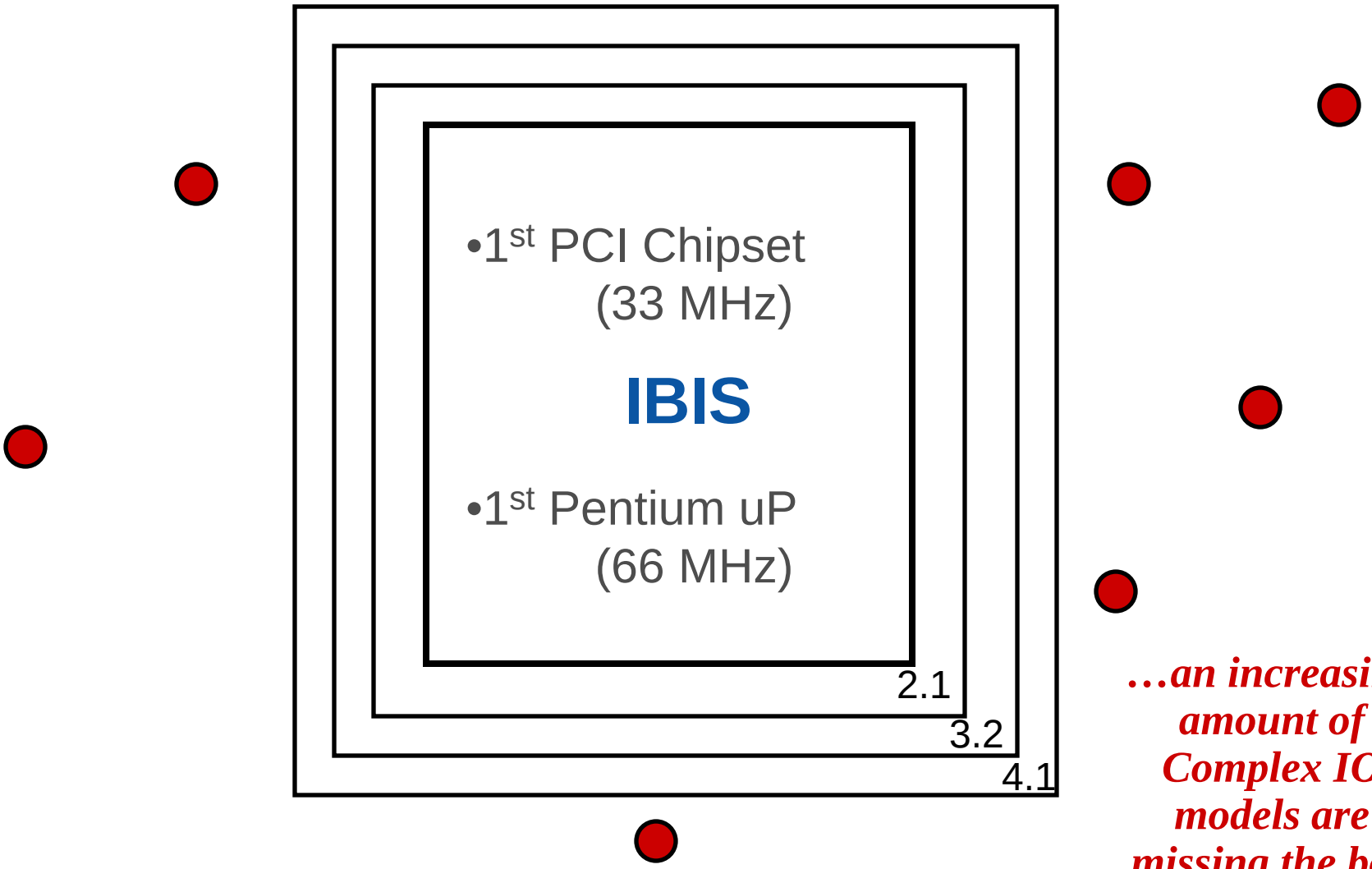
http://www.eet.com/industrychallenges/interconnect/

What We'd Like to Have Happen



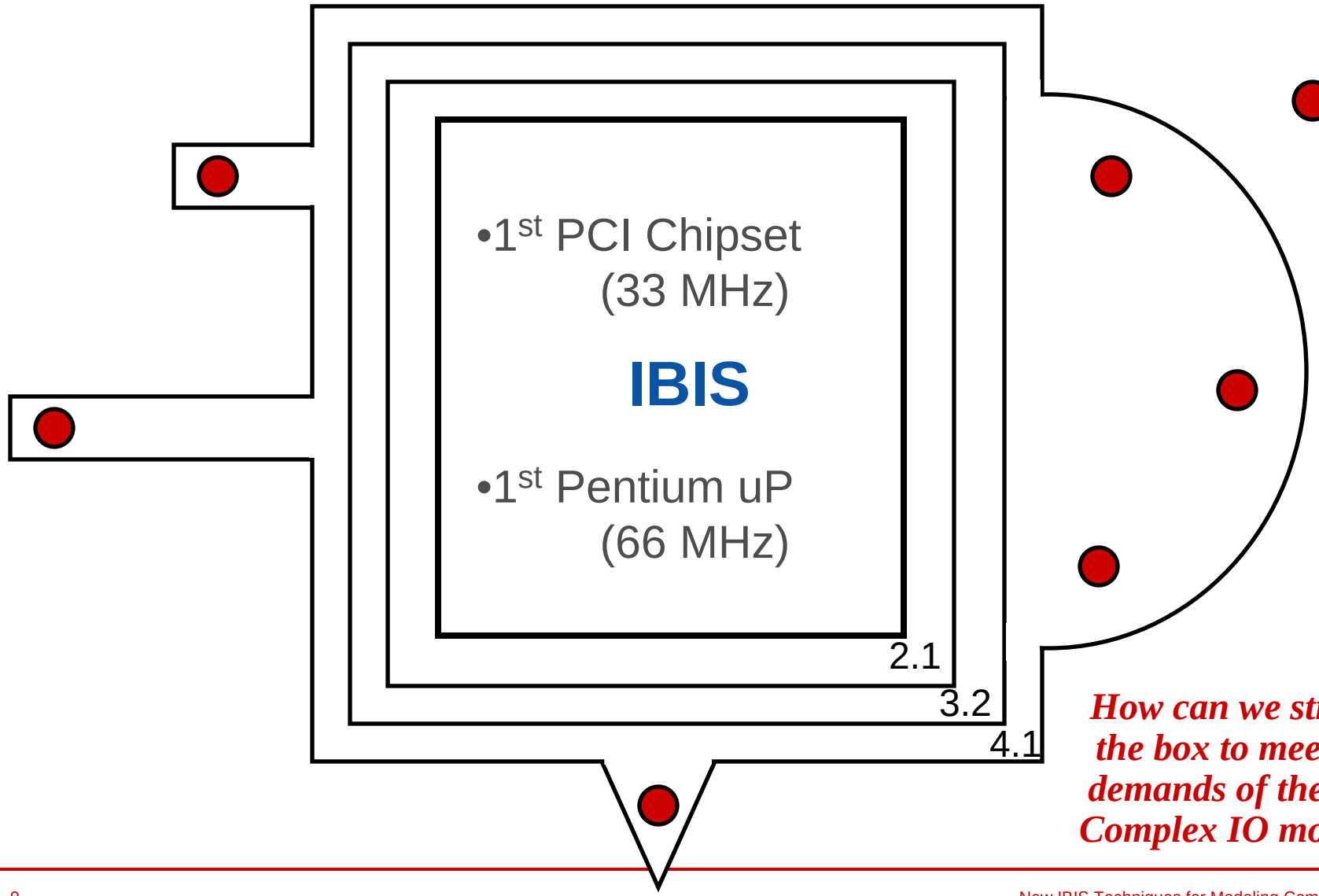
Obtain IBIS files that automatically load the correct models for every component on my PCB.

Unfortunately, although the IBIS Box has expanded…



…an increasing amount of Complex IO models are missing the box

Today: Using IBIS for These Complex IO



How can we stretch the box to meet the demands of the new Complex IO models?

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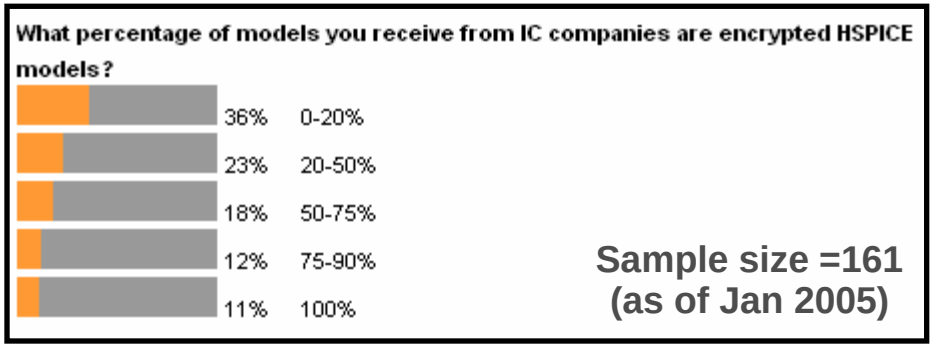
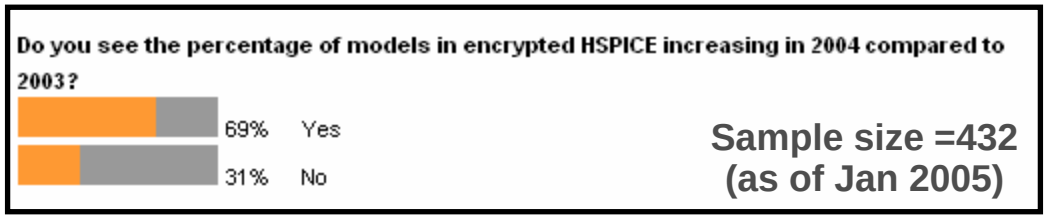
High-Speed PCB Web Surveys

- 64% say that more than 20% of the models they receive are Hspice



http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=62

- 69% say that this percentage increased in 2004 over 2003



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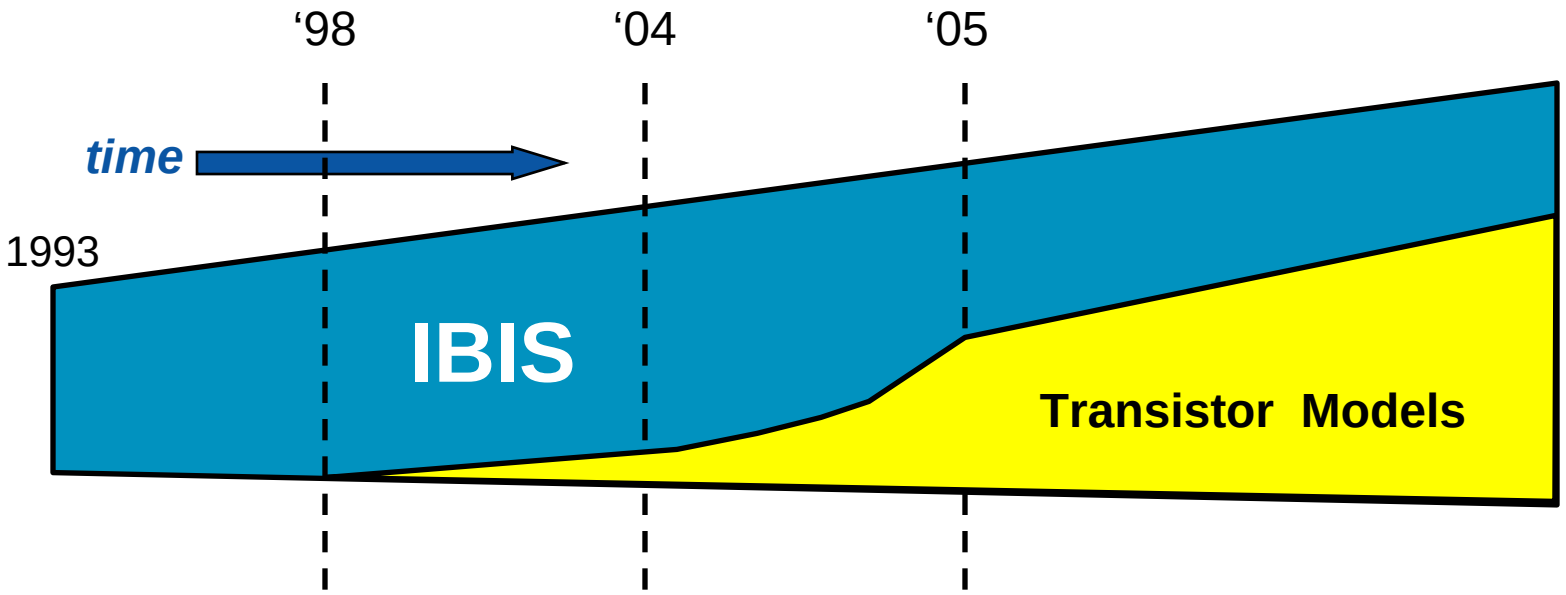
What has Happened

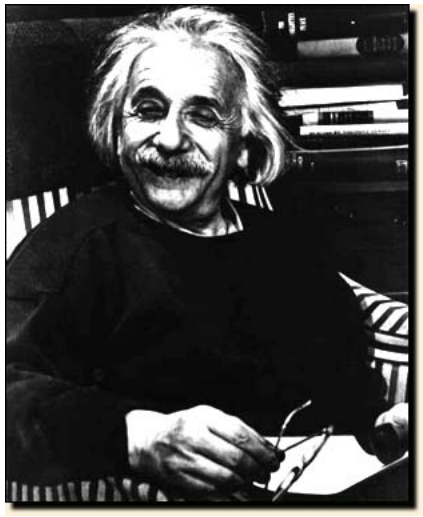


- IBIS enjoyed 5 years as THE digital IO model format
- Higher frequencies brought new issues and more skeptics
- Gigabit serial links brought rapid transistor model increase in 2004

Need to take a deeper look into the needs of Complex IO

11 Interviews During December 2004

- All interviewed were involved with Complex IO
  - Majority were not CDS users
- Good in-depth look at the issues
- The issues are many
  - and the solutions weren't clear
- Will use this data to propose solutions
- Most want "industry standard solution"
  - but don't know how to get there



Hspice Related Interview Questions

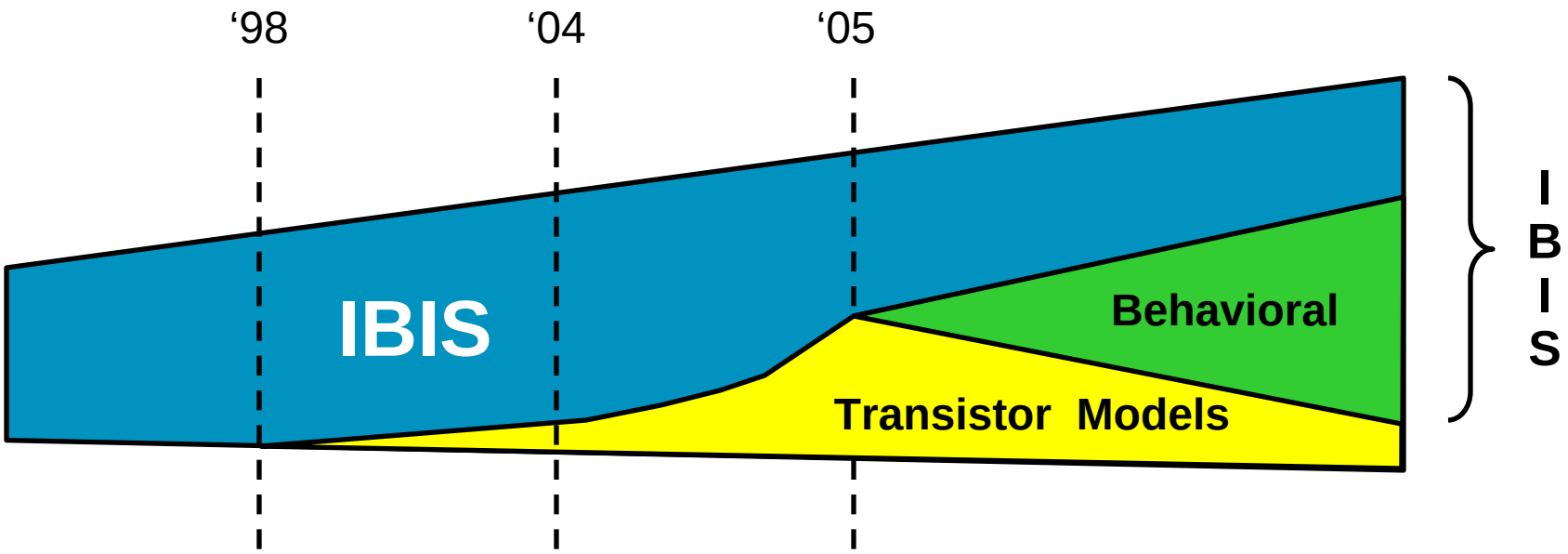
- "Do you want to see [External Model] Hspice?" - all "yes"
  - Half qualified this as a non-optimal short-term solution

This is actually already happening

- "Do you see Hspice as a long-term solution?" - all "no"
  - Unanimous reason: "it's too slow"

- As such, also unanimous in need to return to behavioral

What Needs to Happen



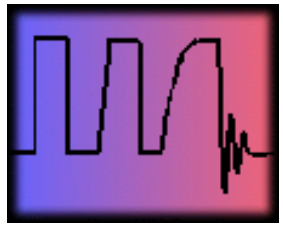
- Enable faster behavioral solutions

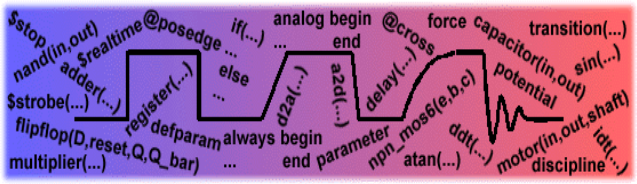
What behavioral options exist?

AMS Models – Issues to Solve

- Most interviewed at this point are unfamiliar with AMS
  - When asked if they think AMS can be a good solution:

    3 said “yes”, 3 were hopeful, and 4 were unsure, 1 said no
- Unfamiliar in SI world, learning curve exists
  - Must seed with templates / training
- Spec nuances/implementations (as with IBIS)
- Not naturally occurring in IO design
  - This is why transistor-level models get used
- Does not naturally offer IP protection
  - 3 would encrypt, 2 might, 4 are unsure, 2 would not
- Does it make sense / cents?
  - Or, are SI users prepared to pay more for this feature?



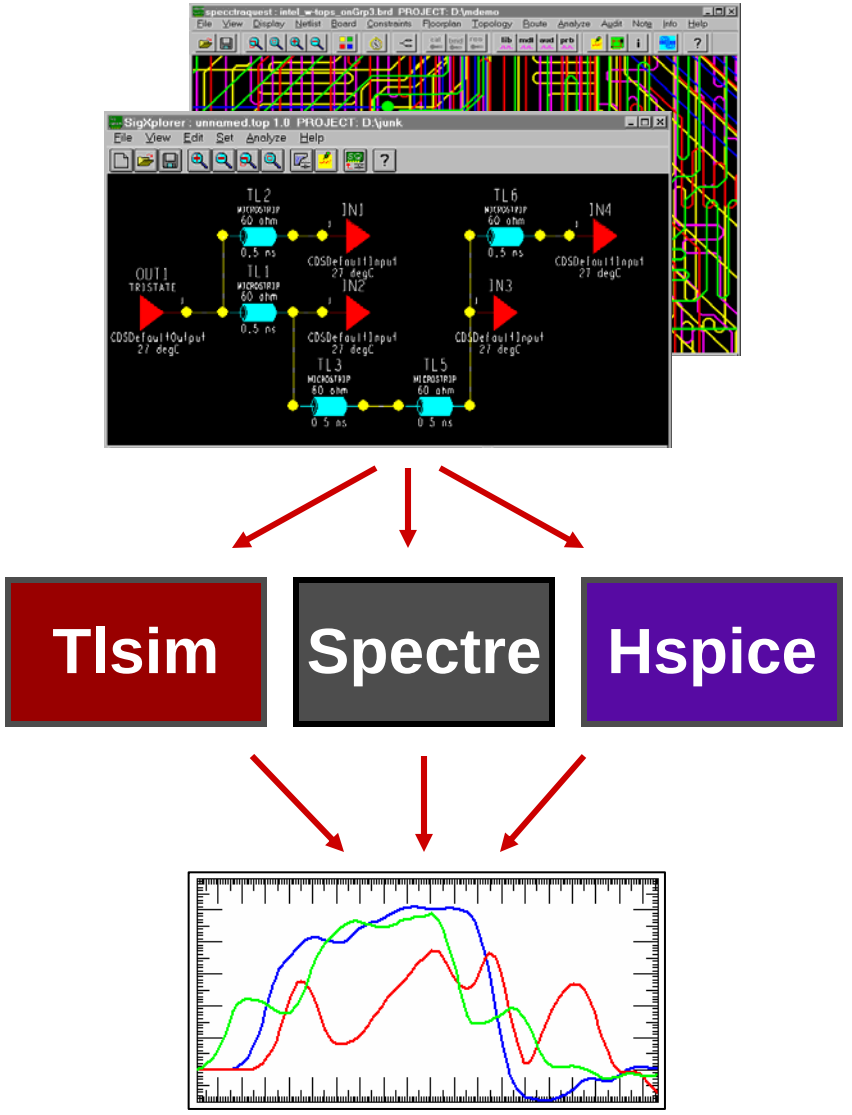


Agenda

- Current Situation
- Industry Polling
- New Solutions
  1. Transistor Models
  2. Faster Simulation
  3. [Driver Schedule]
  4. Behavioral MacroModels
  5. [External Model] SPICE
- Summary
- Q & A

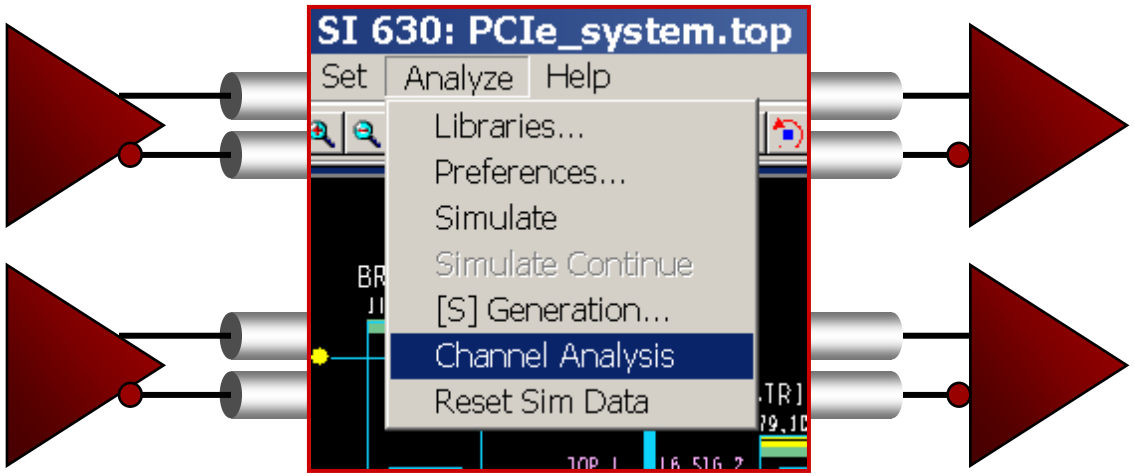
1. Transistor Model Solutions

- Allegro SI has interface to Hspice now
  - Adding Spectre interface, has encryption
- IBIS 4.1 [External Model] can point to these models
  - Customers unanimously asking for it
- Cadence will add both [EM] Hspice and [EM] Spectre
  - Soon, when IBIS 4.1 parser and translator are integrated in aSI
- Result will be automatic “wrap” of transistor model
  - Hence, automatic use within PCB tools



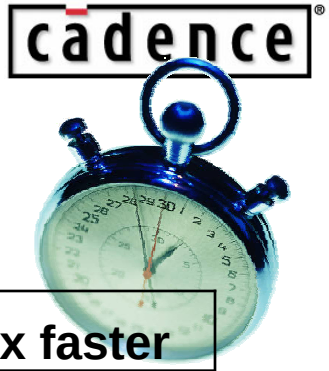
2. Fast Simulation: Channel Analysis

- FAST simulation of millions of bits, with any model type
- New frequency domain analysis capability in Allegro PCB SI
- Any SigXp differential topology, including pair-to-pair crosstalk
- Tx/Rx can be DML, MacroModel, IBIS, or Hspice
- Automatic PRBS, 8b/10b, random, or user-defined bit sequence



Faster simulation by using a faster simulator with existing models

How Fast Is Channel Analysis?



# bits	CA *	CA bits/sec	SPICE +	x faster
1,000	5 sec	200	10 hours	7,200
10,000	7 sec	1,400	4 days	51,000
100,000	20 sec	5,000	1.4 months	180,000
1,000,000	2.5 min	6,300	1 year	225,000
10,000,000	24.5 min	6,800	11 years	245,000

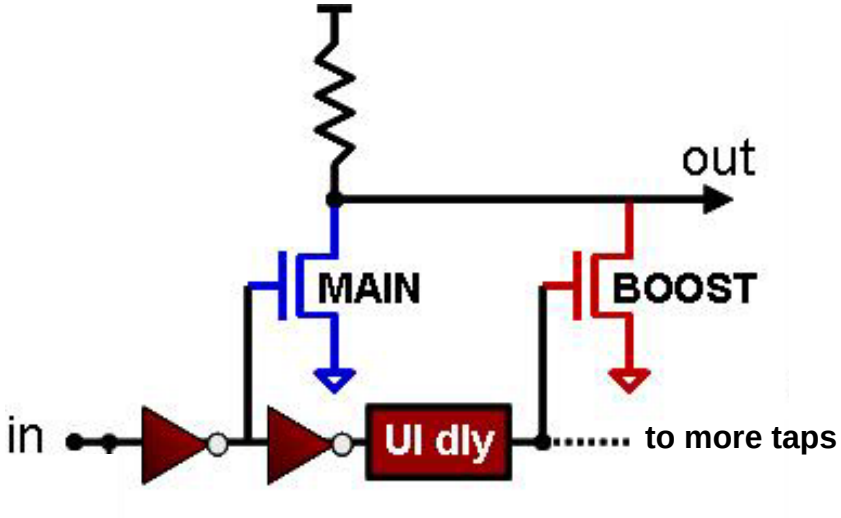
* Reference topology, IBM T41 laptop, Windows XP, 1.6 GHz Pentium M (proceeded by 7.5 min “characterization”)

+ typical SPICE simulation time of 100 bits/hour (0.03 bit/sec) based on transistor-level SerDes model in a typical 3.125 Gbps channel

See award winning DesignCon 2005 Channel Analysis paper, free download at:

http://www.cadence.com/community/allegro/resources/resources_pcbsi/mgh/Dcon05_ISP_CA_Intel.pdf

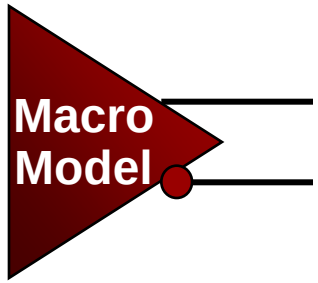
3. [Driver Schedule] for Pre-Emphasis



- Can now use native IBIS syntax to model pre-emphasis
  - Recent development: enabled by BIRDs 84 & 88
- Concept: Schedule the staged drivers/taps in time
- IBIS [DS] 2tap and 4tap examples in free Cadence download:
  - http://register.cadence.com/register.nsf/macromodeling?openform
- Covered in EETimes 2/14/05 and Jan'05 IBIS Summit
  - http://www.eetimes.com/issue/dc/showArticle.jhtml?articleId=60300186
  - http://www.eda.org/pub/ibis/summits/jan05/muranyi.pdf
    - Correlation data shown in these slides
    - Open_side devices work better with Ramp instead of VT curves

4. Behavioral SPICE MacroModels

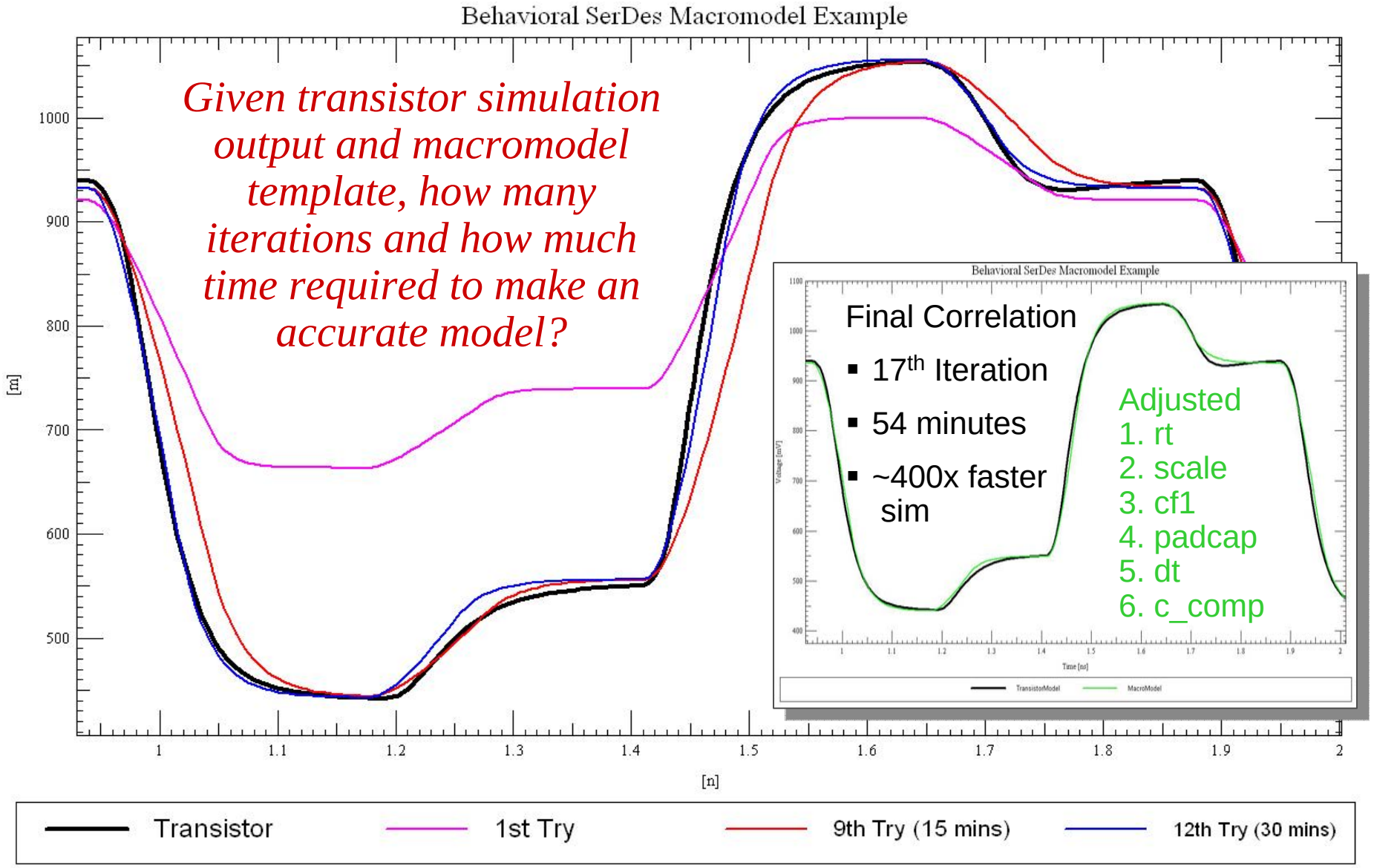
- Standard feature in Allegro PCB SI for many years, accessible examples:
  - 2.5 Gbps PCIe SerDes Chipset
    - http://www.cadence.com/company/newsroom/press_releases/pr.aspx?xml=090804_intel
  - 1.5 Gbps S-ATA SerDes
    - http://www.designcon.com/conference/7-ta3.html
  - Differential pass-thru receiver
    - http://www.eda.org/pub/ibis/summits/jan00/telian.zip
  - Adjustable FPGA SerDes
    - http://www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-cadence_design_kit.html
  - Front-side bus driver, impedance control, SSN, & gate choke effect
    - http://www.cadence.com/company/newsroom/press_releases/11_16_98_SQ_Intel_Merced_Processor.doc



Technique has been used for many "beyond IBIS" Complex IO models

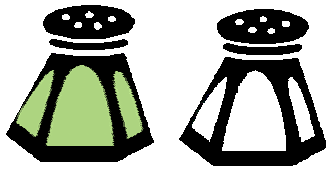
Ready-to-run templates at: http://register.cadence.com/register.nsf/macromodeling?openform
(samples produce same waveforms as [Driver Schedule] examples, yet user can adapt structure)

Case Study: Agere Systems 4 Gbps SerDes



5. [External Model] SPICE

- IBIS 4.1 specifies [External Model] SPICE
  - Allegro PCB SI will use this to point to behavioral SPICE MacroModels
- For most, SPICE == Transistor Model
- BUT



SPICE also == Behavioral MacroModeling

- Interviews found many engineers are already doing this in some form and in various tools
- Some history:

  this is the technique Arpad used to invent IBIS and release the first schematic

What Experience has Shown

- Cadence has used SPICE macromodeling to make IBIS keyword support quite simple
- Once we had a central IBIS 2.1 driver element

All later keywords have been macromodeled around it

- In other words, basic SPICE around a B drvr/element has handled everything IBIS has added for the last 10+ years
- What has slowed the industry down is that *additions have belonged to the committee*, and not the model maker

[EM] SPICE empowers the model maker to also add new features

SPICE MacroModeling

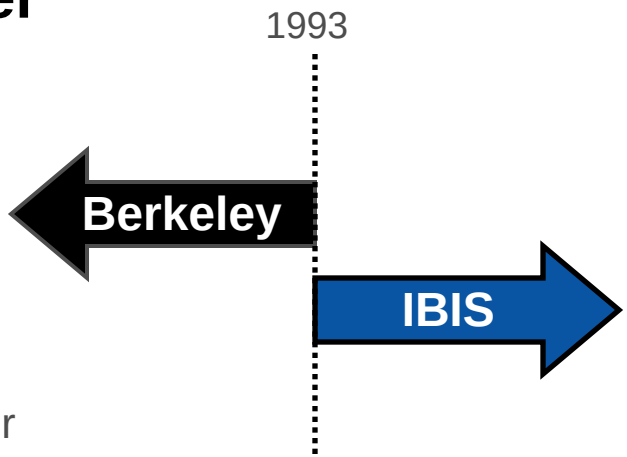
- IBIS began with it
- Many tools and users have experience with it
- With template help, model makers are succeeding
- Academia is quite engaged in macromodeling research
  - http://domino.research.ibm.com/acas/w3www_acas.nsf/images/proposals_04.05/$FILE/madhavan.pdf
  - http://domino.research.ibm.com/acas/w3www_acas.nsf/images/projects_03.04/$FILE/canavero.pdf
  - http://www.spi.uni-hannover.de/2004/presentations/spi04_s08_p02_Stievano.pdf … etc.
- Cadence is implementing [EM] SPICE now
- Cadence has offered MacroModel templates to the IBIS Committee and proposed specification enhancements to better support [EM] SPICE macromodeling
  - http://www.eda.org/pub/ibis/summits/jan05/telian.pdf

How can the IBIS Committee better support this?

2 Things IBIS can do to Improve [EM] SPICE

1. Remove the Berkeley SPICE Barrier

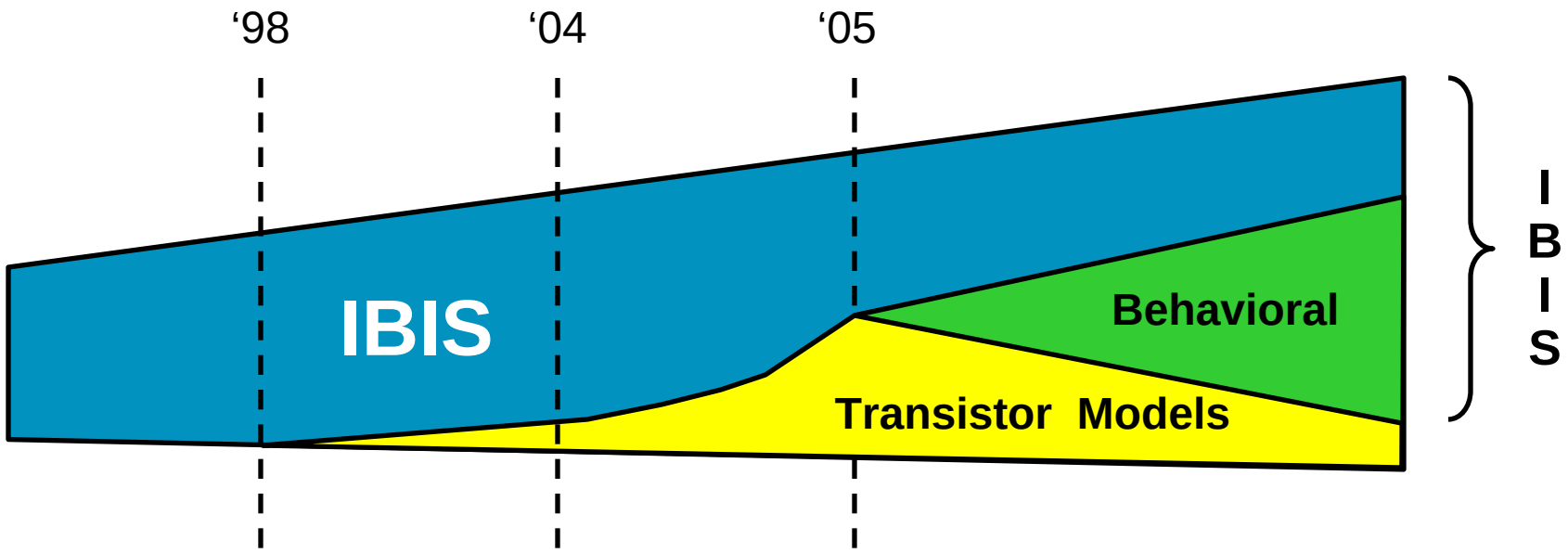
- IBIS ties itself to Berkeley SPICE 3F5
  - This was released/closed in 1993
  - No effort since then – yikes!
- No PCB SI tools use 3F5
  - It is lower than the lowest common denominator



2. Add 3 Updated SPICE Primitives

- IBIS Driver, Table-based EFGH sources, Parameters
- With these elements, all known Complex IO can be implemented
  - Syntax choice is not critical
- All modern SPICE tools have these features
  - Yet IBIS spec does not comprehend them

Working to Enable Behavioral Modeling



- Three new behavioral techniques demonstrated with templates available
  - [Driver Schedule] pre-emphasis
  - Cadence MacroModels
  - [External Model] SPICE macromodeling
- An on-going area of effort, research, collaboration and investment at Cadence

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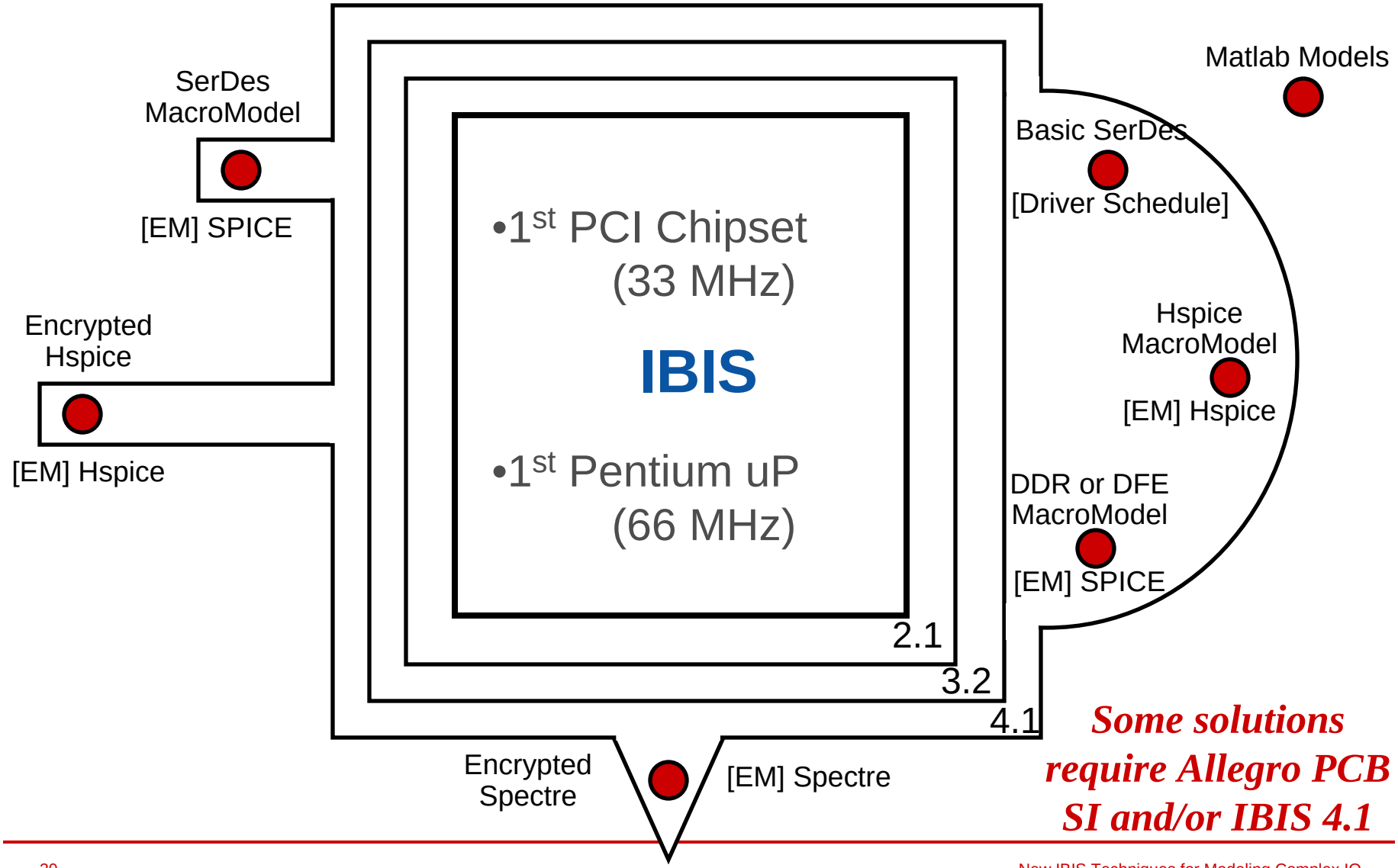
Solutions you can use from IBIS



Some solutions require Allegro PCB SI and/or IBIS 4.1

Solutions Summary & Timeline

Modeling Solution	In aSI:	Achieves
Channel Analysis	Now	Faster simulation with any model
[DS] Pre-emphasis	Now	Behavioral SerDes in native IBIS
Behavioral MacroModel	Now	Flexible behavioral model from templates
[EM] SPICE	Q3 '05 *	Macromodels used within IBIS
Hspice interface	Now	Hspice models within aSI, must wrap models
[EM] Hspice	Q3 '05 *	Hspice called from IBIS, models auto-wrap
[EM] Spectre	Q3 '05 *	Encrypted Spectre called from IBIS

* Could be sooner, date pending integration of new IBIS 4.1 parser and [EM] translator (contact Cadence)

- Ready-to-run model example files available for free download:
  - Allegrosi.com -> Signal Integrity -> Technical Resources -> Multi-GigaHertz -> Request for…
  - OR, goto: http://register.cadence.com/register.nsf/macromodeling?openform
- More info available at www.cadence.com
  - http://www.cadence.com/products/si_pk_bd/index.aspx?lid=spb

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