Signals on Serial Links: Now you see 'em, now you don't. What can we do?

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cdnusers asked Donald Telian to send us some commentary from DesignCon 2007 and the Cadence technologies discussed there. Following are his observations from the show.

Serial Links have brought a number of discontinuities for Signal Integrity (SI) engineers to sort out. While the blazing fast data rates get most of the attention, it's actually the subtler things that keep us up at night—things like ¼ wavelength stubs, differential-pair skew, fiberglass weave, insufficient models, and the way signals disappear in FR4. If you're one of those keeping an eye on how all this is changing the way we do SI, read on.

A good place to take the pulse of the SI community is at DesignCon. Over the years, I've watched it become the primary yearly show for SI engineers. If you're involved in SI and not already attending, you should think about participating next year. There's other things going on there, but where else can you find an entire panel discussion devoted to the resistance of a decoupling capacitor?

This year's show had some very identifiable trends. As Rick Merritt quoted me as saying in his recent EETimes article, serial link equalization is rapidly moving from the transmitter to the receiver. And there was an entire track of papers devoted to just that. Tx equalization (we often refer to it as "pre-emphasis" or "de-emphasis") was a bit simpler because you knew the data pattern you were attempting to equalize in the system. Conversely, Rx equalization must be smarter because it must extract both the data and the clock out of a basically unknown—and many times almost non-existent—signal. I say "non-existent" because differential signals at the Rx are quickly disappearing at higher data rates. This is due to losses in standard FR4, and other phenomena.

Yet Rx equalization schemes have come a long way. Current implementations now routinely boost a collapsed signal by close to 20 dB, and many new techniques are on the dock, as this year's papers clearly demonstrated. However, while we're applauding our new abilities to recover a signal out of an ugly pile of analog noise, we find we've created another monster. Once again, the signal appearing at the component pins can't be measured.

Creating signals we care about yet can not externally observe is nothing new. We did this to ourselves before when we dabbled in specifying timings to places inside the IO ring. Mechanically, it also happened with the introduction of the BGA.

A well-attended DesignCon panel was convened to examine solutions to the problem of un-measurable signals on next-generation serial links. The panel—populated with experts from systems companies and leading test & measurement equipment suppliers—did a good job of raising and articulating the issues but found no clear solution. When ideas were solicited from the audience, I suggested burning one component pin to offer some indication to the outside world of what the bowels of the IC are really seeing. "No way" was the unanimous answer. "Pins are simply too valuable to burn on a mundane function like that. No one would pay for it. And besides, who could trust those IC guys to indicate the right thing?"

The problems advanced Rx equalization raises for the oscilloscope vendors also affect the EDA industry and the rest of us involved in SI. This makes sense when you realize that signal integrity is in the process of moving from something solved on a PCB to something increasingly performed inside the IC. As such, we can no longer simulate our signal's performance without a much more complex model of the IC. The lowly digital receiver model has transformed itself from clamp curves and die capacitance into a complex DSP engine. And how are we going to model that?

Thankfully, Cadence has been working on this problem for some time now, and was demonstrating something at DesignCon called "algorithmic modeling". Using this technique, IC vendors can compile their Tx/Rx signal processing structures and algorithms in their native formats into executable models for the SI simulator. The models appear as a DLL, and the simulator understands ahead of time how to pass signals in and out of it. This black-box approach is ideal for protecting an IC vendor's intellectual property and its performance at Cadence's demonstration looked good—particularly when you consider the complexity of what's involved.

The real beauty of the Cadence solution is this: in theory, both SI simulators and test & measurement equipment can use the same DLL models. Indeed, both have to attach to the collapsed serial link signal and show you what is actually happening. This added bonus didn't occur to me until the day after the panel discussion. But that's OK—no one else at the panel had figured it out either. We'll all need to take a few picoseconds to think this one through, connect the dots, and iron out the details. But it looks like a good solution.

So we may be on the verge of a new executable modeling format. Once this format is accepted and understood, we will have to wait a bit for the IC vendors, EDA companies, and measurement tool suppliers to implement it. This might not be as hard as you think. In early 1993 I visited all the major EDA vendors to ask if they'd like to participate in what became known as IBIS. It was like putting a match to dynamite. Customer demand had already struck the match, and these companies were more than ready to light the fuse. It needed to happen then, and it likely needs to happen again now. Watch this space.

About the author
Donald Telian is an independent Signal Integrity (SI) Consultant serving the electronics industry around the globe. Building on over 22 years of SI experience at Intel, Cadence, HP, and others, his

recent focus has been on helping customers correctly implement today's Multi-GHz serial links and has published numerous works on the topic. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. Donald can be reached at: telian@sti.net.