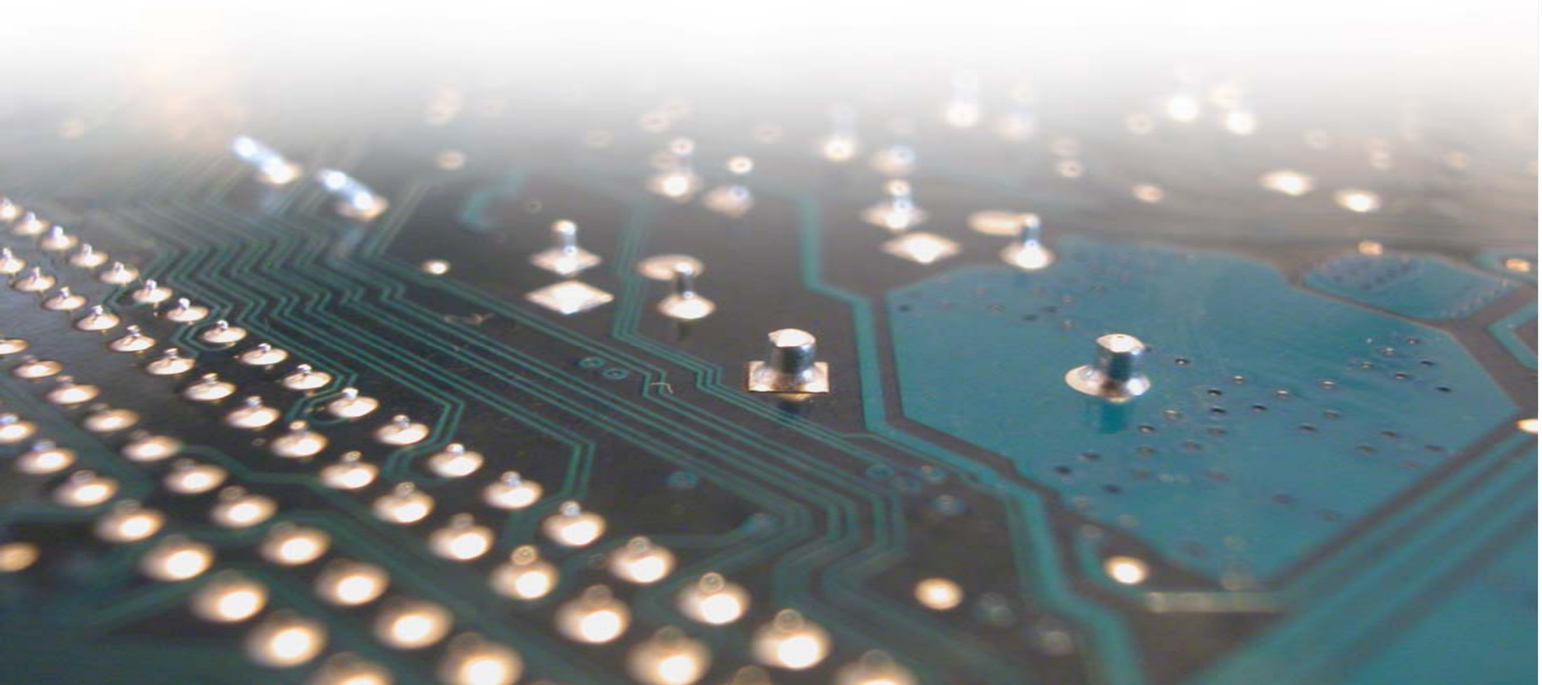
Adapting Signal Integrity Tools and Techniques for 6 Gbps and Beyond

Session 8.3

Donald Telian - SI Consultant



Agenda

- Why Serial Links?
- SI Moving Inside ICs
- Gbit Simulation Today
- Looking Forward

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Agenda

- Why Serial Links?
  - Stubs are Bad
  - Signals are Ugly
  - Gates are Free
- SI Moving Inside ICs
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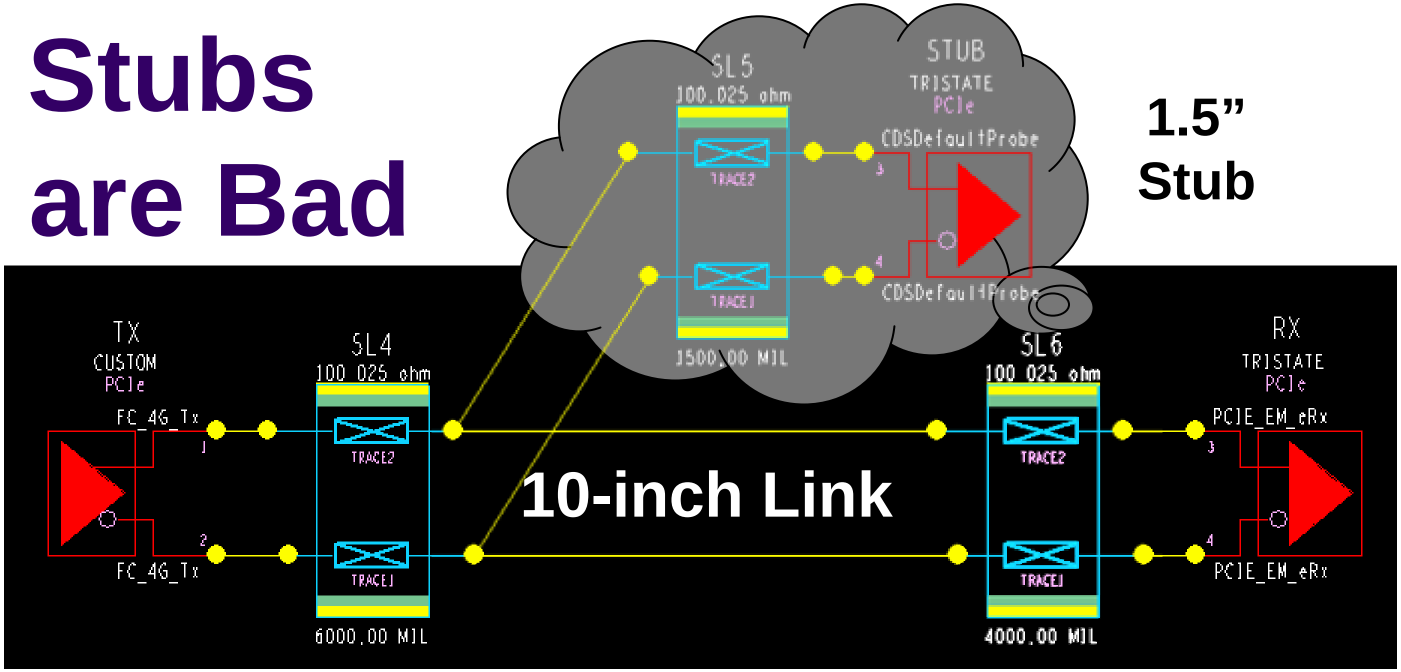
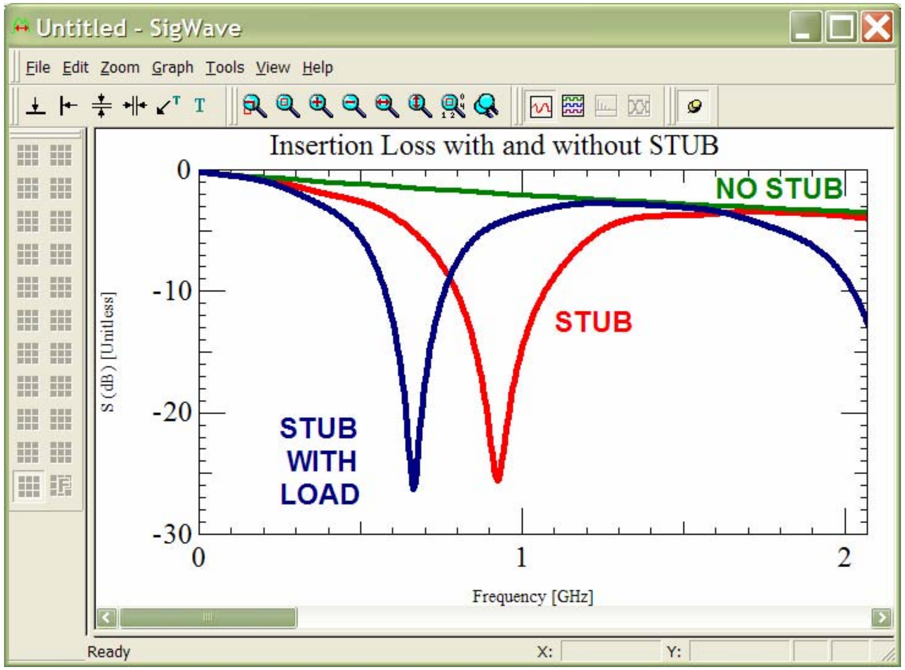
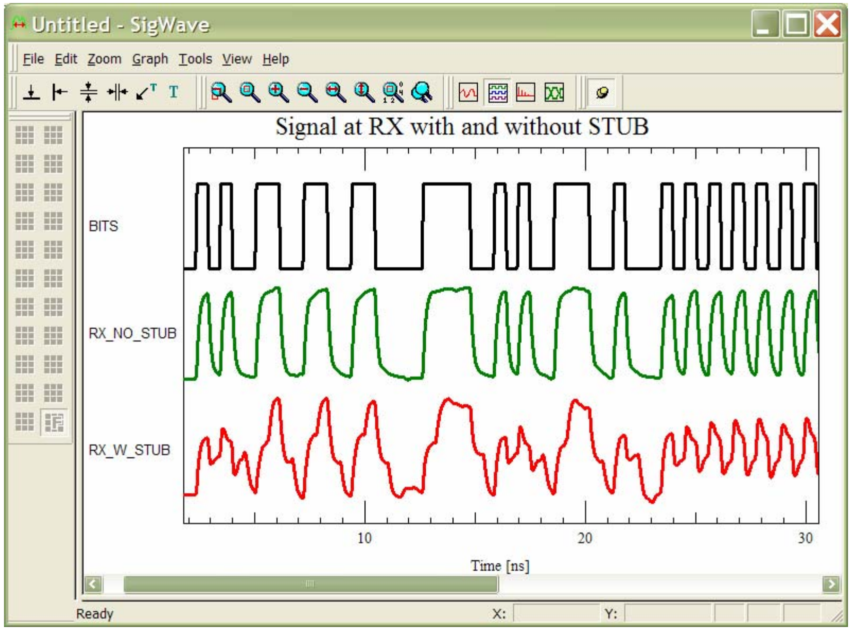
#1: Stubs are Bad







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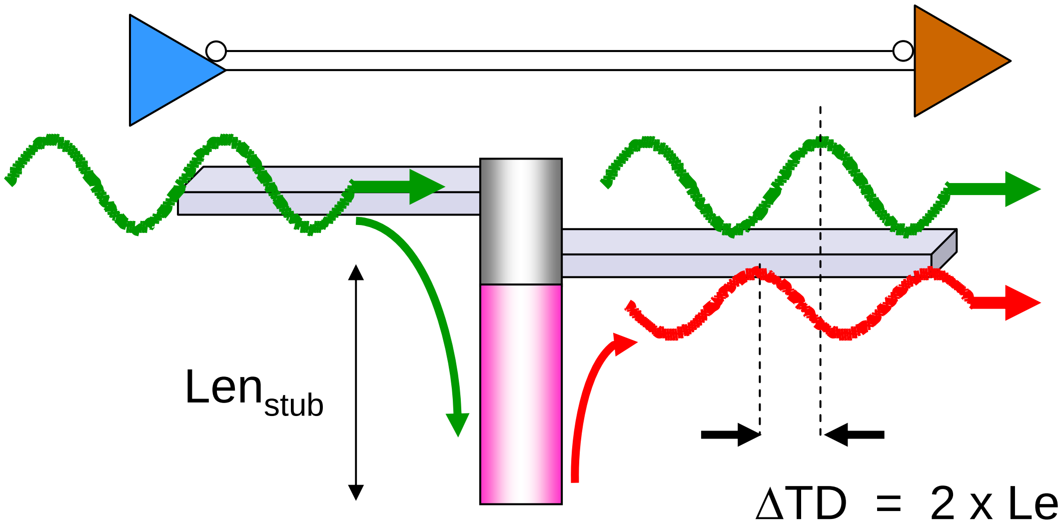
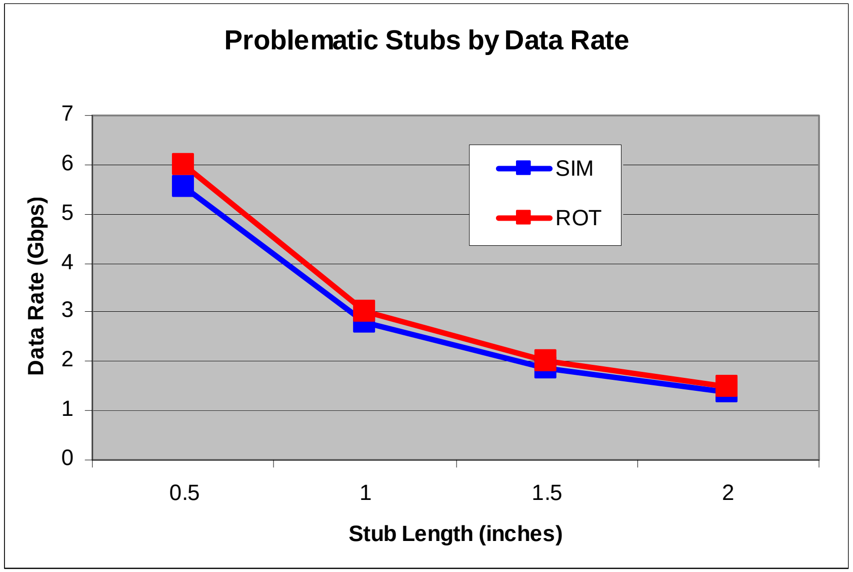
Which Stubs are Bad?



www.BeTheSignal.com
graphics & concepts courtesy Eric Bogatin

$\Delta TD = 2 \text{ x } Len_{stub} / v \;\sim= \; 0.3 \text{ x } Len_{stub}$



Worst Case = ΔTD causes 180º shift, or

Len_{stub} = ¼ wavelength

= ¼ (Vel_pcb / freq)

= ¼ (2*6 in/nS / bit-rate)

Dr. Bogatin's Rule-of-Thumb (RoT):

Bad_Stub ~= 3 / Bit-Rate

Or, OK_Stub ~= 3 / (10*Bit-Rate)
xxx_Stub in inches, Bit-Rate in Gbps

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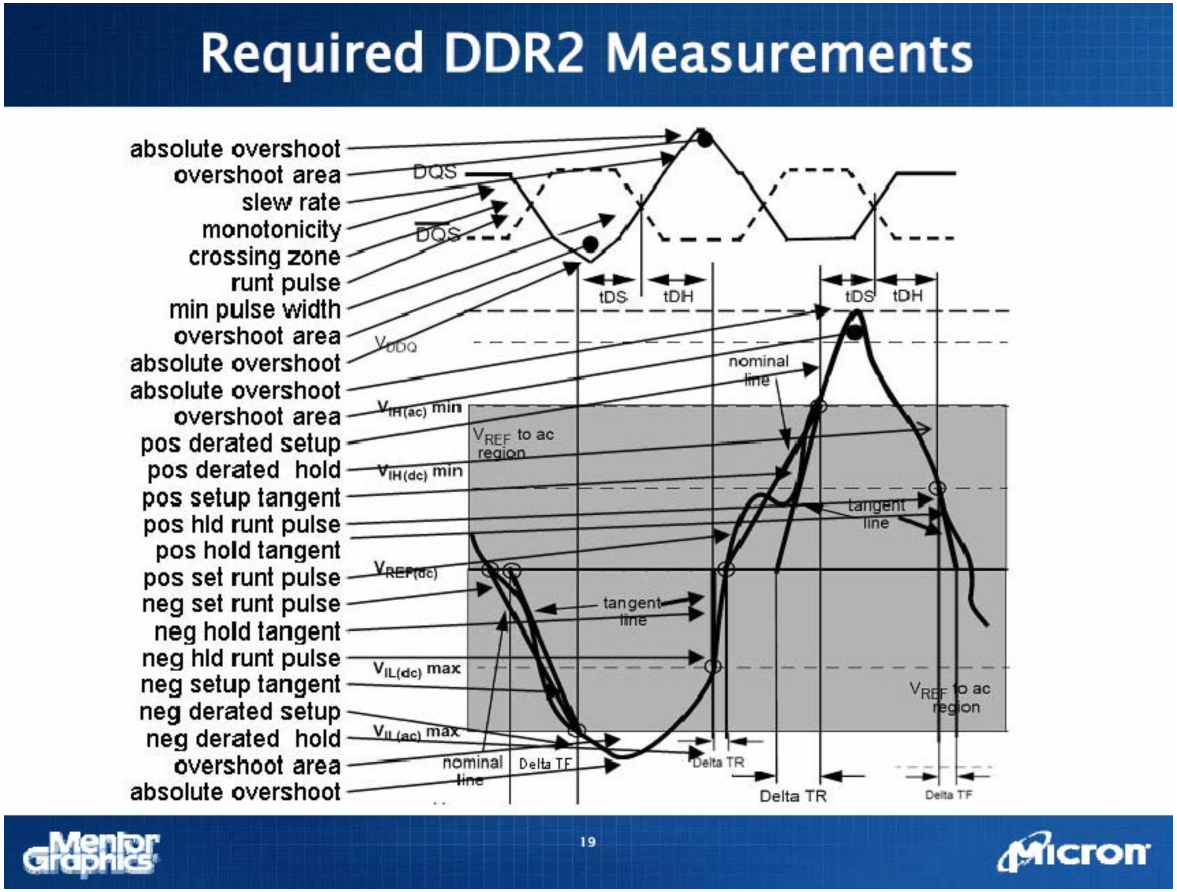
#2: Signals are Ugly



- High-speed signals need post-processing
- Shall we do that during design? …or in silicon?

Receiver's behavior and specifications are sensitive to these effects

Source: "Single Simulation Analysis of a DDR2 Interface in IBIS 4.1" from DesignCon 2007, courtesy Randy Wolff, Micron

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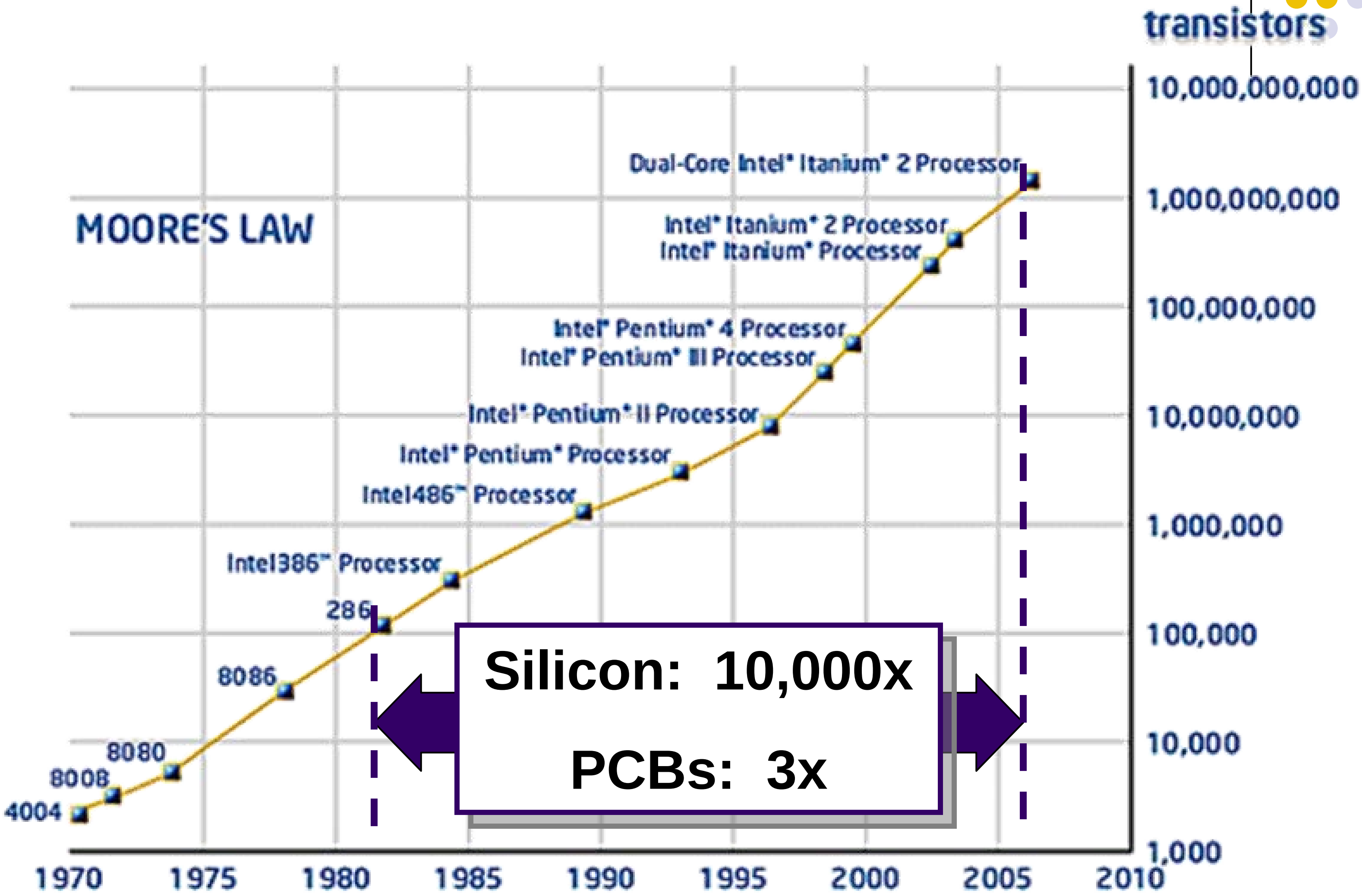
#3: Gates are Free



source: http://www.intel.com/technology/mooreslaw/index.htm

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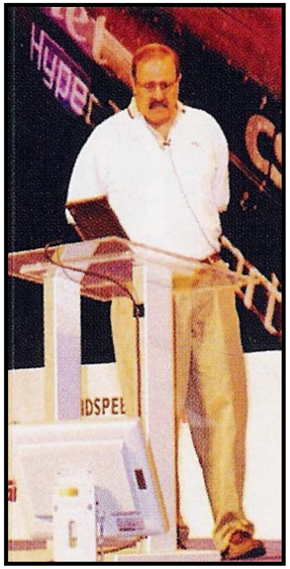
The Turning Point



"We're now at the point where it's getting cheaper to put more gates behind a fast serial line than to lay down copper traces."

Jim Pappas, Intel

– commenting on why PCI Express used serial technology and PCI used parallel – EETimes February 18, 2002 page 92

Traces ⇨ Gates

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Why Serial Links?

- Stubs are Bad
  - Frequency issues arise with stubbed interconnects
    - As early as 400 MHz, see DesignCon 2006 Best Paper
  - The point-to-point nature of serial links removes stubs
- Signals are Ugly
  - Receiving high-speed signals is challenging
  - Serial links use built-in filtering to recover signals
- Gates are Free
  - Surplus silicon has added features to IO transceivers
  - Signal Integrity is moving inside the chip

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Agenda

- Why Serial Links?
- SI Moving Inside ICs
  - Transmitters (Tx)
  - Receivers (Rx)
- Gbit Simulation Today
- Looking Forward

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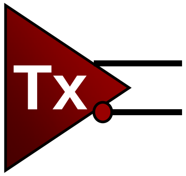
Tx Techniques



- Adapting signal at Tx is simpler than Rx
  - Data pattern is known
- Around 2.5 Gbps “pre-emphasis” was used
  - Sometimes called “de-emphasis” or “2-taps”
- At higher rates, more “taps” are used
  - Some taps before bit, or “pre-cursor”
  - Taps typically spaced by bit times
- Most efficient when Rx signal understood
  - Through simulation, spec boundaries, etc.

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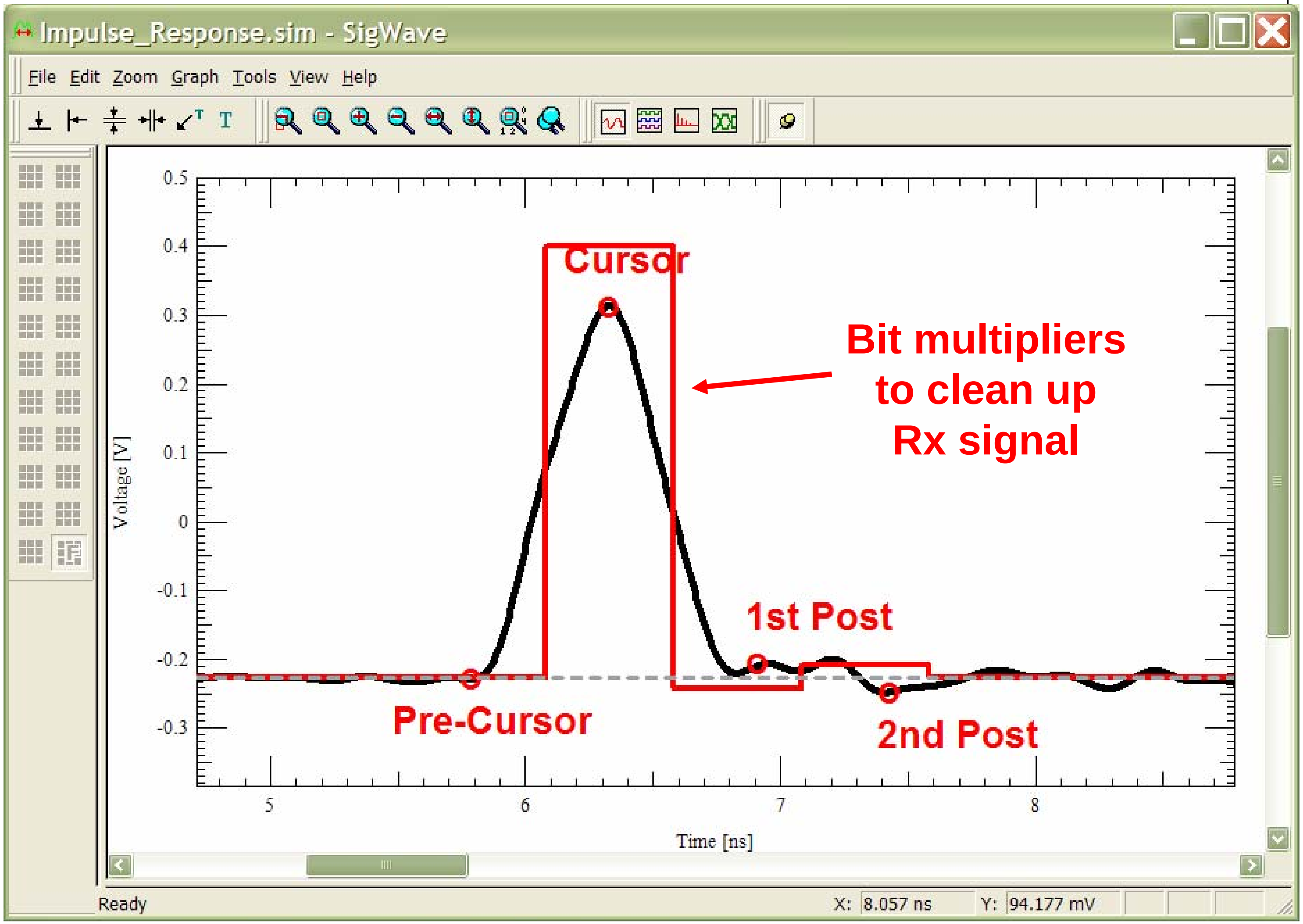
Taps & Impulse Response



- All non-cursor signal causes ISI

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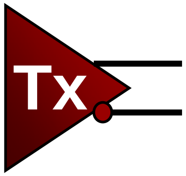
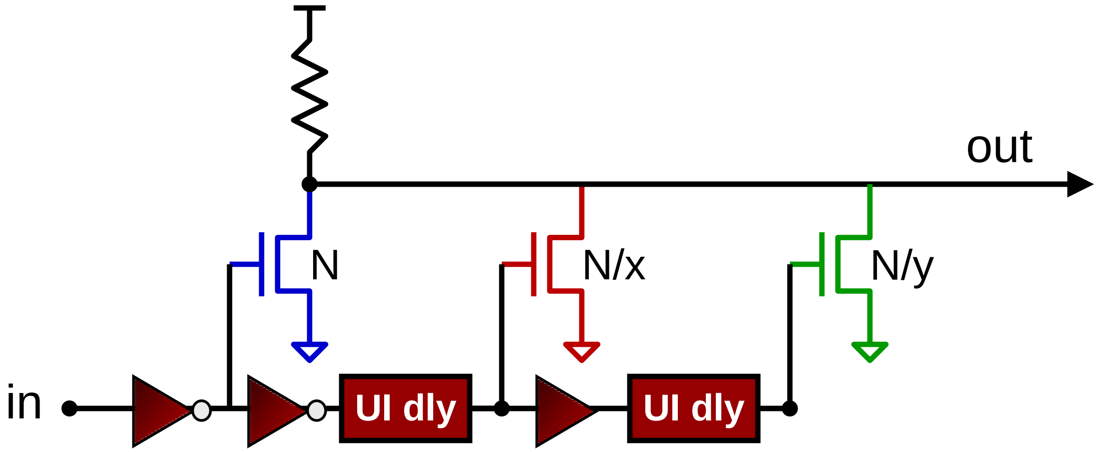
Tx Implementation





- Bit-stream fed directly to SerDes
- For more detail, see Cadence webinar
  - [How to build fast and accurate multi-gigabit transceiver models]

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Rx Techniques

- Rx Equalization (EQ) is more challenging
  - Data pattern is NOT known
  - Signal at Rx has often disappeared
    - typically 20 dB down (10% of signal) at 6+ Gbps
- Primary area of SerDes advances
  - Higher speeds = more creative solutions
  - Techniques increasingly complex and/or non-linear
    - DFE = Decision Feedback Equalization
    - Some are continuously adaptive
    - Implementations inconsistent

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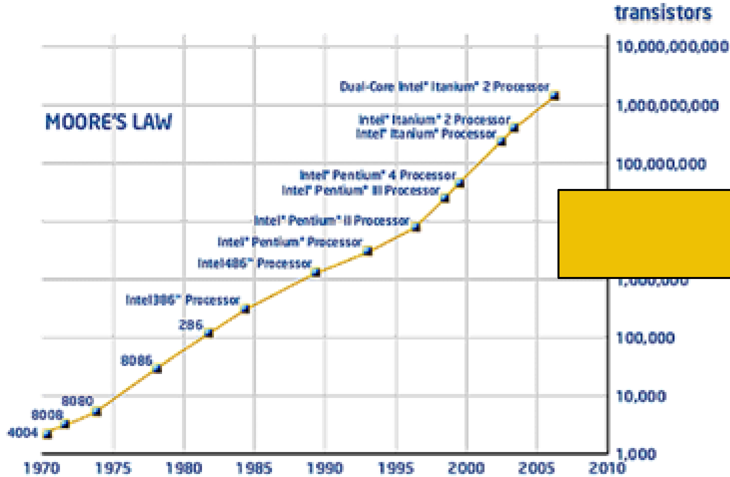
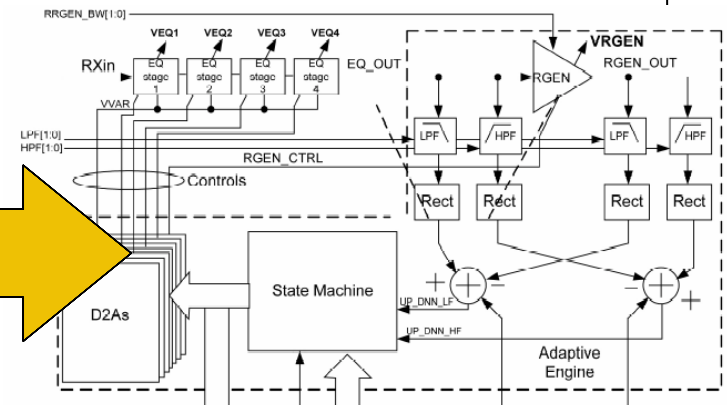
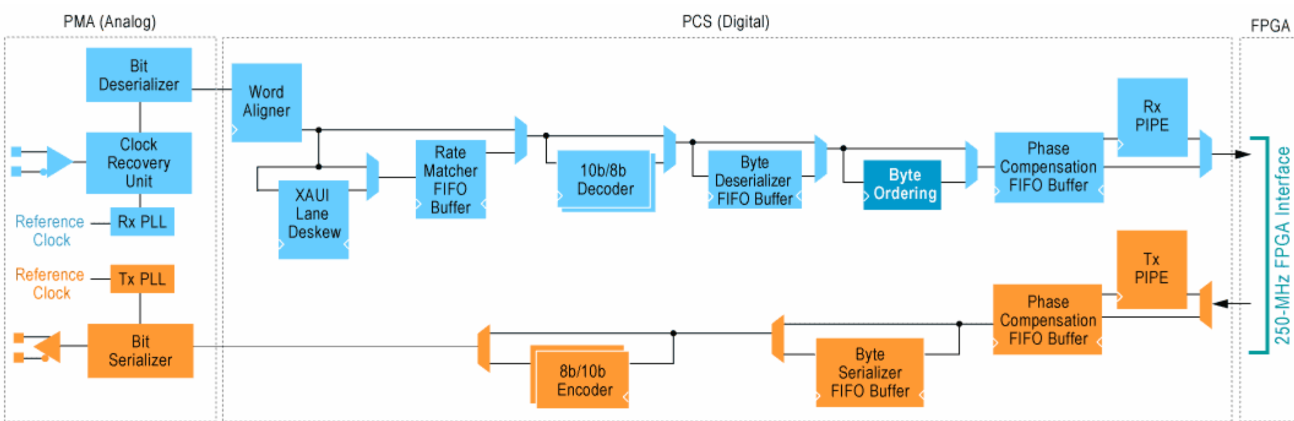
Moore's Law Meets IO Interfacing



source: http://www.intel.com/technology/mooreslaw/index.htm



source: DesignCon 2007 Paper "Digitally Assisted Adaptive Equalizer in 90 nm With Wide Range Support From 2.5 Gbps to 6.5 Gbps" see http://www.altera.com/literature/cp/cp-01026.pdf



source: http://www.altera.com/products/devices/stratix2gx/features/transceiver/s2gx-mgt-transceiver.html

An increasing amount of transistors are consumed by signal transmission

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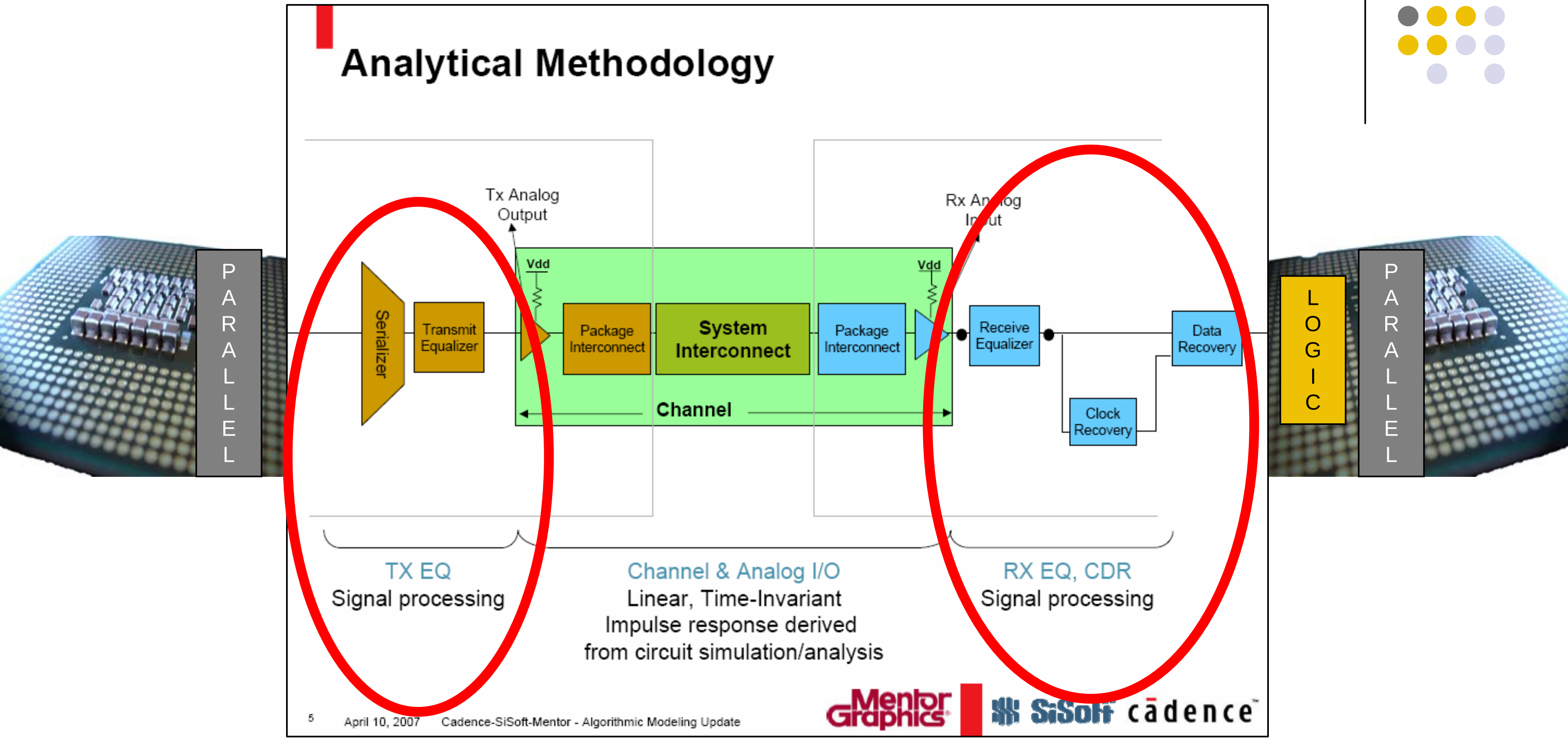
IO = Signal Processing?!



Source: http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20070410/toddwesterhoff/Algorithmic%20Modeling%20BIRD%20-%20Update/IBIS-ATM_Apr10-v3.pdf

- There’s a lot of gates between serial and parallel
- Communications theory has met the digital IO

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Agenda

- Why Serial Links?
- SI Moving Inside ICs
- Gbit Simulation Today
  - Outside the IC
  - Inside the IC
  - Signal Processing
- Looking Forward

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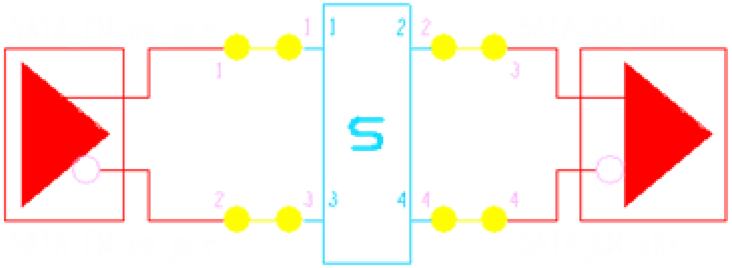
Outside the IC = S-Parameters



- S-params common for passive interconnect
  - Lab characterization covered for absence of tools
  - Generated by both measurement and analysis tools
  - Viewed as better than cascaded discrete models
  - Can read loss directly from S-param plots
  - Format for industry-standard “channels”
- Now handled by most PCB analysis tools
  - Some more mature than others
- Proper fixturing/measurement is challenging
- For more details see Cadence webinar
  - Understanding and Using S-Parameters for PCB Signal Integrity

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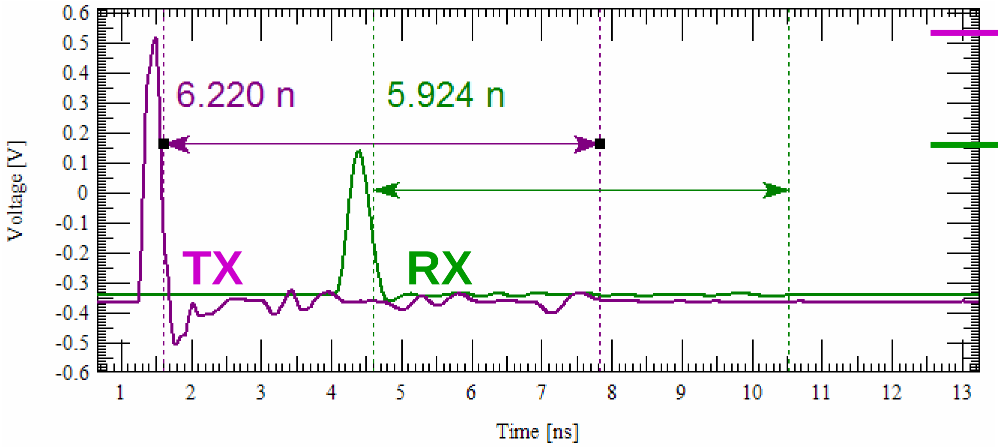
The Impulse Response



Rx ~60% of Tx, or ~ -5dB loss

ISP ~6 nS => #bits to sim =

2^(6*2.5) = 2^15 = 30k (2.5Gbps)

2^(6*3.125) ~= 500k (3.125 Gbps)

- System interconnect's "fingerprint"
- Reveals Tx to Rx "loss" (similar to eye or S_21)
- Reveals "Interconnect Storage Potential (ISP)"
  - From which we can determine # bits to simulate
  - ISP detailed in Intel/Cadence DesignCon 2005 paper "New Techniques for Designing and Analyzing Serial Links"
- Used in "high-capacity" simulators

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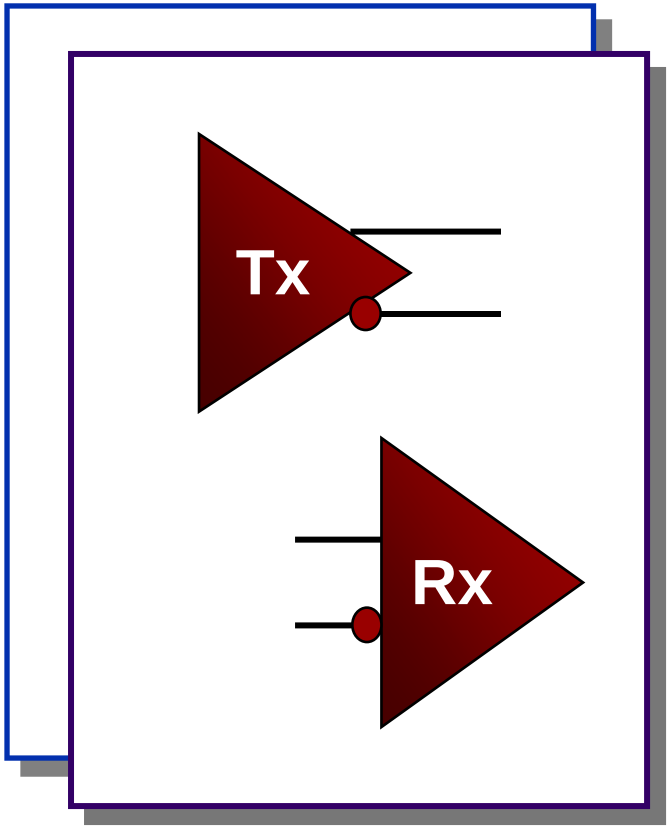
Understanding Analog Tx/Rx

- The simple IO had a set of characteristics
  - VI, T_rf (VT), C_comp
- And the differential Tx and Rx do too
  - V_swing, T_rf, V_cm, R_term, Pre-emp%, Cpad
- Same Tx/Rx handles multiple standards
  - Excessively programmable



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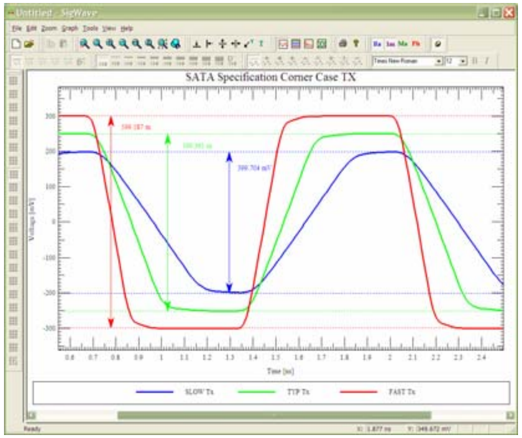
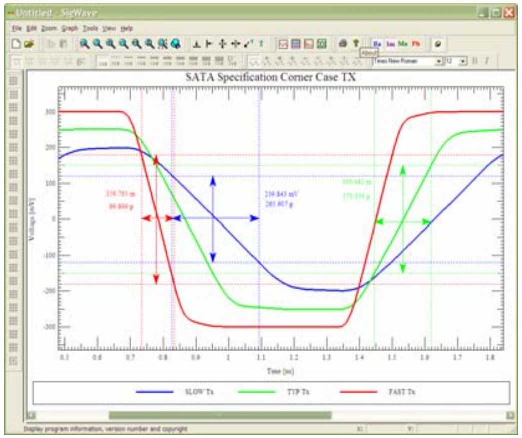
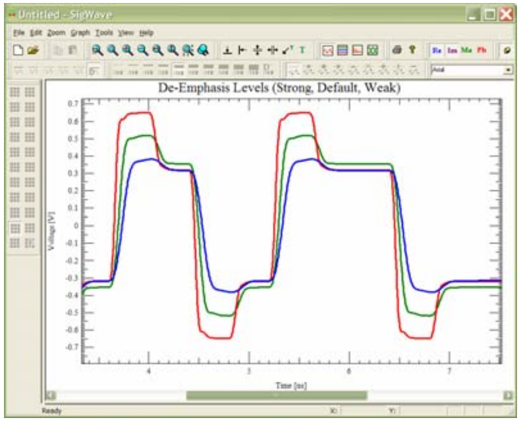
Using "Spec" Models

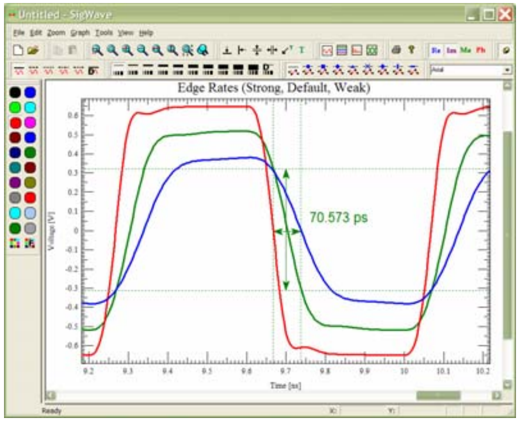
SATA Spec
Voltage Swing &
Edge Rates





~PCI Express
Voltage Swing &
Edge Rates





- Craft from base set of parameters in Specs
- Set of model templates at this link

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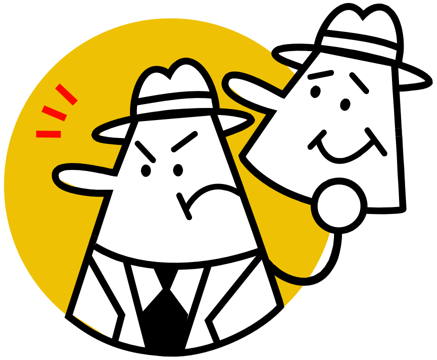
Beyond Analog Tx/Rx ~ Modeling Signal Processing

- Tools and models exist within IC companies
  - Used for IC architecture and design
- Excessively proprietary
- In some cases they're offered to customers
  - Support issues
  - Maintenance issues
- THE BIG ISSUE
  - Require same IC (vendor) on both ends of the link



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Interoperability Challenge

- Must simulate models from different vendors
- It happened once before with “IBIS”
  - Early ’90s many IBIS-like SI simulators emerged
  - Plug n Play SI required consistent model format
  - IBIS was born
- Once again the leaders are deriving a format
  - Executable “Algorithmic Models” contained in DLLs
  - All work in public domain done by IBIS-ATM
    IBIS Advanced Technology Modeling Task Group

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Towards Interoperability

IBIS-ATM SerDes Task Group

- Goal: SerDes Rx/TX model interoperability
  - Multiple EDA platforms
  - Multiple SerDes vendor models
  - Protect SerDes vendor IP
- IBIS-ATM committee participation
  - EDA: Agilent, Cadence, Mentor, SiSoft
  - Semiconductor: IBM, Intel, Micron, ST-Micro, TI, Xilinx
  - System: Cisco
- Two part modeling standard
  - Characterization model: existing IBIS syntax models TX / RX analog characteristics
  - Algorithmic model: equalization, clock recovery, device optimization algorithms

Slide courtesy IBIS-ATM Group and Todd Westerhoff: http://www.vhdl.org/pub/ibis/summits/sep07/

- IBIS-ATM: http://www.vhdl.org/pub/ibis/macromodel_wip/

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Proposed Analysis Flow

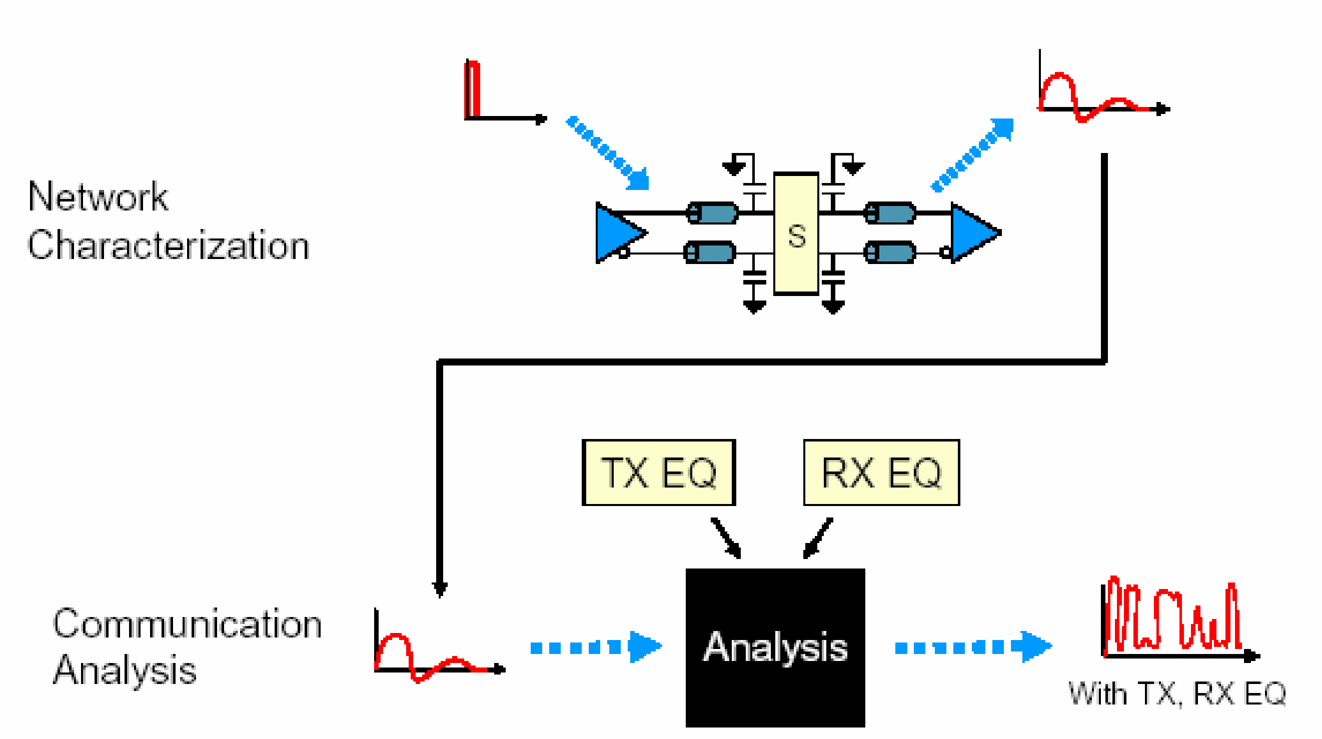

Image courtesy IBIS-ATM Group and Todd Westerhoff: http://www.vhdl.org/pub/ibis/summits/sep07/

Circuit Analysis with Existing Models

Algorithmic Models

- Algorithmic models typically implemented in .dll files

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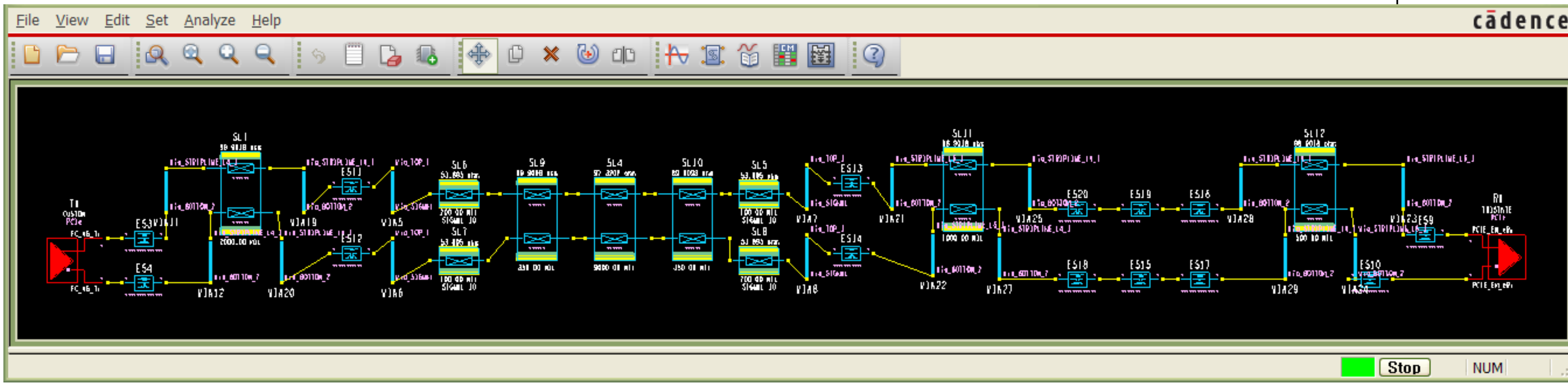
Algorithmic Models Within Cadence Flow

cadence



- Algorithmic models fit within existing MGH flow
  - Invoked as part of Channel Analysis, some scripts etc.
- Cadence demo'd in Jan07, released in 16.0
- Tx/Rx macromodels contain "ami" portion
  - Includes path to dll file and settable parameters
- Cadence working towards industry standardization
  - Within IBIS domain (proprietary solution for now)

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Industry Standardization

IBIS-ATM Status

- Original proposal submitted by Cadence & IBM
  - Current version authored by Cadence, Mentor, SiSoft
- First draft of BIRD approved by IBIS-ATM task group for prototype model & EDA platform development
  - Prove interoperability & refine proposal before bringing back to IBIS Open Forum
- Subcommittee work, presentations & BIRD available on-line:
  - http://www.vhdl.org/pub/ibis/macromodel_wip/
- Public TX/RX models, modeling "toolkits" will be available

Status courtesy IBIS-ATM Group and Todd Westerhoff: http://www.vhdl.org/pub/ibis/summits/sep07/

- Achieved model/EDA interoperability in Aug 2007
- Updated proposal (BIRD) for ATM approval ~Sep/Oct 2007
- …and then on to IBIS committee approval and release

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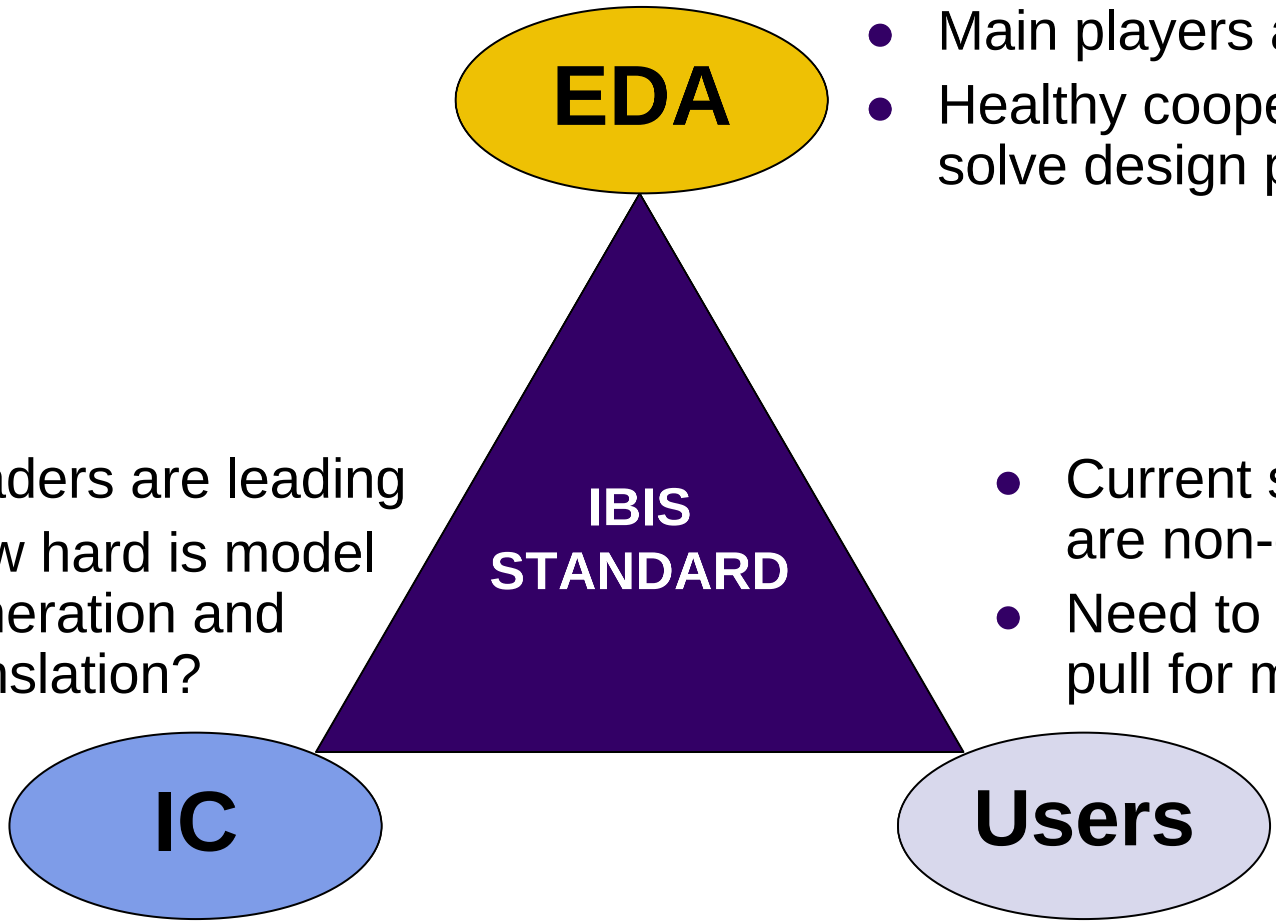
SerDes SI into Mainstream



- Main players are there
- Healthy cooperation to solve design problems

- Leaders are leading
- How hard is model generation and translation?

- Current solutions are non-optimal
- Need to create pull for models

Pieces are coming into place to enable push past 6 Gbps

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Existing Solutions

- IBM offers Algorithmic Models for their 6 Gbps and 11 Gbps SerDes NOW
  - Operates within Allegro PCB SI 16.0
  - Available only to IBM customers
    - Contact your local IBM representative to obtain models

- IBIS-ATM group released AMI model Eval Toolkits
  - Visit the Work Archive at: http://www.vhdl.org/pub/ibis/macromodel_wip/

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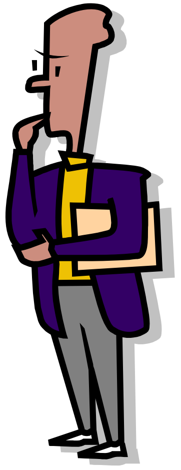
In Summary

- Serial links dominate for higher speeds
- Signal integrity moving inside chips
- Models, methods, metrics changing
- SerDes now do signal processing
- Interoperable models an issue
- Cadence/others driving a solution
- Algorithmic models coming into place



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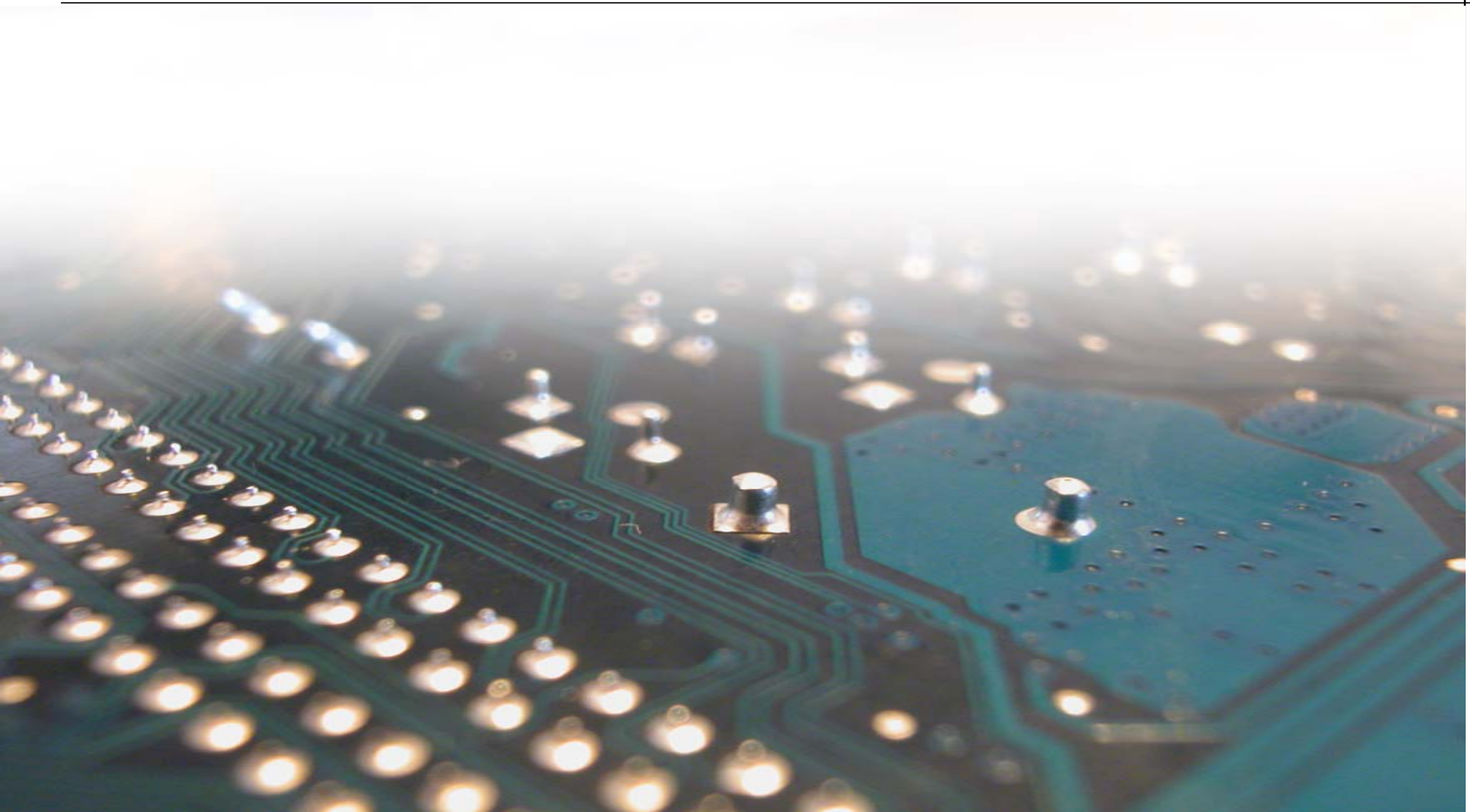
THANK YOU



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