New Serial Link Simulation Process, 6 Gbps SAS Case Study

Donald Telian – SI Consultant
About the Authors

Donald Telian is an independent Signal Integrity Consultant. Building on 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today’s Multi-GHz serial links. He has published numerous works on this and other topics. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. Donald can be reached at: telian@sti.net

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Ravinder Ajmani is a Senior Engineer with Hitachi GST. He has over 15 years of experience on High-speed PCB Design, Signal integrity, and Electromagnetic Compatibility. During this period he has worked on several generations of disk drive products, and resolved numerous design and customer integration issues with these products. Ravinder can be reached at: ravinder.ajmani@HitachiGST.com

Kent Dramstad is an ASIC Application Engineer at IBM. He has over 27 years of experience working on both power and signal integrity issues for a wide variety of applications. His current emphasis is on helping customers select and integrate IBM’s series of High Speed Serdes (HSS) cores into their ASIC designs. Kent can be reached at: dramstad@us.ibm.com

Adge Hawes is a Development Architect for IBM at its Hursley Labs, United Kingdom. He has worked for IBM for more than 30 years across such hardware as Graphic Displays, Printing Subsystems, PC development, Data Compression, and High-Speed Serial Links. He has represented the company in many standards bodies such as PCI, SSA and Fibre Channel. Recently he has moved from Digital Logic to Analog and Mixed-Signal, where he develops simulators for IBM's High Speed Serial Link customers. Adge can be reached at: adge@uk.ibm.com
Agenda

- Intro to Project, Tools, & Technologies
- Verifying SAS Spec Compliance
- Virtual Systems Analysis
- Conclusions
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About the Project

- **Identify and implement new simulation environment for future 6+ Gbps Hard Disk Drive (HDD) designs**
- **Prove-in environment on design of future products**
- **6 Gbps Challenges**
  - Loss ~20dB (10% of Tx signal at Rx)
  - Rx signal un-measurable
  - Complex equalization schemes
  - New model formats (AMI)
  - New simulation techniques
  - New modeling standards emerging
  - Spec compliance requires simulation
- **Coordinate ~15 key industry players**
  - Customers, suppliers, tool vendors, standards committees
Project Phases

- Assessment
- Proof-of-Concept
- Model Development
- System Analysis
- Kit Environment

- ~ 6-month Effort
Terminology

- SAS = Serial Attached SCSI
- Serial Link = Channel
- Channel Analysis = Serial Link Simulation
- CA = Channel Analysis = simulation tool
- DFE = Decision Feedback Equalization = Rx Eq
- FFE = Feed-Forward Equalization = Tx Eq
- SerDes = IBM 6 Gbps core, in this case
- AMI = Algorithmic Modeling Interface
AMI Model Review

- Algorithmic models typically implemented in .dll files
- AMI format approved by IBIS Committee in Nov. ’07
- More background see: CDNLive! 2007 Session 8.3

Image courtesy IBIS-ATM Group and Todd Westerhoff: http://www.vhdl.org/pub/ibis/summits/sep07/
Hard Disk Drive Model

HDD model used with both compliance and system loads
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SAS Compliance Testing

- **Tx**
  - HDD
  - RTTL (Reference Transmitter Test Load)
  - Reference Rx (3-tap DFE)
  - Measure eye after Rx DFE

- **Rx**
  - Reference Tx (2-tap FFE)
  - Rx Stress Circuit
  - Measure S-Parameters at PCB edge
  - HDD

- **Port**
  - HDD
  - Measure S-Parameters at PCB edge

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**Legend:**
- HDD
- RTTL
- Reference Rx
- Rx Stress Circuit
- Reference Tx
- Rx DFE
- 2-tap FFE
- 3-tap DFE
- Reference Transmitter Test Load
- Measure S-Parameters at PCB edge
Tx Compliance Testing

- Simulation specified as only way to validate
  - Eye measured inside IC at output of Rx DFE
  - Spec calls out Reference Rx 3-tap LMS DFE
- Transmit through -15dB “RTTL” S-parameters
Tx RTTL Simulation Results

- 4 taps configured in Tx, noise channel active
- Tx set at spec reference levels (nominal EQ)
- Height/width = 179mV/0.41UI (100/0.40 spec)
- Comfortable with small margin on width
Rx Compliance Testing

- Rx stress testbench implemented in *simulation* environment
- Delivered crosstalk, loss, eye w/h, from Reference Tx as specified
Rx Stress Test Results

- Two HDD route styles tested
  - 100 Ohm microstrip
  - 85 Ohm stripline
- Eye height & width measured at 1e15 bits
  - height extrapolated
- Derive design margins
- Guide design choices

<table>
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<th>Parameter</th>
<th>o100</th>
<th>i85</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Eye Height (1e6 bits)</td>
<td>108</td>
<td>131</td>
<td>mV</td>
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<tr>
<td>Eye Height Margin (60mV - 10%)</td>
<td>37</td>
<td>58</td>
<td>mV</td>
</tr>
<tr>
<td>Eye Width (1e15 bits)</td>
<td>0.408</td>
<td>0.418</td>
<td>UI</td>
</tr>
<tr>
<td>Margin in UI (target = 0.2 UI min)</td>
<td>0.208</td>
<td>0.218</td>
<td>UI</td>
</tr>
<tr>
<td>Margin in pS</td>
<td>35</td>
<td>36</td>
<td>pS</td>
</tr>
</tbody>
</table>
S-Parameter Limit Compliance

- Differential nets extracted for virtual VNA measurement
- Plot SDD, SCC, SCD against specified limits (in red)
- All measurements below limits
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System Configuration Testing

- **TYP**
  - Reference Tx & Rx
    - 4” PCB: CON
    - 8” backplane with vias: CON
    - HDD

- **WC1**
  - Reference Tx & Rx
    - 4” PCB: CON
    - 16” backplane with vias: CON
    - HDD

- **WC2**
  - Reference Tx & Rx
    - 4” PCB: CON
    - 16” cable & 2 conns: CON
    - 6” PCB: CON
    - 10” backplane with vias: CON
    - HDD
System Configuration Metrics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TYP</th>
<th>WC1</th>
<th>WC2</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>PCB &amp; Cable Length</td>
<td>13</td>
<td>21</td>
<td>37</td>
<td>inches</td>
</tr>
<tr>
<td># of Connectors</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>#</td>
</tr>
<tr>
<td># of Vias</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>vias</td>
</tr>
<tr>
<td>Propagation Time</td>
<td>2.5</td>
<td>4</td>
<td>6</td>
<td>nS</td>
</tr>
<tr>
<td>6 Gbps bits in channel</td>
<td>15</td>
<td>24</td>
<td>36</td>
<td>bits</td>
</tr>
<tr>
<td>Channel Loss (SDD21 @ 3 GHz)</td>
<td>-8.9</td>
<td>-13.6</td>
<td>-16</td>
<td>dB</td>
</tr>
</tbody>
</table>

- Apply experience to augment spec’s coverage
- Acquire intuitive sense of what works, what doesn’t
- Wide range of length, loss, discontinuities
- Drive with minimal Tx, recover signal with IBM DFE
# 7-Step Link Analysis Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Task</th>
<th>Purpose</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Collect &amp; Connect Models</td>
<td>Build Link Model</td>
<td>Link Ready-to-Run</td>
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<tr>
<td>2</td>
<td>Model Sanity Check</td>
<td>Verify Model</td>
<td>TD Functional</td>
</tr>
<tr>
<td>3</td>
<td>Quantify Loss &amp; Crosstalk</td>
<td>Understand &amp; Gauge Link</td>
<td>S21 dB, mV RMS</td>
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<tr>
<td>4</td>
<td>Plot Impulse Response &amp; ISP</td>
<td>Measure ISP, Calculate #bits</td>
<td>#bits for CA</td>
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<tr>
<td>5</td>
<td>Verify Eye Convergence</td>
<td>Test #bits, Confirm Coverage</td>
<td>CA Functional</td>
</tr>
<tr>
<td>6</td>
<td>Parameter Determination</td>
<td>Setup for Worst-Case</td>
<td>CA Parameters</td>
</tr>
<tr>
<td>7</td>
<td>Corner Case Analysis</td>
<td>Derive Design Margins</td>
<td>Eye h/w Margins</td>
</tr>
</tbody>
</table>

*Illustrate on WC1 channel (TYP & WC2 in paper)*

*Can be applied to any serial link SI analysis*
Step 1: Collect & Connect Models
Step 2: Model Sanity Check

CtlrTx/Rx – 4” trace – Conn – BpVia – 16” tr – BpVia – Conn – 100Ohm 1” mstrip trace – Pkg – IBM Tx/Rx

Voltages, System Loss, Time Delay Reasonable

Short TD Eye at Rx Input Mostly Collapsed

Typical CA Eye Re-opened, Rx DFE Functioning
Step 3: Quantify Loss & Crosstalk

**S21 for WC1 Rx Channel**

- Total Loss = $2 \times BpVia + 2 \times CdVia + 2 \times Conn + 21'\times 0.33\text{dB/inch} + \text{Misc}$
  
  Hand Calculation = $2 \times 1 + 2 \times 0.3 + 2 \times 1 + 21/3 + 2 = 13.6\text{dB}$

**Crosstalk on Quiet Channel, 6mV rms**

- Crosstalk = 5.6 mV rms
Step 4: Plot Impulse Response & ISP
Step 5: Verify Eye Convergence

- Impulse Response shows noise to ~8nS
- Interconnect Storage Potential (ISP) = 1.6 nS
- Bit affected by 10 bits previous (1 symbol)
- Eye converges ~1e5 bits
- #bits parameter for CA
- ISP defined in [this paper](http://www.t11.org/ftp/t11/pub/fc/fcsm2/05-215v0.pdf)
### Step 6: Parameter Determination

<table>
<thead>
<tr>
<th>#</th>
<th>Variable</th>
<th>Influences</th>
<th>Source</th>
<th>Value</th>
<th>Unit</th>
<th>Apply In</th>
<th>Notes</th>
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<tbody>
<tr>
<td>1</td>
<td>Tx Swing</td>
<td>Eye shape</td>
<td>SAS Spec Table 61</td>
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<td>Tx De-emp</td>
<td>Eye shape</td>
<td>SAS Tables 64 65</td>
<td>-2</td>
<td>dB</td>
<td>Tx Model</td>
<td>Ref Tx value</td>
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<td>3</td>
<td>Bit Pattern</td>
<td>Jitter, Eye</td>
<td>SAS Spec, etc</td>
<td>CJTPAT</td>
<td></td>
<td>CA Form</td>
<td></td>
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<tr>
<td>4</td>
<td>Dj</td>
<td>Eye, B-tub</td>
<td>Tx Parameter</td>
<td>23.4</td>
<td>pS p-p</td>
<td>chsim.clm</td>
<td>= 0.14% UI</td>
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<td>5</td>
<td>Rotator Linearity</td>
<td>Eye, Bathtub</td>
<td>AMI Model Kit</td>
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<td>file</td>
<td>Rx model</td>
<td>pr_fast.dat a bit better</td>
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<tr>
<td>6</td>
<td>On-chip Params</td>
<td>Eye shape</td>
<td>AMI Model Kit</td>
<td>0</td>
<td></td>
<td>Tx/Rx models</td>
<td>enabled</td>
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<tr>
<td>7</td>
<td>Rj</td>
<td>Eye, B-tub</td>
<td>Tx Parameter</td>
<td>1.4</td>
<td>pS rms</td>
<td>CA Form</td>
<td>= 0.84% UI</td>
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<td>8</td>
<td>Duty Cycle Dist.</td>
<td>Eye shape</td>
<td>Tx Parameter</td>
<td>0.05</td>
<td>UI</td>
<td>CA Form</td>
<td>Use 45 as HI%</td>
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<tr>
<td>9</td>
<td>Pj Magnitude</td>
<td>Jitter, Eye</td>
<td>AMI Model Kit</td>
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<td>UI</td>
<td>CA Form</td>
<td>Enter as 0.05</td>
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<tr>
<td>10</td>
<td>Pj Cycles/UI</td>
<td>Jitter, Eye</td>
<td>AMI Model Kit</td>
<td>0.01</td>
<td>UI</td>
<td>CA Form</td>
<td>Enter as 0.01</td>
</tr>
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- Extract from specs for worst-case analysis
- Unlike standard SI (has wc parameters in models)
Step 7: Corner Case Analysis

- **Width**: corner (red) decreases significantly to 0.25 UI
- **Height**: must derate to 1e15 (155 mV)
- **Margin**: 95mV/0.05UI against 60mV/0.20UI targets
Margins for All Systems

- Margins at 1e15 per SAS spec
- IBM Rx DFE Handles all Cases
- WC2 Margins Approaching Limit

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<tr>
<td>Crosstalk</td>
<td>9.1</td>
<td>5.6</td>
<td>7.4</td>
<td>mV rms</td>
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<tr>
<td>ISP</td>
<td>1.5</td>
<td>1.6</td>
<td>2.1</td>
<td>nS</td>
</tr>
<tr>
<td>#bits for Coverage</td>
<td>1e4</td>
<td>1e5</td>
<td>1e5</td>
<td>bits</td>
</tr>
<tr>
<td>Corner Eye Height (1e6 bits)</td>
<td>244</td>
<td>172</td>
<td>103</td>
<td>mV</td>
</tr>
<tr>
<td>Eye Height Margin (60 mV -10%)</td>
<td>160</td>
<td>95</td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>Typ Eye Width (1e6 bits)</td>
<td>0.72</td>
<td>0.59</td>
<td>0.52</td>
<td>UI</td>
</tr>
<tr>
<td>Corner Case Width (1e15 bits)</td>
<td>0.34</td>
<td>0.25</td>
<td>0.218</td>
<td>UI</td>
</tr>
<tr>
<td>Margin in UI (to 0.20UI target)</td>
<td>0.14</td>
<td>0.05</td>
<td>0.018</td>
<td>UI</td>
</tr>
<tr>
<td>Margin in pS</td>
<td>24</td>
<td>9</td>
<td>3</td>
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Key Learnings

- HDD implementation has margin against all tests, IBM SerDes performing well
- Worst-case margins become questionable around -16dB, typical channels <= -10dB
- 6 Gbps sim environment with AMI models now functional, performance meets expectations
- Environment enables compliance testing that previously required physical hardware
In Summary

- Serial link frequencies continue to increase
- Specs require virtual probing inside IC
- AMI models are starting to appear
- Simulation environment functional
- A process for link SI described
- Refer to paper for complete details
THANK YOU