Advanced Techniques for Channel Analysis

Donald Telian – SI Consultant – Siguys.com

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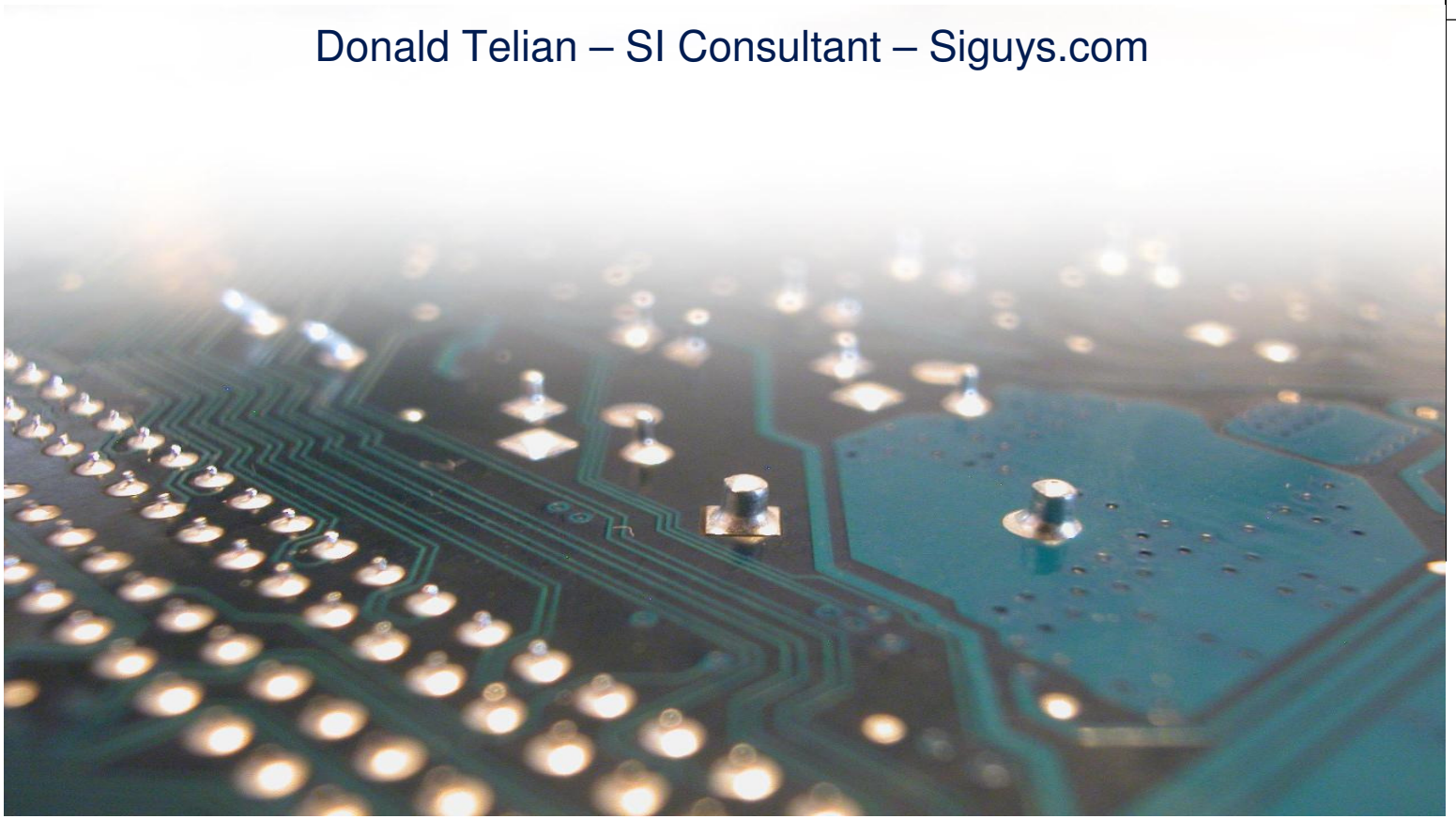

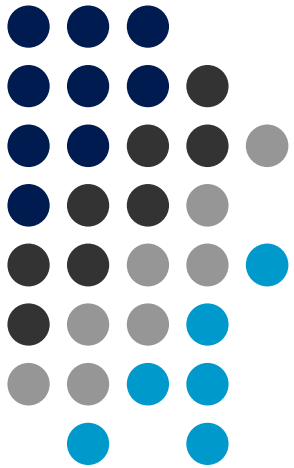

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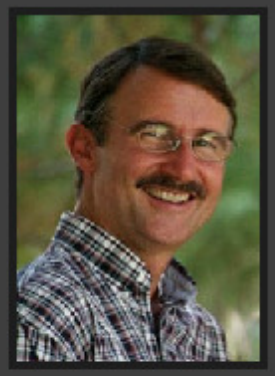

Donald Telian

Donald Telian has been in the Signal Integrity field for 25 years, and is now serving as an independent Signal Integrity Consultant. Building on many years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-GHz serial links. He has published numerous works on this and other topics. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. Donald can be reached at: telian@siguys.com

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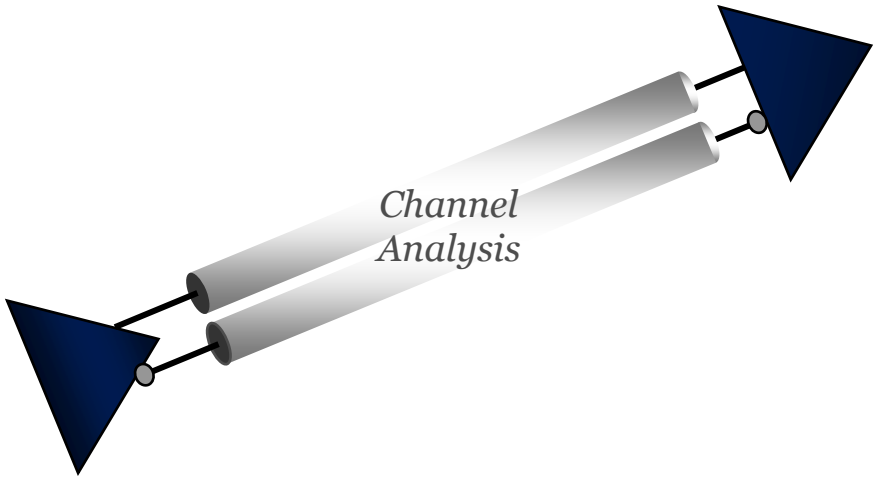
Agenda

How to Perform Channel Analysis (CA)…

- Faster
- Better
- Deeper



The Basics

- Channel Analysis (CA)
  - 1st introduced mid-2004
  - High-capacity (ie, millions of bits) simulator
  - Used to analyze multi-gigabit (1+ Gbps) serial links
  - Works with S-parameters, 3D vias, AMI, Hspice… models
- Siguys has used CA on dozens of links
  - PCIe, SATA, SAS, QPI, FC, SFI, XAUI, etc., 1-10 Gbps
- We'll focus on tips for using CA in practice
  - This is advanced material, not introductory
  - Assumes familiarity with the tools

To Lean More

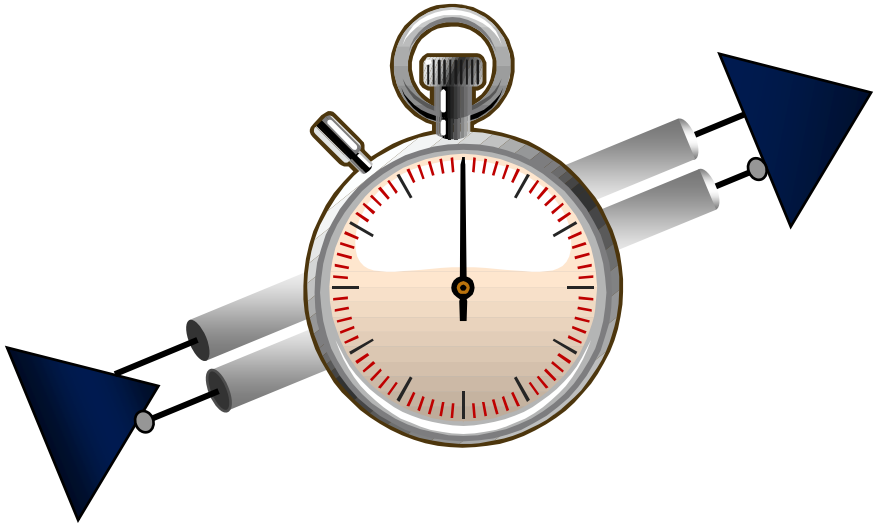
- Get up-to-speed at siguys.com/published.html
  - Intro to CA, S-parameters, SerDes modeling
  - CA papers applied to PCIe, SAS, SATA, etc

- Lean more at Advanced CA Training Course
  - Full-day advanced CA training
  - Contact Siguys for more info

- Visit DesignCon® 2010
  - Feb 1-4 2010
  - Siguys/Ericsson/Amphenol 6+ Gbps paper 7-TA4

Agenda

- Faster
  - Working around “the modeling issue”
  - The time-step two-step
- Better
- Deeper



SI Engineer's Creed

I will never fail to produce meaningful data
because I do not have a model

It's better to have
data with 10% accuracy in an hour than
data with 5% accuracy in a month

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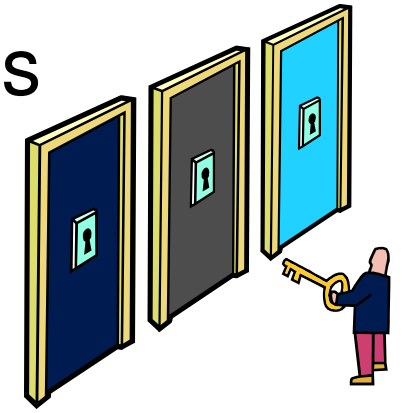
SerDes Model Options

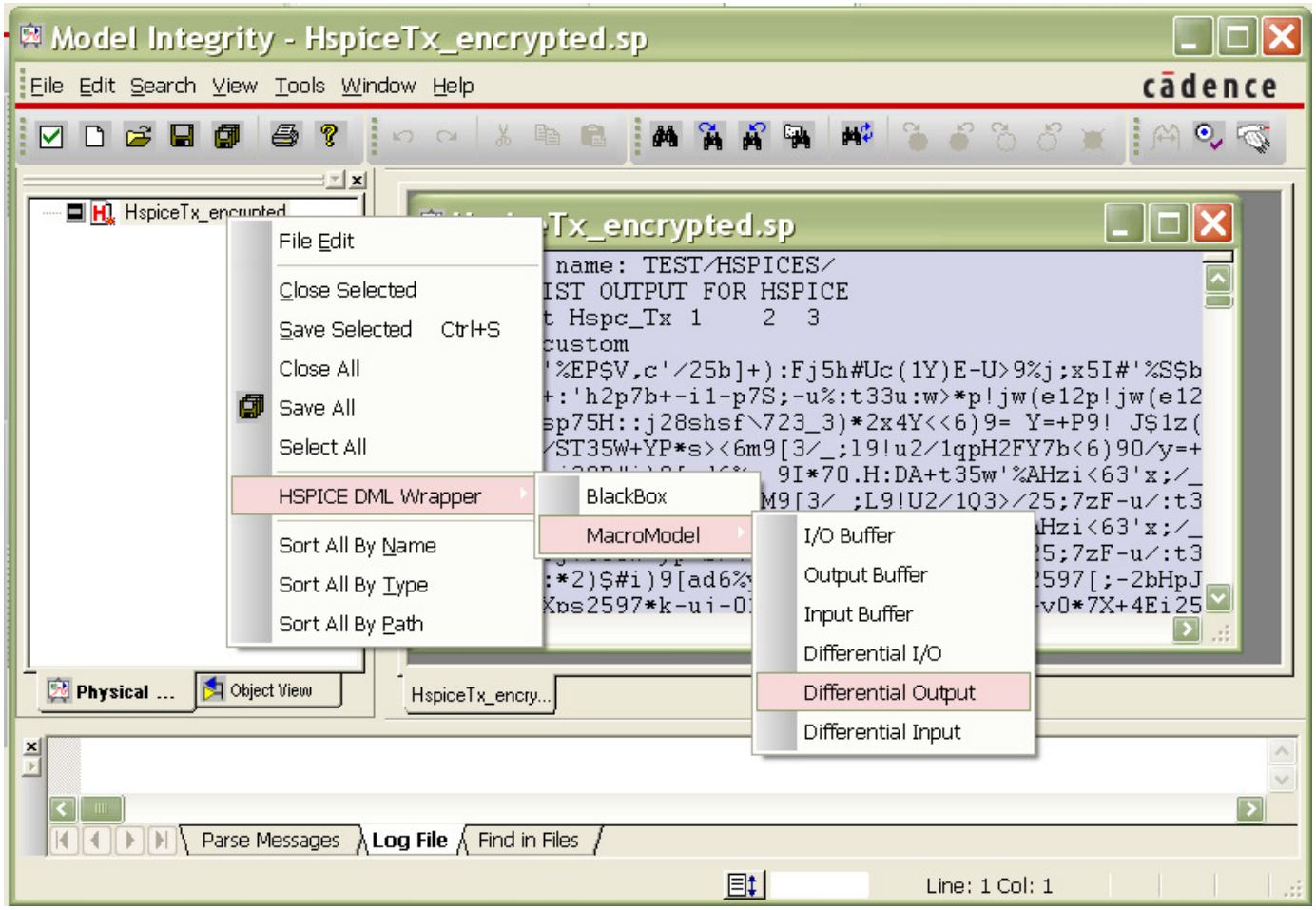
1. Get and AMI or DML model from IC vendor
2. Work with vendor's SPICE models
   a) Import (wrap) model in DML (new 16.3 feature)

      OR

   b) Import channel's characterization into CA
3. Use Cadence's generic AMI models



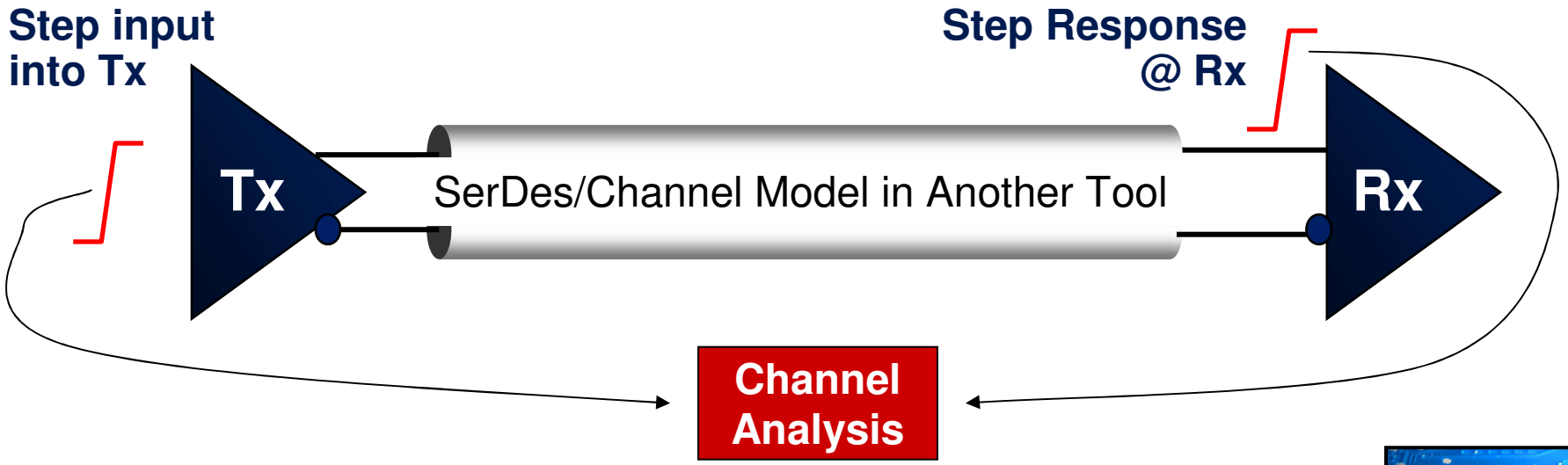
New Model Wrapping in 16.3



- Cadence's import (DML wrap) of transistor-level SPICE models
  - Spectre, Hspice, Generic-SPICE

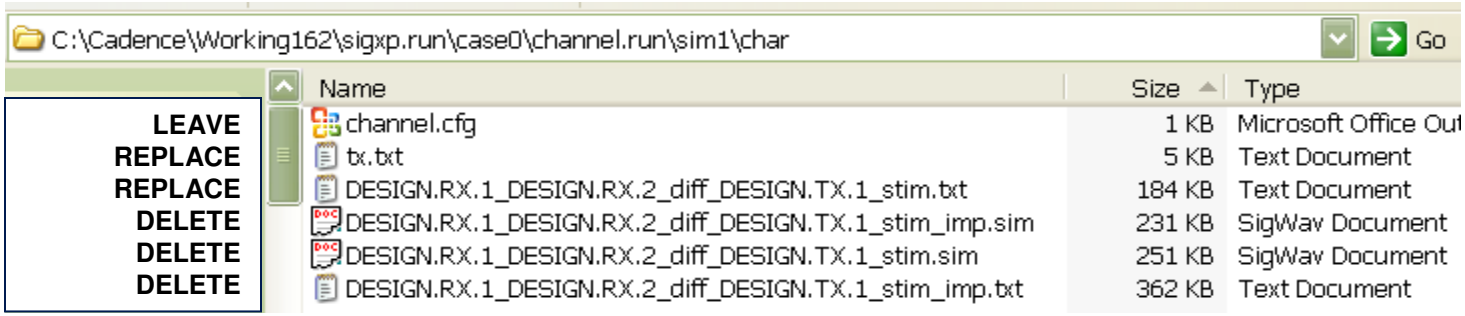
Import Characterization into CA

- Some vendors supply their SerDes models configured to run in an example channel in another simulator (eg, Hspice, Spectre)
- You can adapt that channel to match yours, simulate a step response, and import the Tx and Rx signals as a Characterization for CA
- CA runs as usual, **no model wrapping required**



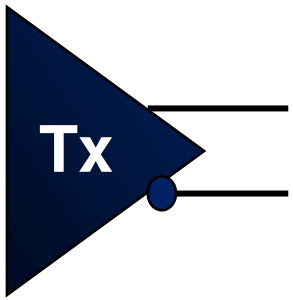
Characterization Import Procedure

1. Use SigXp to run a “dummy” CA
2. Browse to the \char directory
3. Replace tx.txt with step input into Tx
4. Replace xxx_stim.txt with Rx step response
   - Be sure formatting both txt files matches originals!
5. Delete other xxx.sim and xxx_stim_imp.sim
6. Run CA as usual on channel from other simulator



Using Cadence's Generic AMI

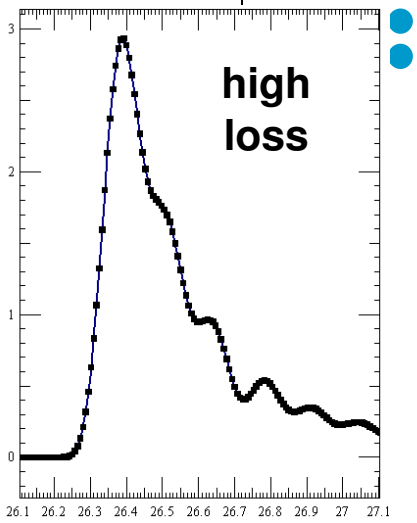
- Configurable FFE, DFE, CDR, etc Models
  - <install>\share\pcb\channelanalysis\ami\toolkit
  - Program Vswing and any number of pre/post taps
  - Adjust imp, edge, die_cap in macromodel portion
  - Mimic behavior of any spec-level Tx
  - Example: scale Vswing x1.2, 2 pre-, 3 post-cursors
    - Pre1=-2%, Pre2=-11%, Main=120%, P1=-50%, P2=-25%, P3=-10%

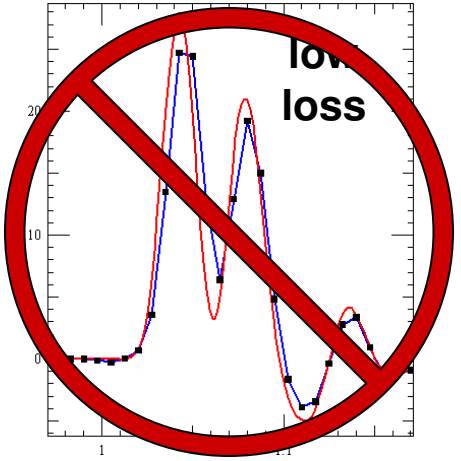



```
(ami_ffe <path to Cadence AMI ami_ffe.dll file>
    (fwd 6 ) (offset 2 )
    (fwdtaps "160e-12 3 -0.02 -0.11 1.2 -0.50 -0.25 -0.10" ) )
```

Time-Step Two-Step

- CA Characterization can be slow due to hard-coded 1.6 pS fixed time-step
  - Works well for *any* channel
- Many channels can be characterized with a larger time-step, especially those with high loss
- Can over-ride time-step with env variable “SetTlsimTimeStep” in pS
  - Makes characterization much faster
- Be careful!
  - Impulse response must be well-sampled

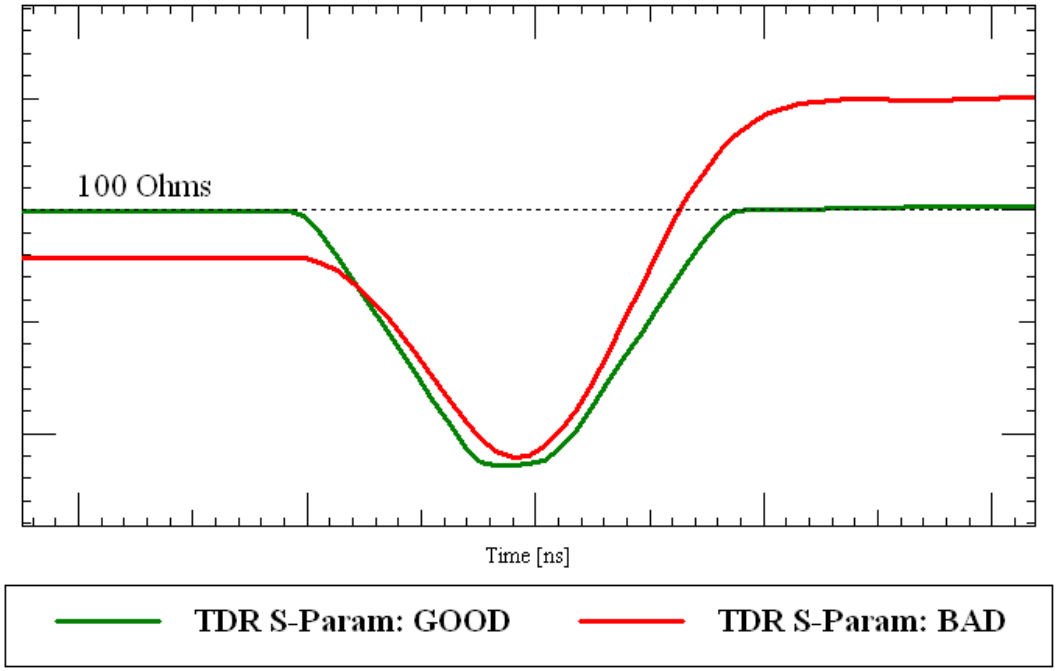




Agenda

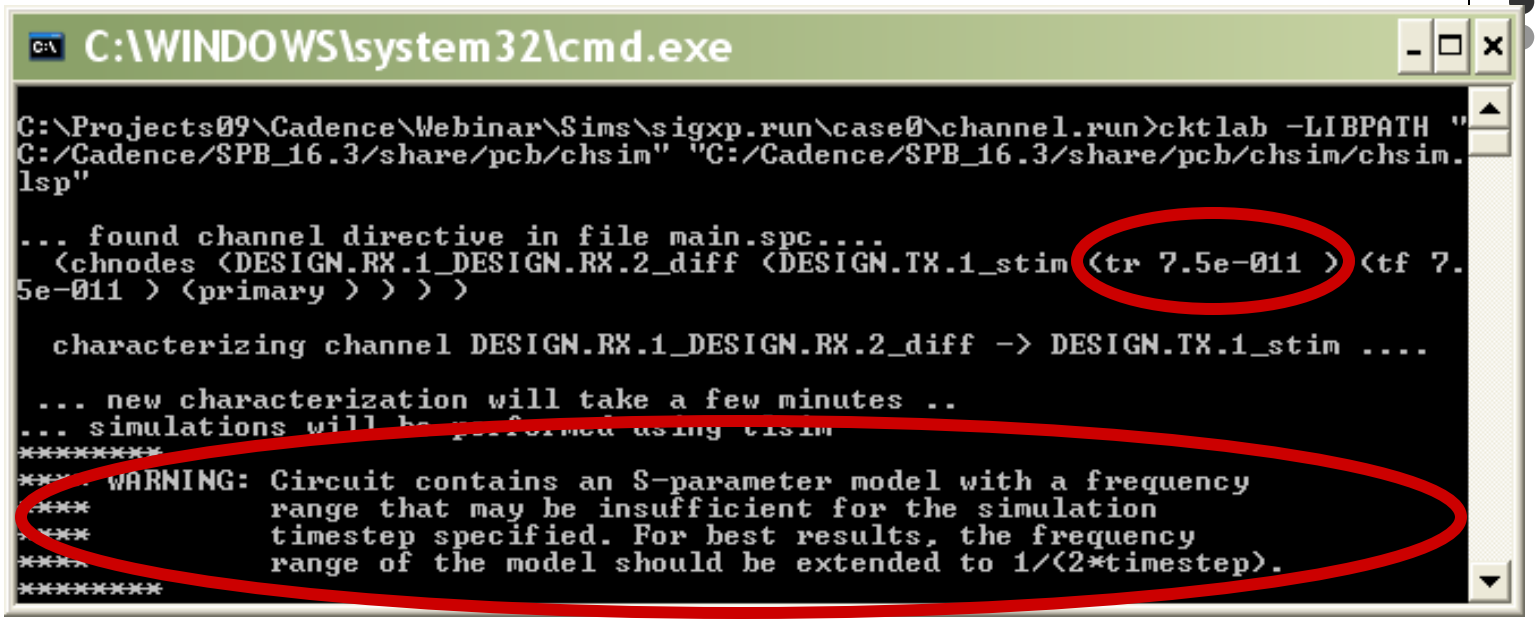
- Faster
- Better
  - S-Parameter Handling
  - Via Modeling
- Deeper

The Problem



- Simulated TDR of diff-pair trace solved into S-Params
  - S-parameters solved with different frequency ranges
  - note: you need simulated TDR capability
- Red = Incorrect impedances (DC levels)
- Green = Correct impedances (before/after discontinuity)
- Discontinuity looks (sort of) OK

The Reason



- Heed the WARNING
  - Especially if you have lots of cascaded S-params
- The Math:
  - Timestep = tr/10, therefore
  - Frequency_range must be >= 5/tr

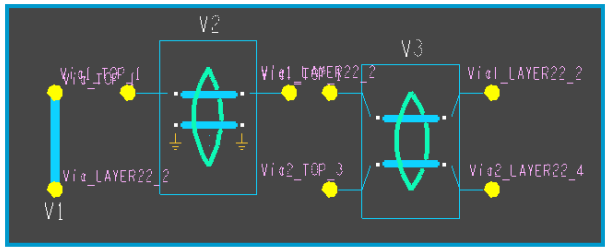
The Solution(s)

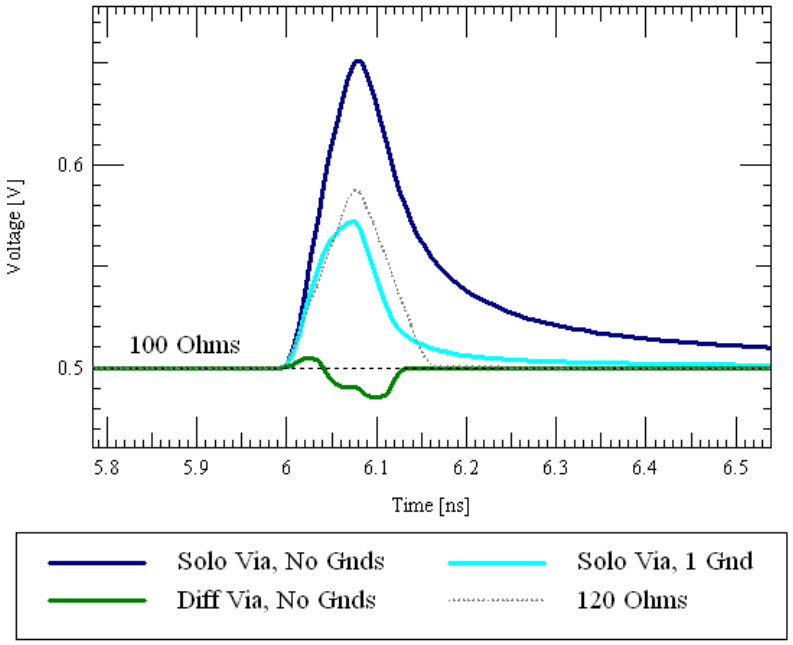
- Adapt S-params to edge rate
  - Becomes infeasible
- Adapt edge rate to S-params
  - Becomes inaccurate
- Force time-step using SetTlsimTimeStep
  - Becomes inaccurate
  - Characterizations with S-params likely need this
- Combination of the above
  - Particularly at higher Gbps

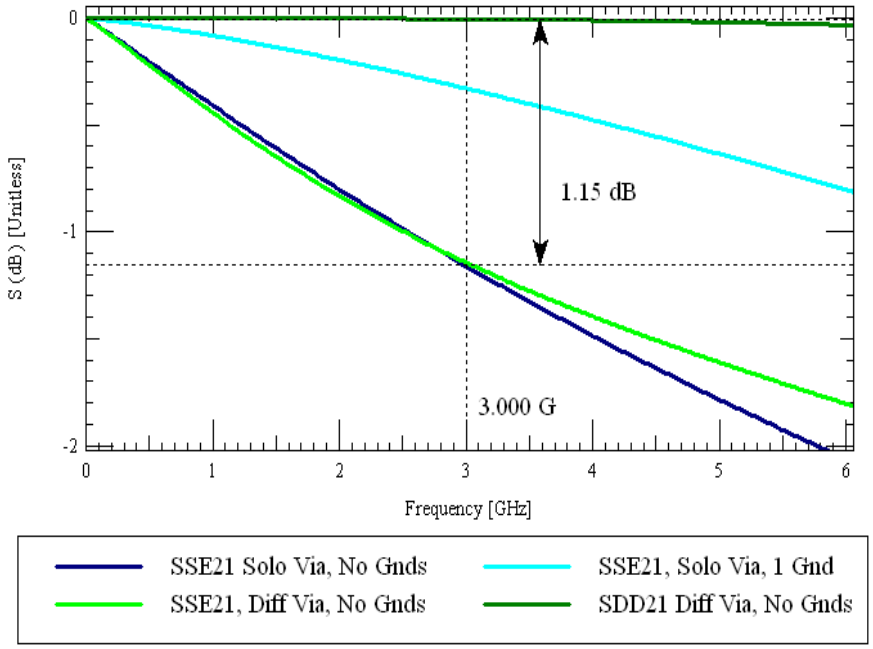
Trise-fall	FreqRange
200 pS	25 GHz
100 pS	50 GHz
50 pS	100 GHz

Time-Step	FreqRange
20 pS	25 GHz
10 pS	50 GHz
5 pS	100 GHz
1.6 pS	313 GHz

Use the Right Via Model







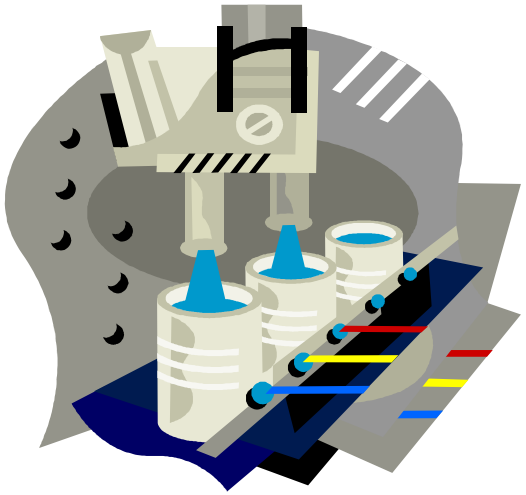
- Differential impedance off by 40%
- Differential loss off by 1+ dB

Agenda

- Faster
- Better
- Deeper
  - Scripting
  - Batching
  - Graphing

Scripting

- Scripts can be recorded in SigXp
  - File -> Script -> Record
  - Saves script.scr file
- Record scripts to
  - Generate topology permutations
  - Change sim corners/preferences
  - Change CA config and settings
  - Run CA char and results



Batching

- With scripts in place, execute batch runs
- sigxp –nograph –s scriptname.scr file.top
  - -nograph = no graphics (ie, do not open GUI)
  - -s = run script scriptname.scr
- Coordinate with Perl, DOS, Unix, etc. commands
- In this way, thousands of CA runs can be generated, configured, and simulated

Graphing

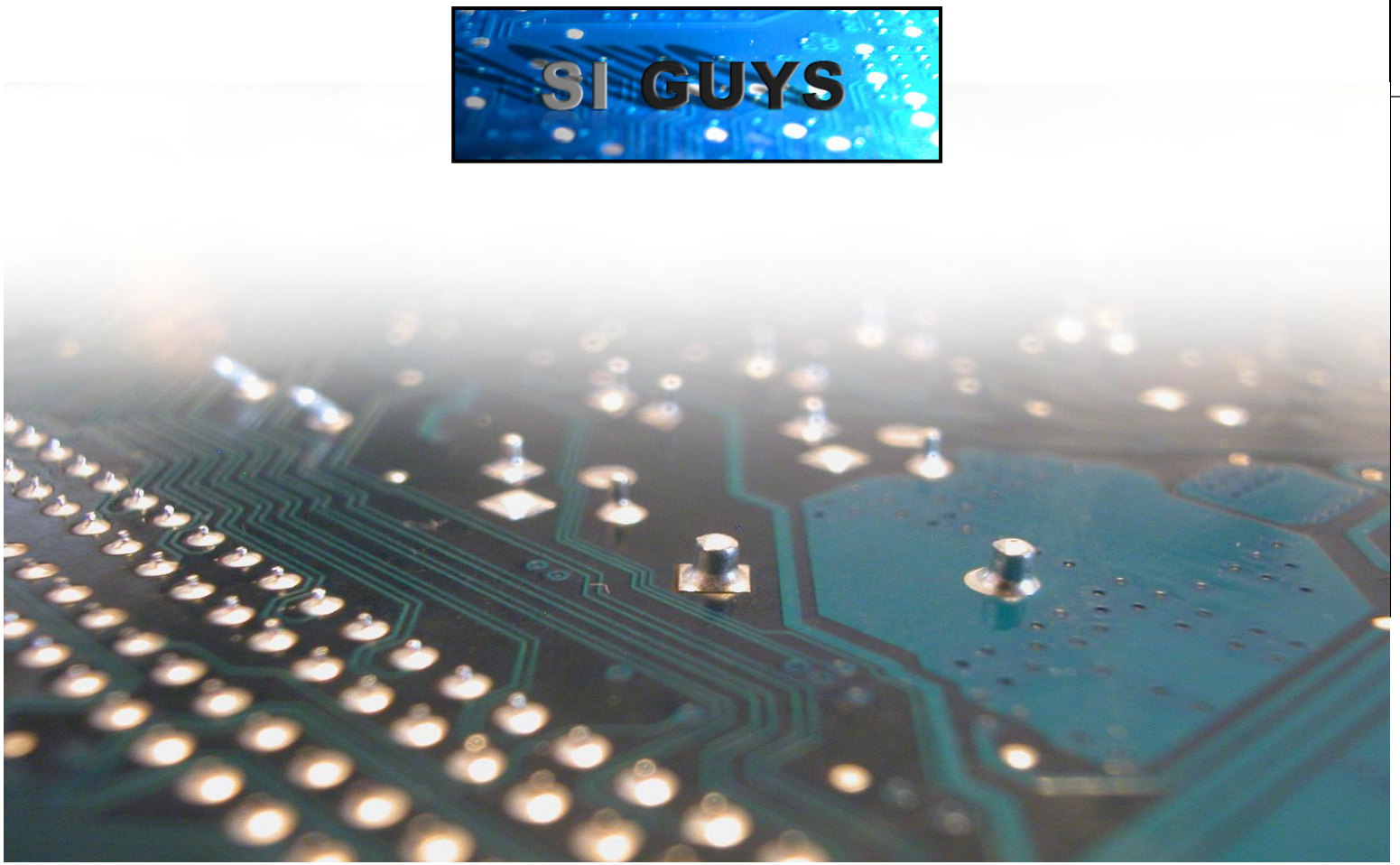
- Each CA run creates chsim.rpt in \results dir
- Automate extraction of key eye parameters
  - Height and width, at any number of bits
- Build table of values, graph in Excel
- Sort by different variables
- Identify trends, sensitivities, dependencies

```
Eye height                    = 826 mV
    UI at max height          = 0.54 UI
Eye jitter                    = 0.06 UI

Report:

   logBER      UI
  -9        0.82
  -10       0.81
  -11       0.8
  -12       0.8
  -13       0.79
  -14       0.78
  -15       0.78
```

In Summary

- CA provides high-capacity simulation
  - For a variety of multi-gigabit data rates
  - For a variety of channels and standards
- We have presented advanced techniques to help your use of CA become faster, better, deeper
- For more info, visit the virtual booth or contact me at telian@siguys.com

THANK YOU



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