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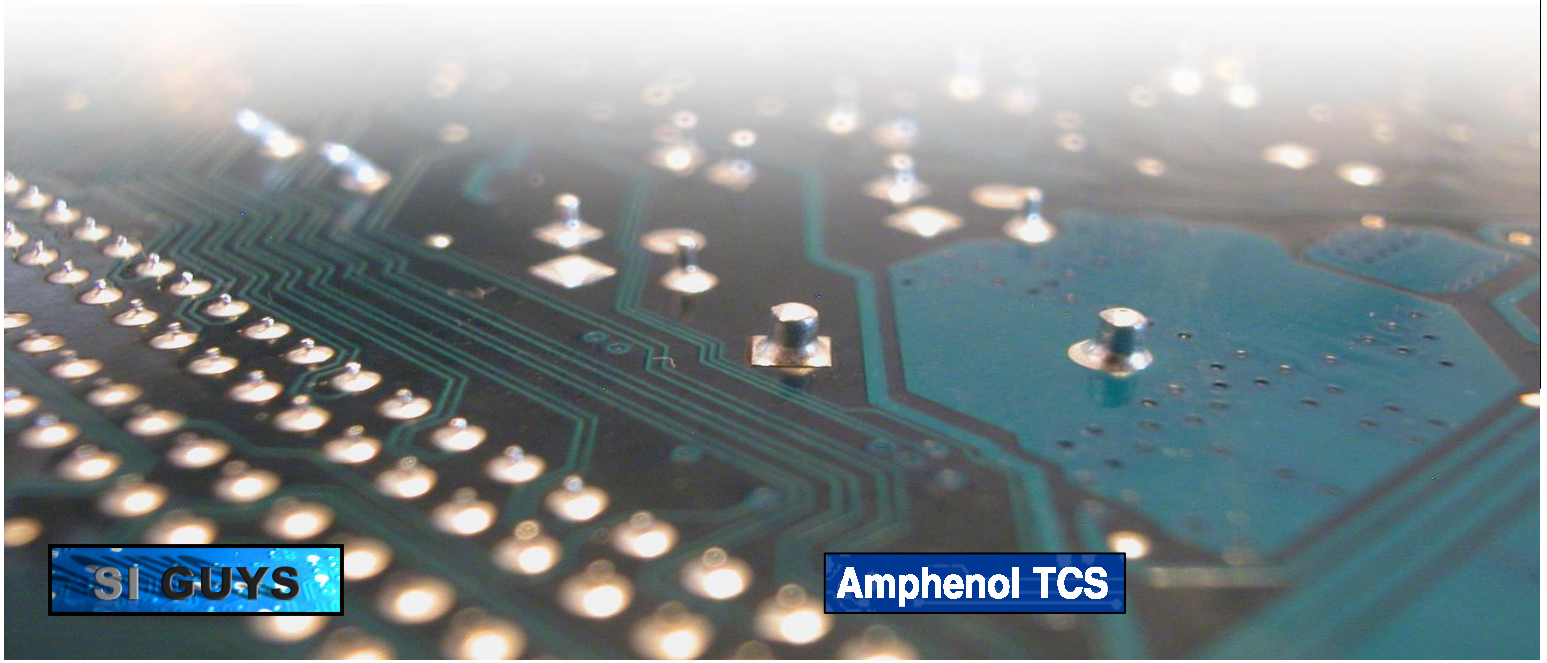
Simulation Techniques for 6+ Gbps Serial Links

Donald Telian – SI Consultant, Siguys
Sergio Camerlo – Sr. Director, Ericsson
Brian Kirk – SI Engineer, Amphenol TCS

Session 7-TA4



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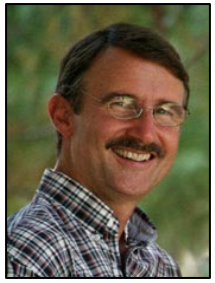
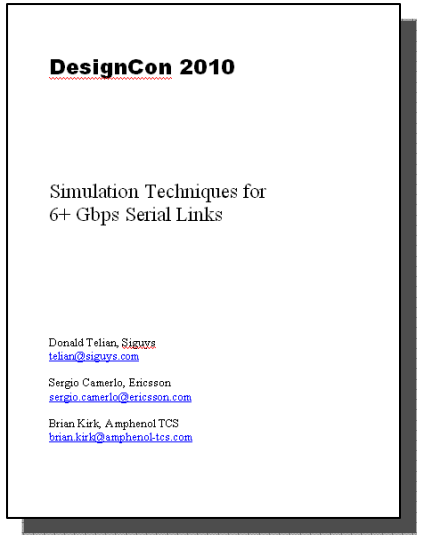
About the Authors



Donald Telian is an independent Signal Integrity Consultant. Building on over 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-Gigabit serial links. His numerous published works on this and other topics are available at his website siguys.com. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling, and has taught SI techniques to thousands of engineers in more than 15 countries.



Sergio Camerlo is a Sr. Director, HW Engineering with Ericsson Silicon Valley, which he joined through the Redback Networks acquisition. His responsibilities include the New Platforms Channel Design and Backplane Technology, including Signal and Power Integrity. He has also served on the company Patent Committee. In his previous assignment, Sergio was VP, Systems Engineering at MetaRAM, a local startup, where he dealt with 3D integration and modularization of memory structures. Before, Sergio spent close to a decade at Cisco Systems, where he served in different management capacities and as Engineering Director. Sergio holds 13 US Patents on signal and power distribution, interconnects and packaging.

Brian Kirk is a signal integrity engineer at Amphenol TCS. He has previously worked for Digital Equipment Corporation, Compaq, Hewlett Packard and Teradyne. His previous experiences include a variety of signal integrity tasks, module designs and FPGA designs for servers and routers. He is currently involved in connector development, simulation and correlation for high-speed interconnects. He received his PhD in Electrical Engineering from the University of New Hampshire.

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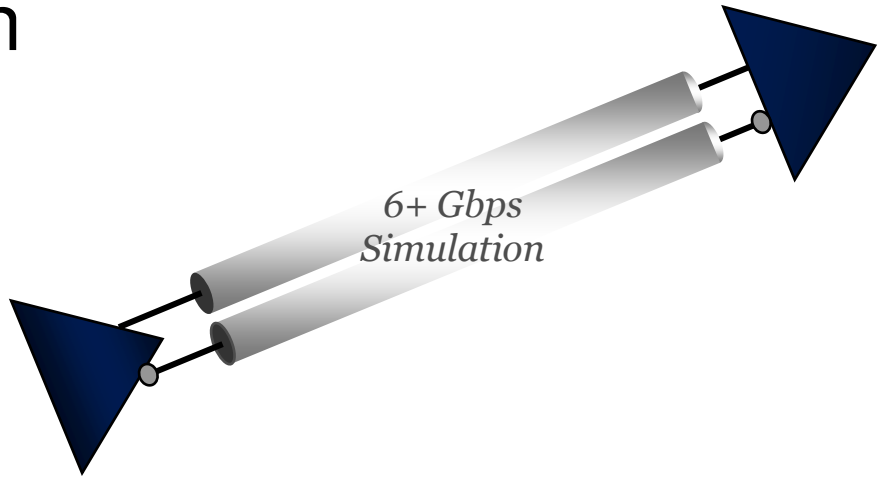
Agenda

- 6+ Gbps Simulation Process
- Modeling Techniques
- Link Simulation
- Summary



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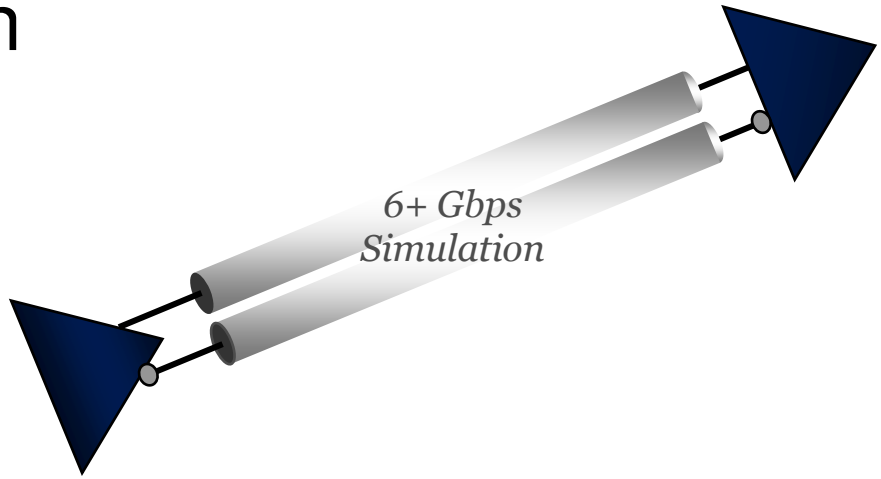
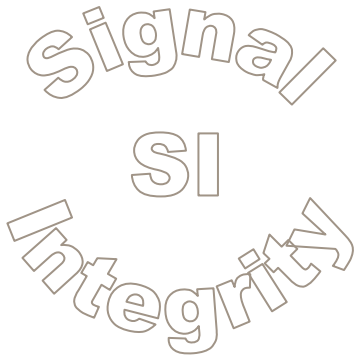
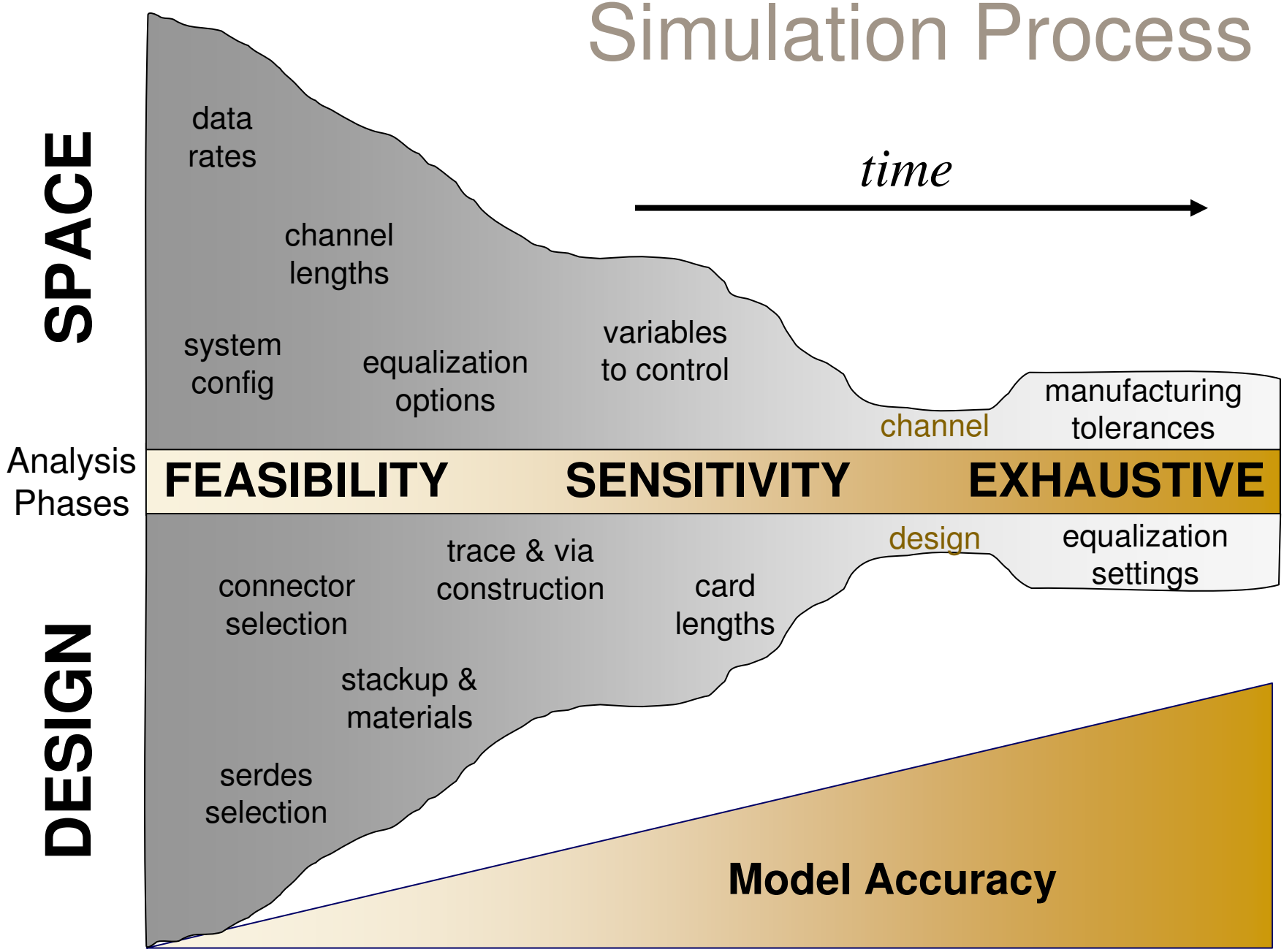


6+ Gbps Channel Simulation

- Channel simulators on open market for 5+ years
  - Frequencies and #bits simulated x1,000
  - Enabled new standards, new design processes
- Familiar SI techniques now feasible (…and practical!)
  - Exploration, what-if's, trade-offs
  - Variations
- Thousands of equalization options and settings
- Accurate models are key
- PoP: **P**ower **o**f **P**artnership



Simulation Process



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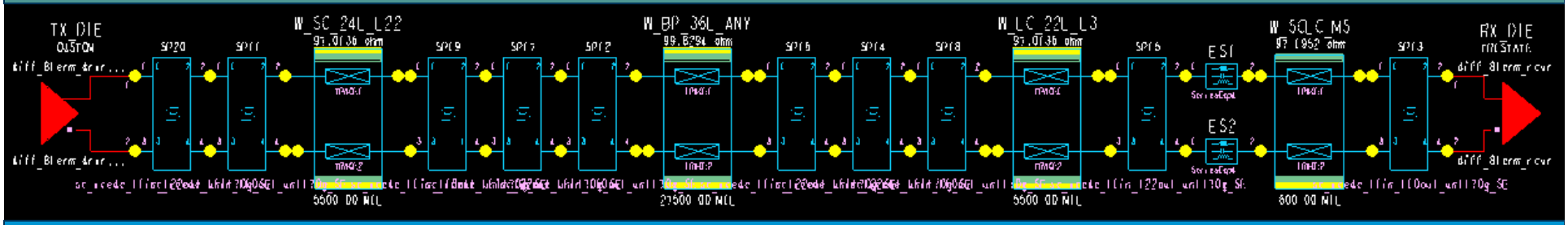
Typical Serial Link Channel Topology

Tx Pkg		**Backplane Connector**	**Backplane Connector**	Vendor Supplied S-Params	**Rx Pkg**
Transmission Line Models	**Tx Stripline Route**		**Bp Stripline Route**	**Rx Stripline Route**	**Rx Microstrip Route**



	Tx Pkg Via	**Tx Conn Via**	**Bp Conn Via**	**Bp Conn Via**	**Rx Conn Via**	**Rx Cap Via**	Field-solved S-Parameters
Tx Model		SPICE / AMI / Experience -based Models				**Cap Model**	**Rx Model**

- 17 cascaded elements allow exploration and tuning of channel across 3 PCBs
- Valuable work can be done with generic/approximate SerDes models
- Library of via/trace models comprehend various routing layers

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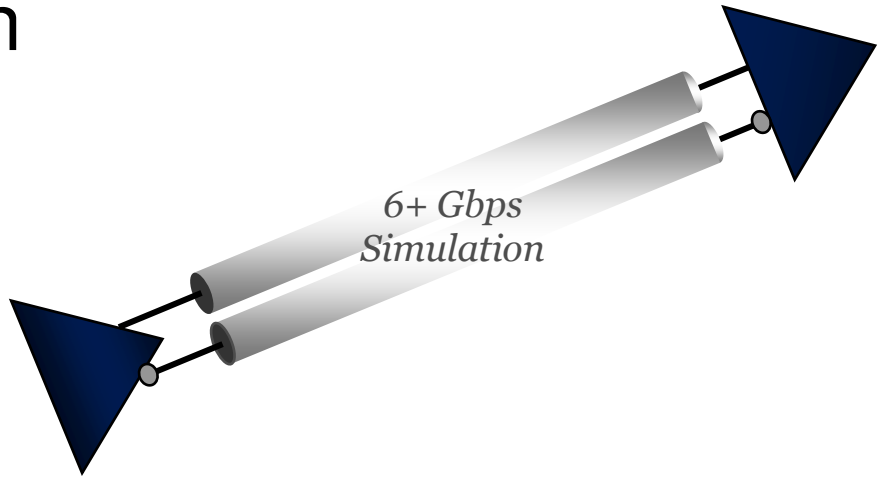
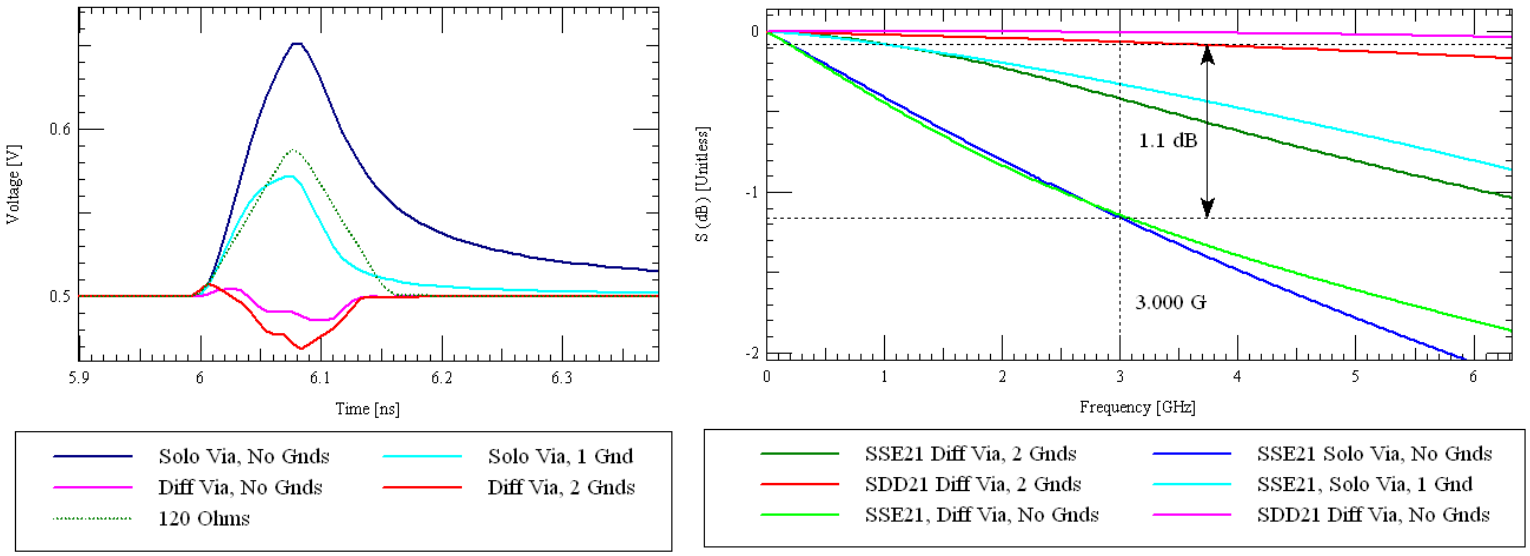
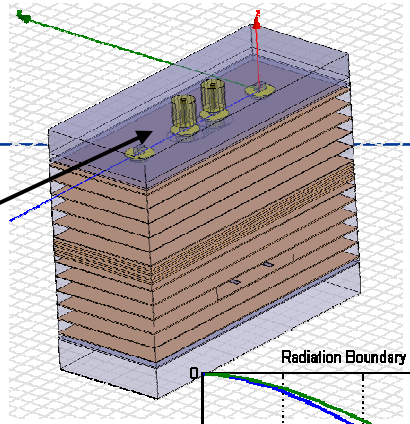


Via Models – Why do we care?

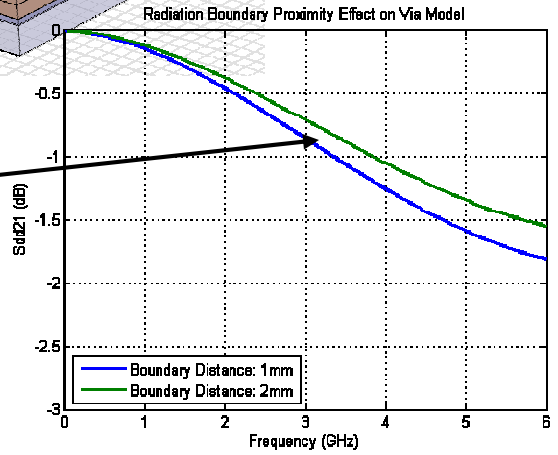
- Vias (& connectors) are the primary discontinuities
- Big mistakes can cause 90% of signal to disappear
- Subtle changes yield 50-100% improvement
  - Not-so-subtle changes yield 700% improvement
- Incorrect via models cause 50% error in channel loss

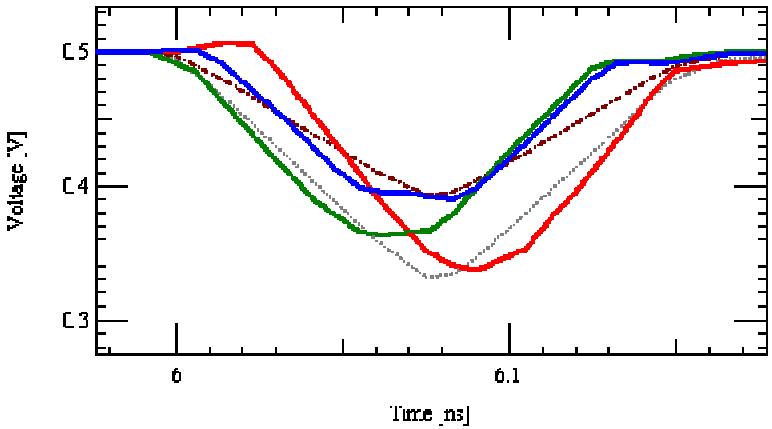


Correct Via Modeling

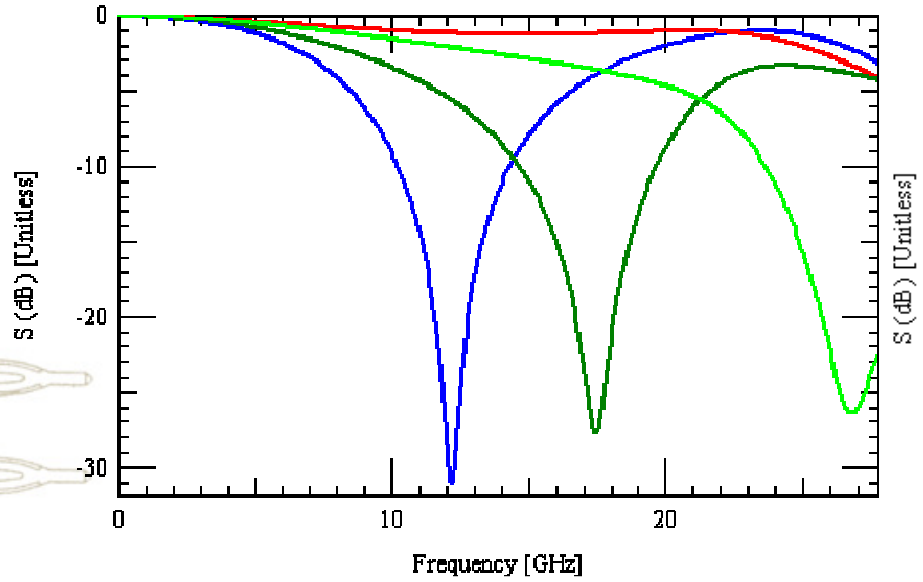


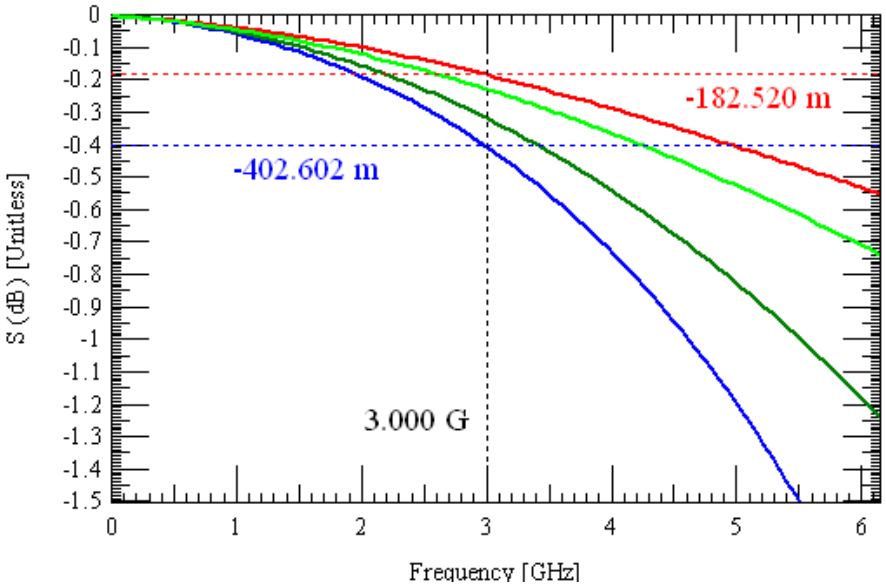
- Pay attention to:
  - Excitation ports
  - Boundary conditions
    - 20% error
- Guide design choices
  - Decent 2s/2g model (red)
  - Remove metal (green)
  - Refine model (blue)
  - 10 Ohm improvement





Longer Vias Often Have Less Loss

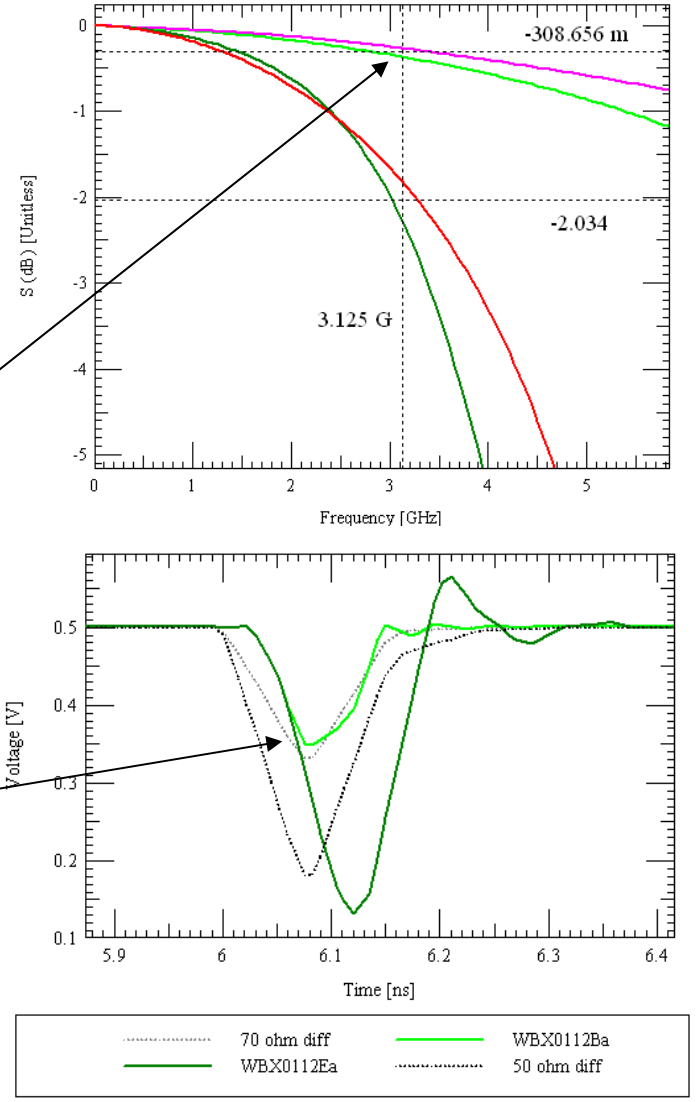




- 120 mil PCB, blue=short_via, red=long_via
- Short vias typically have long stubs
- freq_dip ~= 1.5/stub (stub in inches, freq in GHz)
- short_via loss 2x greater than long_via (at 3 GHz)

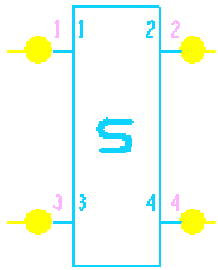
Back-drilling to Remove Stubs

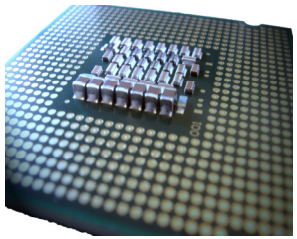
- ¼” backplane vias
  - lighter shades are back-drilled
- Insertion loss
  - improved 7x 2.1 to 0.3 dB
- Impedance
  - 60% better 45 to 73 Ohms



Other Passive Interconnect

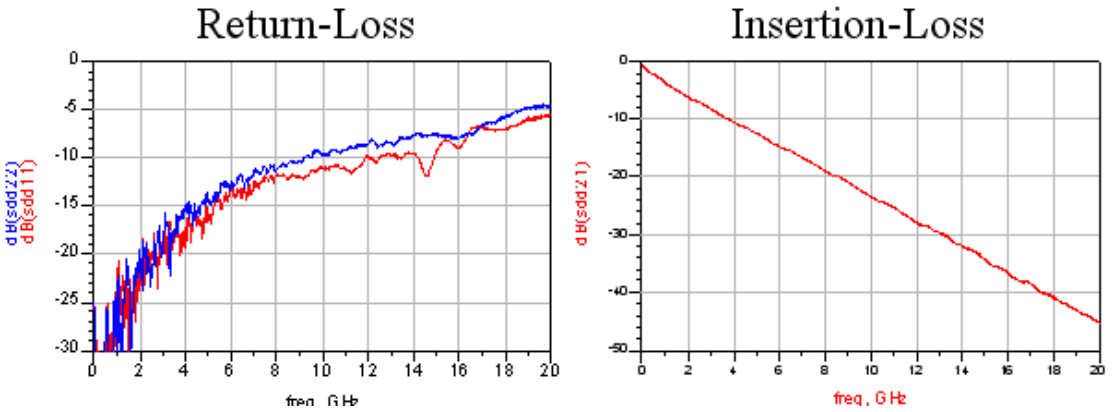
- Trace construction impacts system performance
  - dimensions, materials, cost/performance trade-offs
  - accurate modeling of trace loss imperative
- Carefully select, model, and design:
  - AC capacitor's placement, vias, mounting
  - Connector, vias, and mounting
- SerDes package parasitics
  - Accurate model is essential



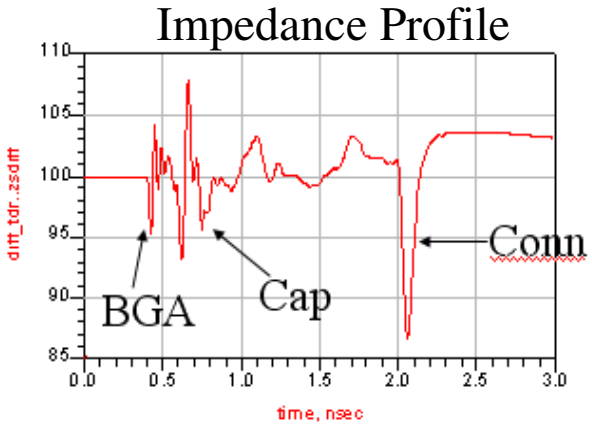


Learning from Measurements

- Many model and system insights from measured loss/impedance (VNA/TDR) of passives

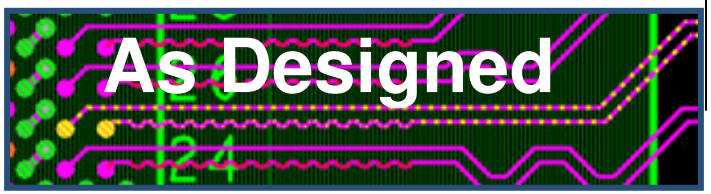


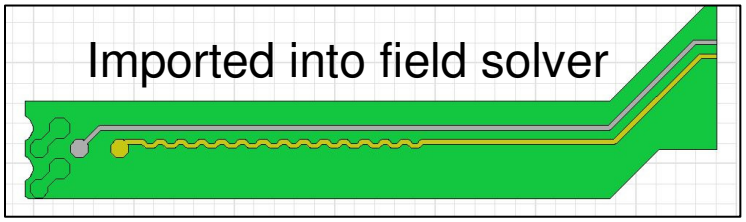
- 3D structures more difficult
  - 2D trace impedance/loss ~good
  - Mounted AC cap model a challenge
  - Via measurements typically a few ohms better than model

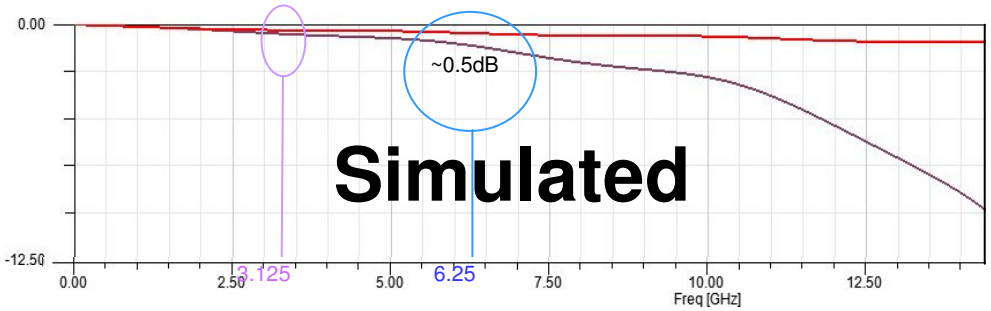


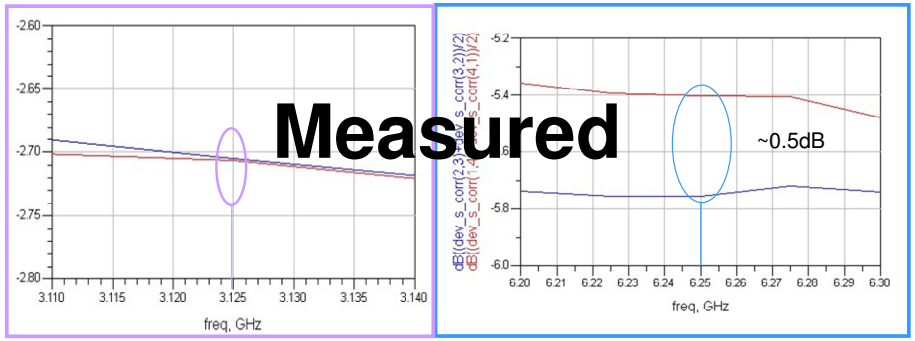
Correlating Assumptions vs Frequency

- Assumptions from lower frequencies might not be true at higher frequencies
- Utilize tools, test vehicles, and measurements to find answers early in design cycle
- Example: p/n length matching
  - 3 GHz: p/n, similar loss
  - 5+ GHz: loss unbalance → skew → eye closure

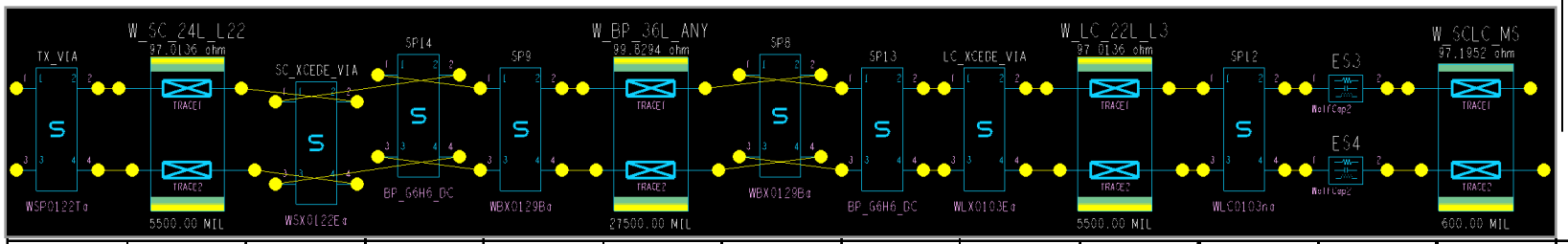






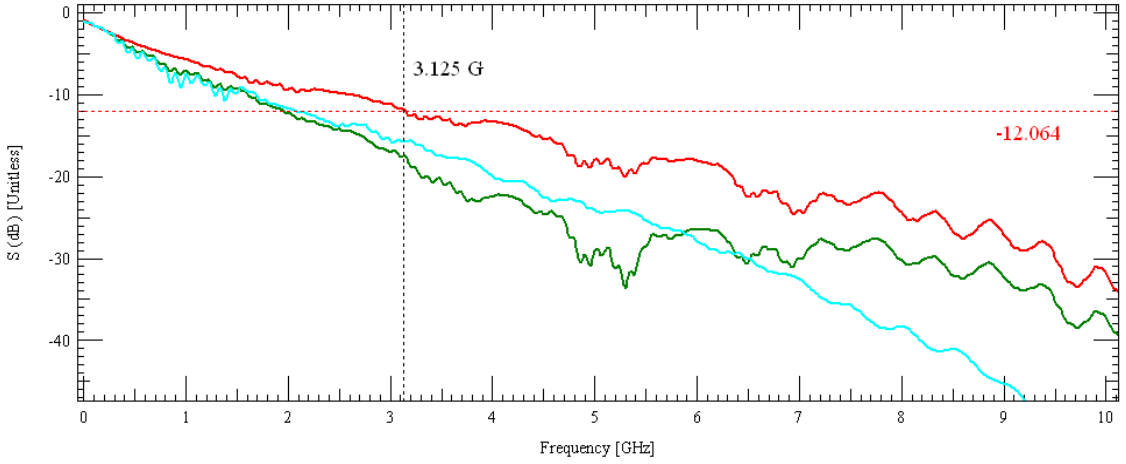


Passive Channel Loss Analysis

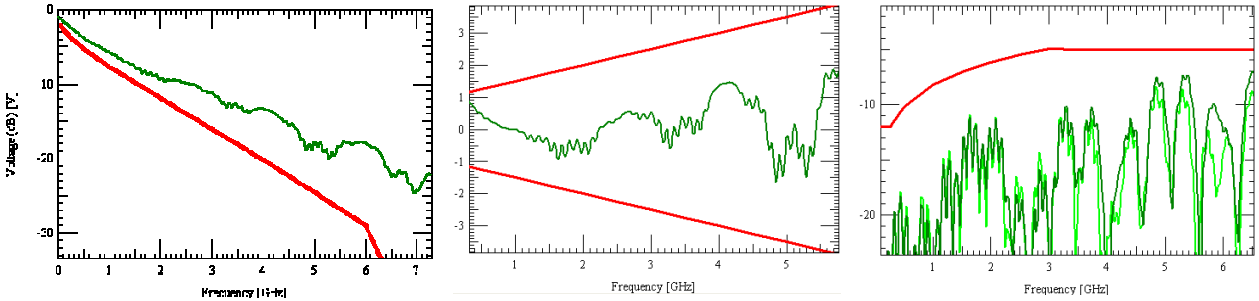


Tx Via	TxCd Tr	TxCn Via	Conn	Bp Via	Bp Tr	Bp Via	Conn	RxCn Via	RxCd Tr	RxCd Via	AC Cap	Rx us Tr	Total dB
0.12	1.97	0.21	0.51	0.40	5.38	0.40	0.51	0.31	1.97	0.12	0.01	0.20	12.11

- Good models =
- Correct loss =
- Right Amplitude =
- Correct Eye



- SSE21 ≠ SDD21



- Industry Masks

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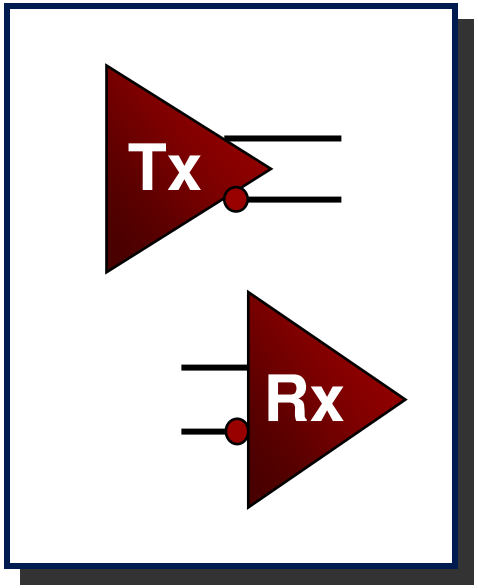
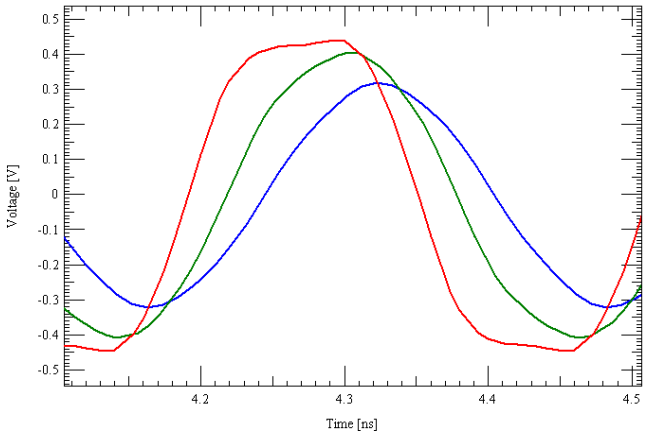
SerDes Modeling

- Rapid simulation assumed
- Model has two portions for two tasks
  - “analog” for “channel characterization”
  - “equalization” for “channel simulation”
- Analog portion captures datasheet parameters
  - Impedance, return loss, amplitude, edge rate, etc.
- Equalization typically in AMI
  - Tx FFE, Rx DFE





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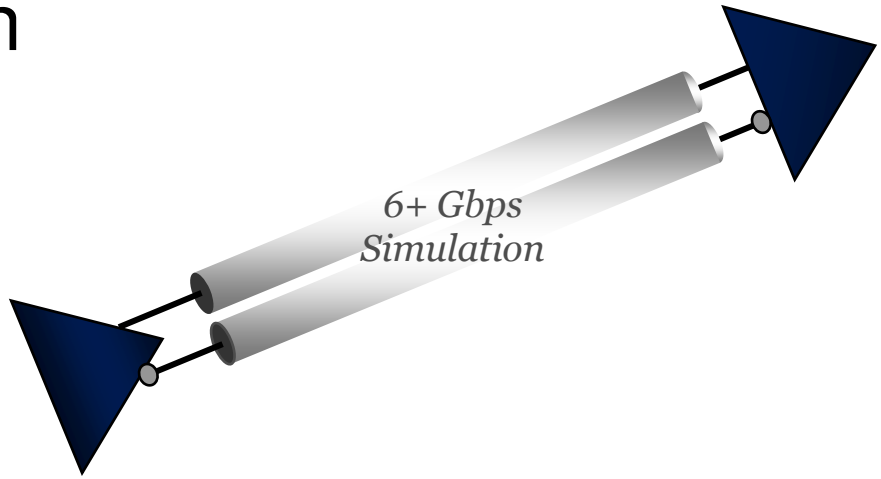
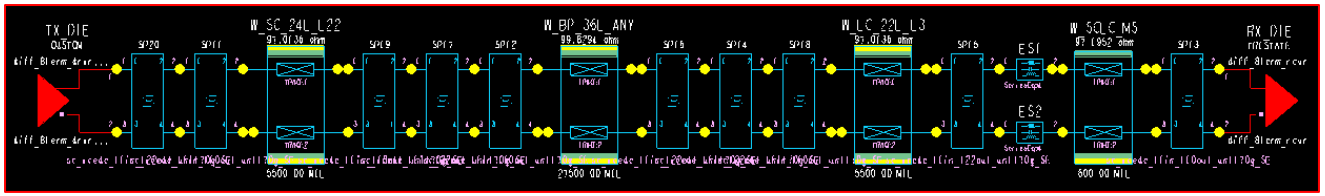
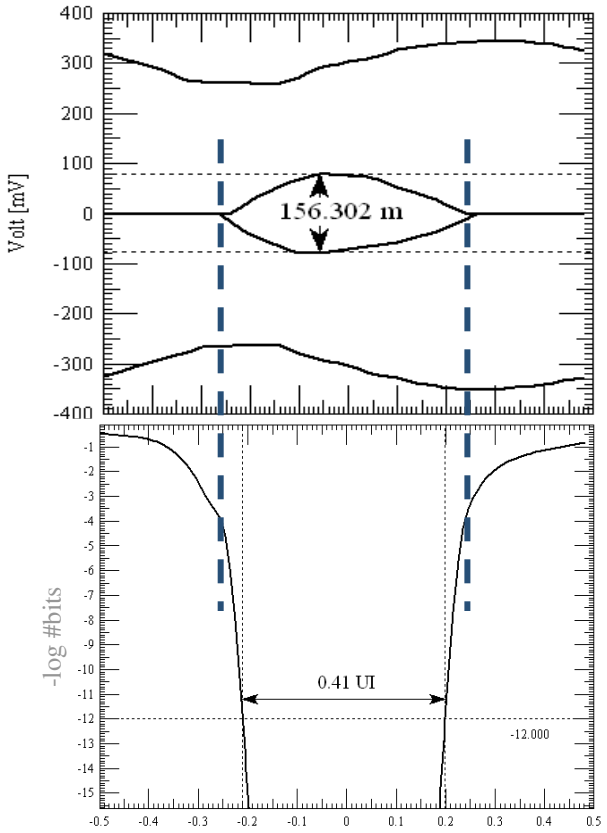


Channel Simulation Metrics

- Simulate Channel

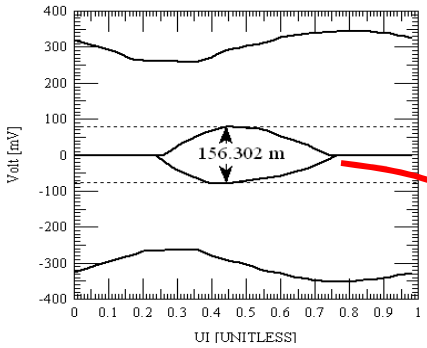


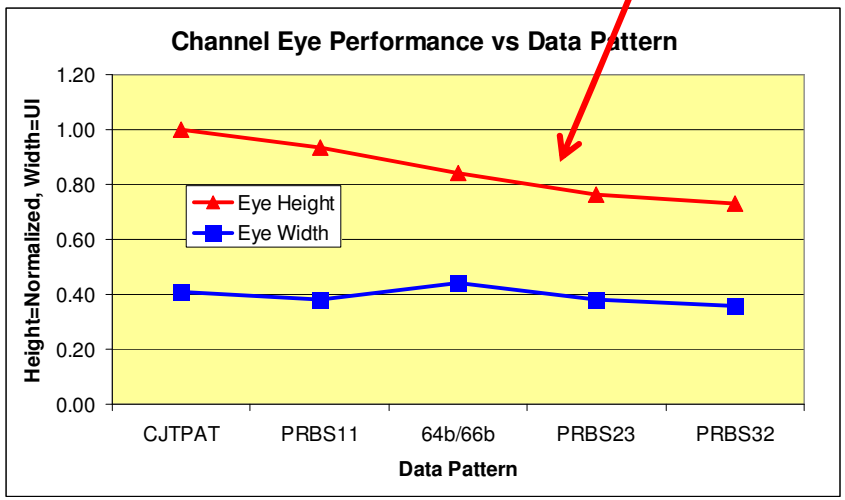
- Standard Metrics
  - Rx Eye Height (mV)
  - Rx Eye Width (UI)
- Simulate ~million bits
  - Various data patterns
  - Get beyond knee
- Statistical jitter sources
  - Width at 1e12 bits
- Baseline metric
  - Ht/Wd, mV/UI, 156/0.41



Eye Charts

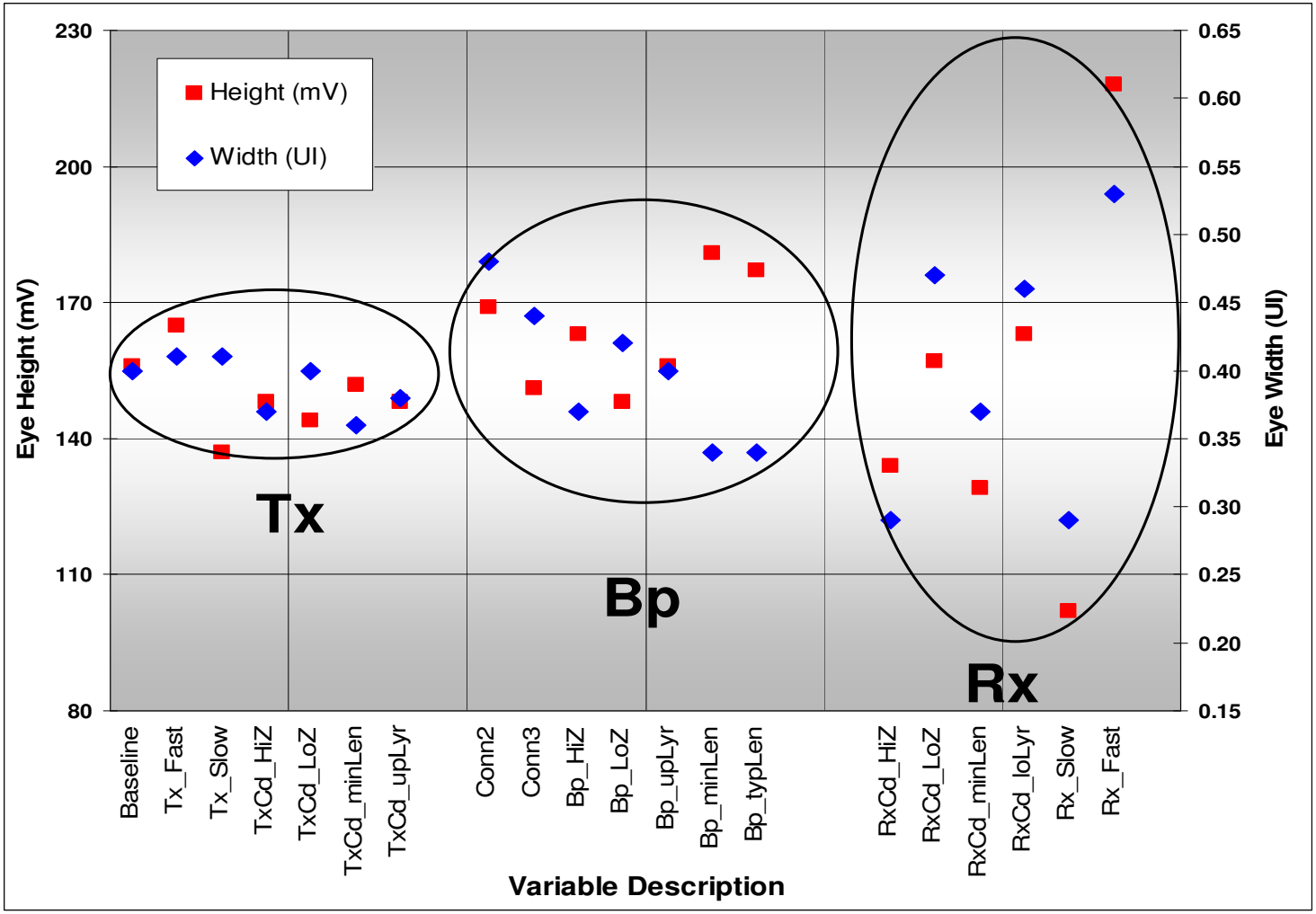
- Abstract eye metrics into charts
  1. Achieve reasonable eye
     - see process in 2009 paper
  2. Gain confidence in eye at “corners”
  3. Extract eye height/width, plot in charts
- We did this with many other SI metrics
  - e.g., Switch/Settle times
- No more eyes shown
- Example:
  Ht/Wd vs Data_Pattern
- Simulation techniques shown by example





Sensitivity Analysis

	Tx Card				Backplane					Rx Card			
Baseline →	Tx	Card	Length	Layer	TxConn	Bp	Layer	Length	RxConn	Card	Length	Layer	Rx
	Typ	NomZ	Max	Lower	Conn1	NomZ	Lower	Max	Conn1	NomZ	Max	Upper	Typ
	Fast	HighZ	Min	Upper	Conn2	HighZ	Upper	Min	Conn2	HighZ	Min	Lower	Fast
	Slow	LowZ			Cpnn3	LowZ		Typ	Conn3	LowZ			Slow



Manage:

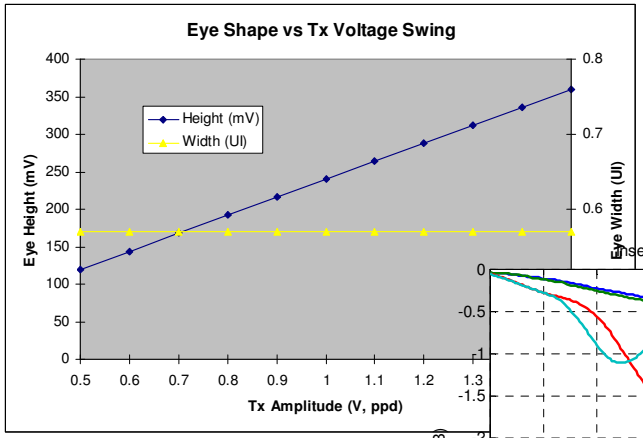
Tx

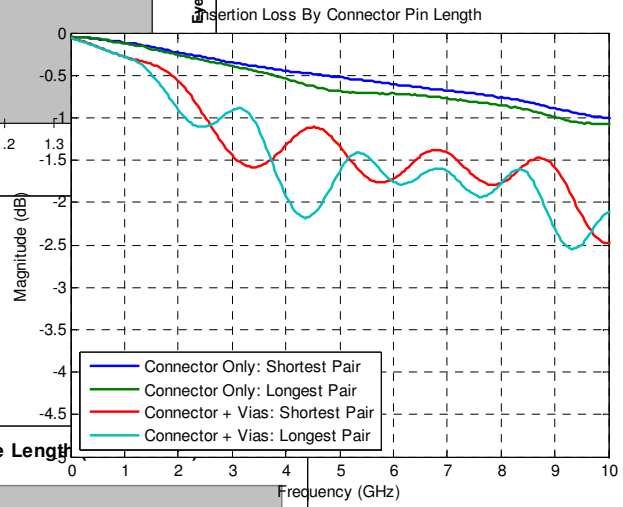
Bp

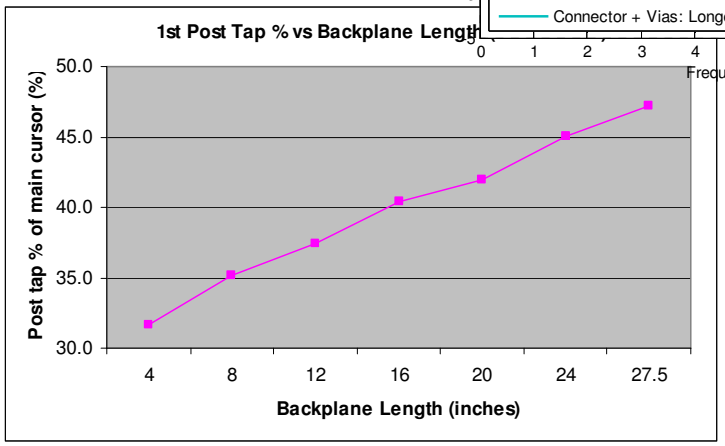
Rx!

Sensitivity Analysis Observations

- Tx Amplitude
  - Rx height scales linearly w/ Tx
  - Width stable
- Connector
  - Conn / Via combo causes variation
- BP Length
  - Ideal EQ ~linear with bp length
  - Use “net bundles” with different EQ

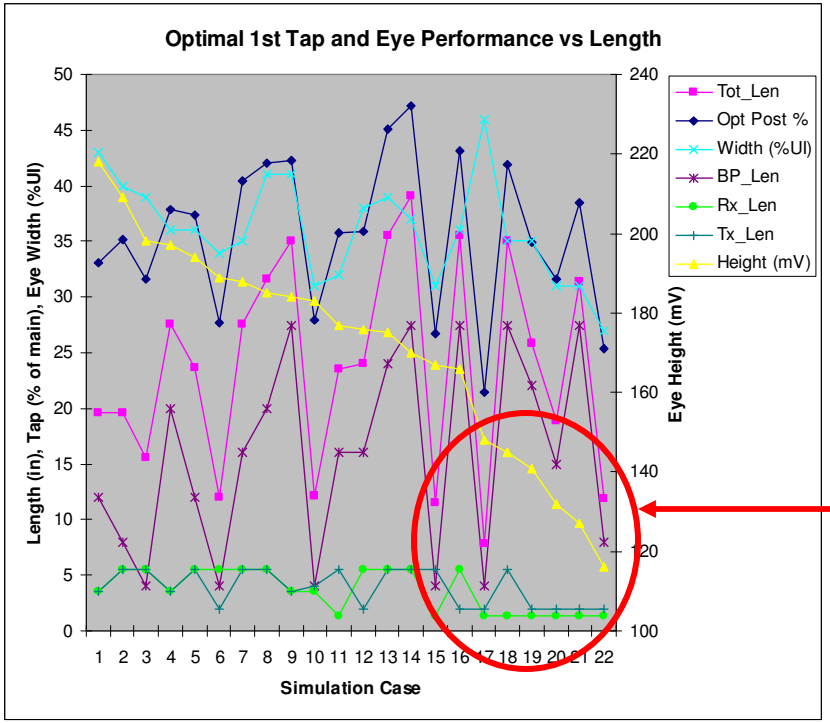


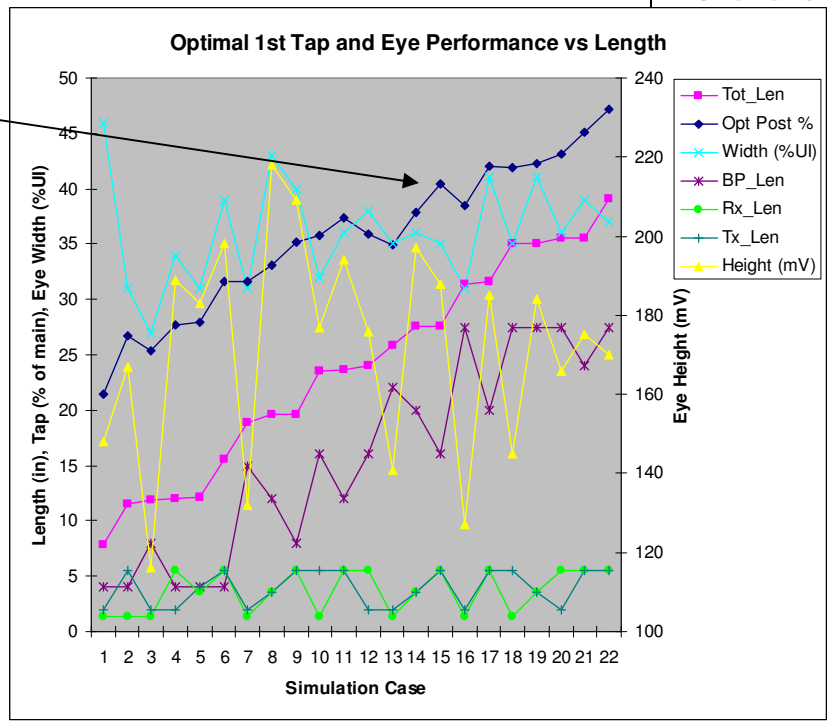




Exploring Range of Channels/EQ

- Most tools will calculate & simulate optimal Tx EQ values for a given channel
- Eye height (yellow) doesn't track with length (pink) or EQ setting (dark blue)





- Sort by eye performance metric instead of length
- Min lengths on cards show worst performance – even with ideal EQ
- Fix by constraints, not EQ

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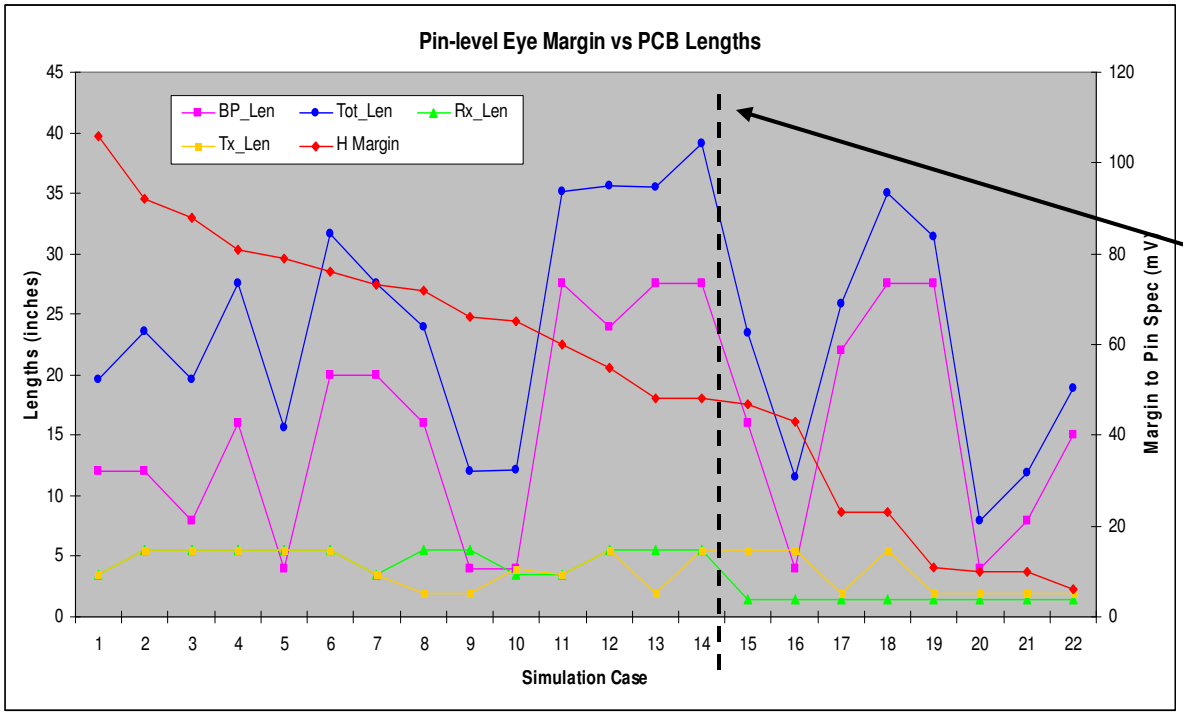
Net/EQ Bundle Derivation

A unique EQ for each channel is undesirable, so:

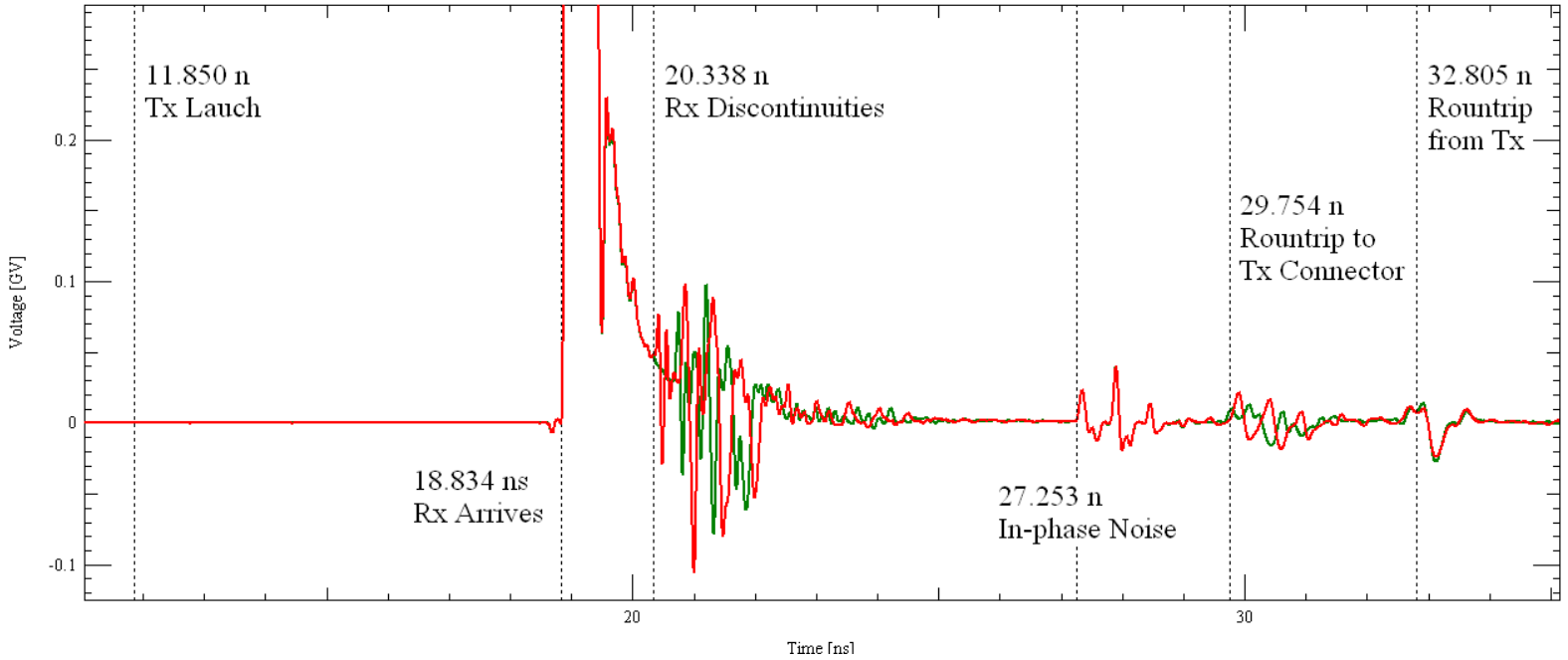
1. Divide optimal EQ range into “bundles”
2. Associate bundles with net lengths on largest PCB
3. Simulate to verify performance at discrete EQ values
4. Loop back to step 1, if necessary



- Margin (red) found in all bundles
- Constrain min Rx length removes low margins
- Worst margins now longest nets
  - desirable, fix with new bundle as required

Manage Rx Discontinuities

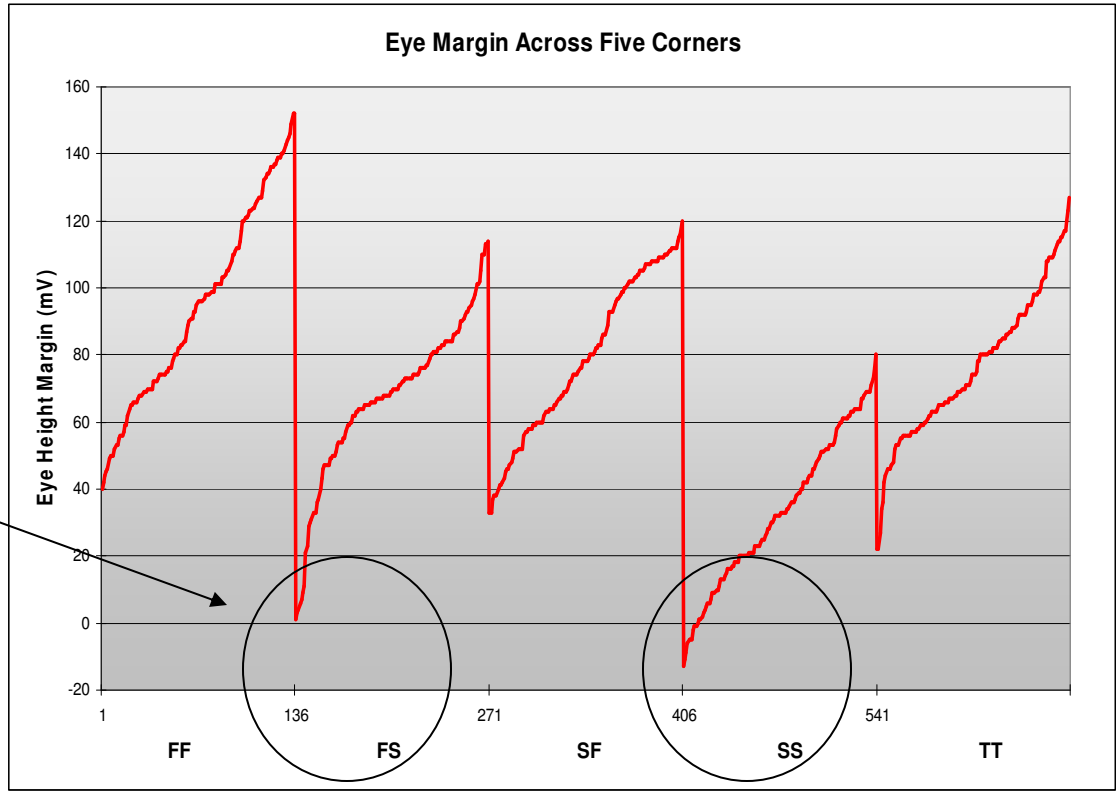
- Impulse response of two same-length channels
- Red (short Rx len) eye 20% worse than green (long Rx len)



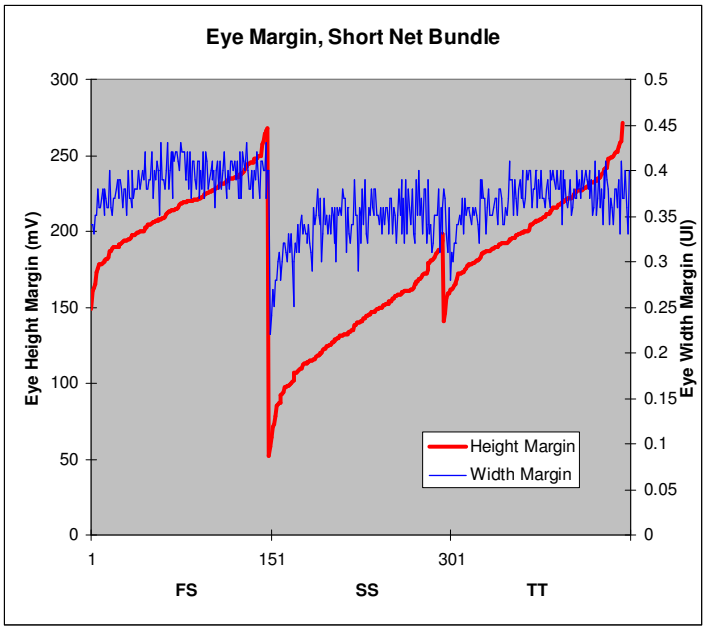
- Minimize via stubs, design AC cap structure
- Enforce minimum length: 40% more margin!

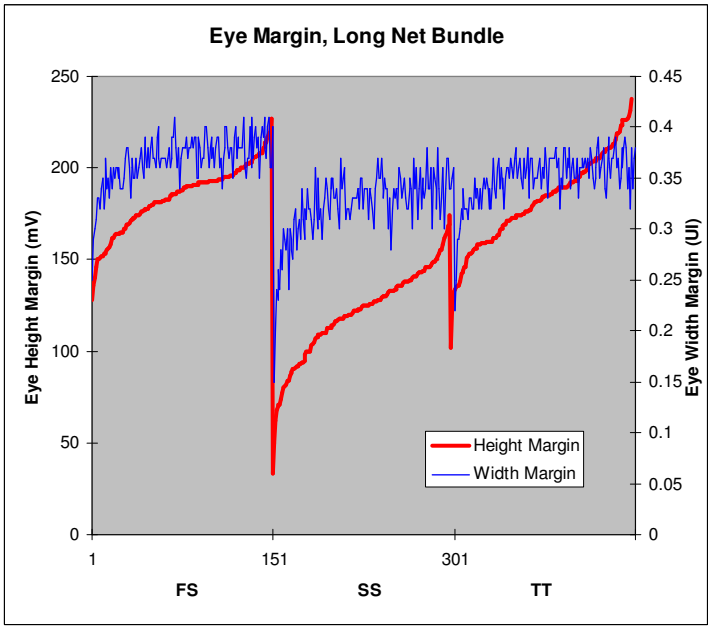
Exhaustive Analysis

- Exhaustively test margins against tolerances
- Channel analysis time ~ 2 mins for 100k bits
  - Characterization and simulation
  - Use automation
- 5 TxRx corners
  - FF FS SF SS TT
- Lowest margins at FS and SS
- Improve by:
  - Tx swing scaling
  - Increment EQ



Revised Config, ~2k Datapoints

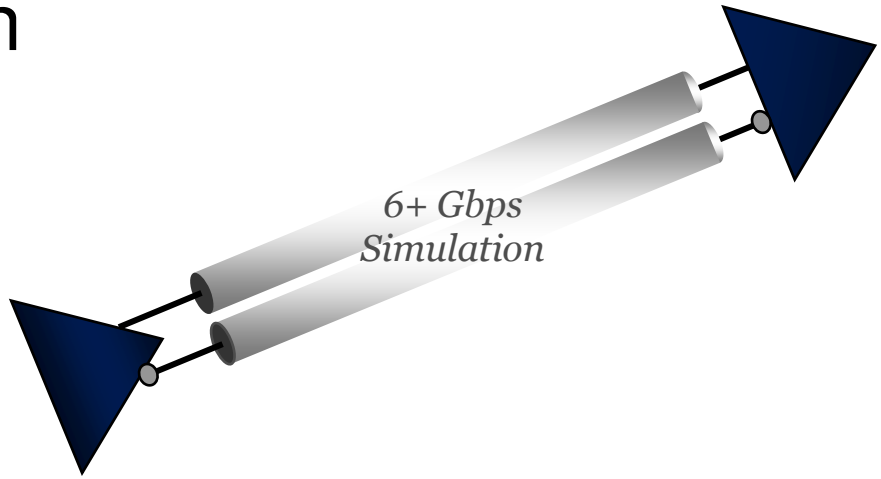




- Good height margin, and width fairly stable
- Create additional bundles to minimize tails and range
  - Power / System_complexity trade-off
- Simulation time: 2.5 days

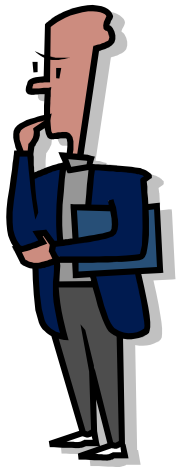
Agenda

- 6+ Gbps Simulation Process
- Modeling Techniques
- Link Simulation
- Summary



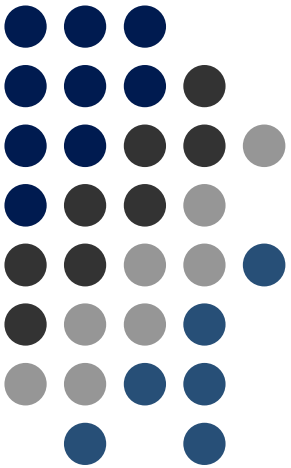
6+ Gbps Simulation Summary

- Accurate modeling = accurate simulation
- Cascade models, minimize discontinuities
- Accurate via modeling essential
- Measure to validate assumptions
- Approximate SerDes, as needed
- Test sensitivity to system variables
- Constrain performance limiters
- Create net/EQ bundles
- Exhaustively simulate manufacturing variations



THANK YOU

rev 1.1



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