Welcome to

25TH ANNIVERSARY

DESIGNCON® 2020

WHERE THE CHIP MEETS THE BOARD

Conference
January 28 - 30, 2020

Expo
January 29 - 30, 2020

Santa Clara Convention Center

Succeeding with Next-Generation AMI Models & Analysis

Panel Discussion: Wednesday January 29 2020, 3:34-5pm

Moderator: Donald Telian, SiGuys

Welcome to the 2020 AMI Panel Discussion

- **Moderator:**
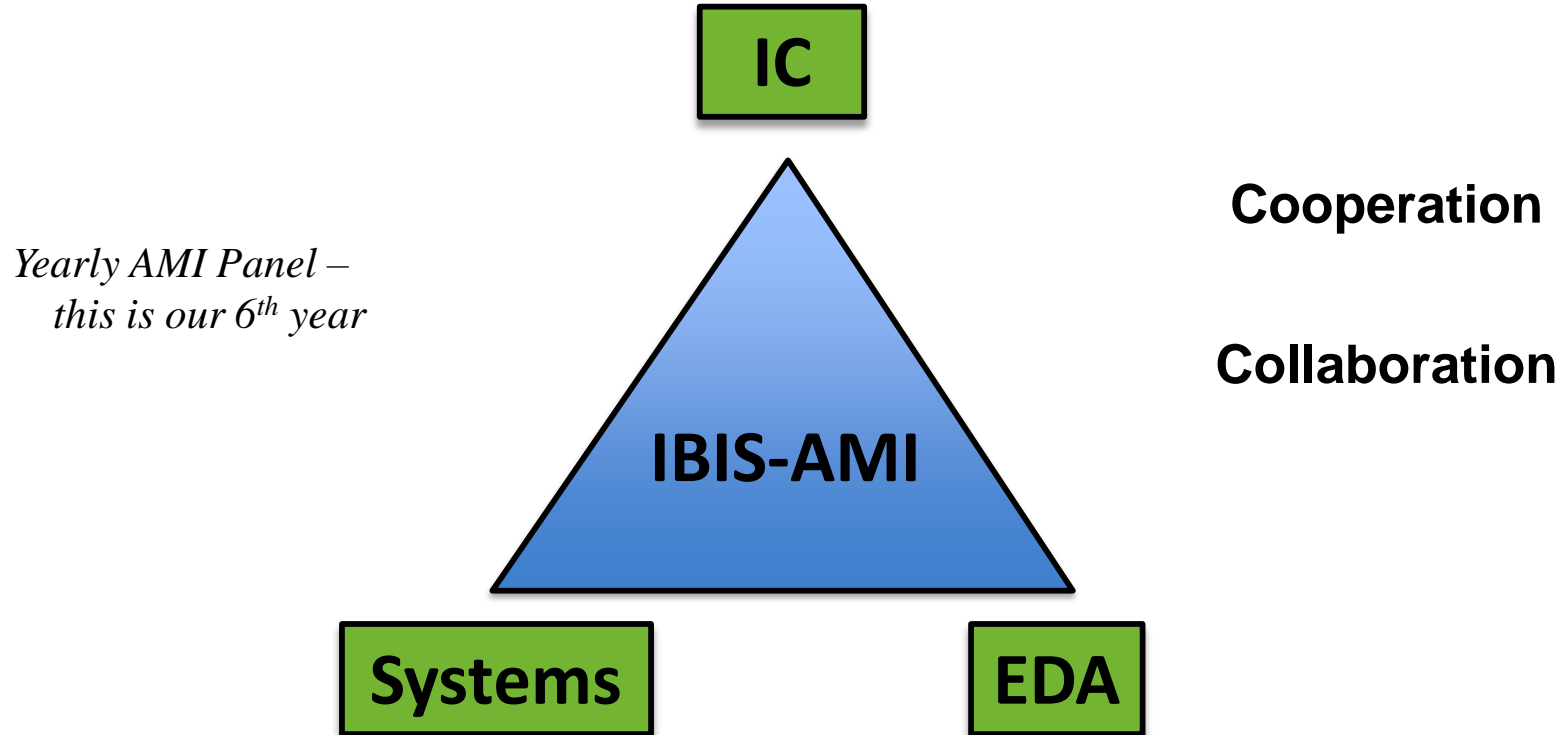 - Donald Telian, Signal Integrity Consultant / Owner, SiGuys

- **Panel Format:**
  - 5 Panelists
  - 4 questions
  - Timed response
  - Interruptions - flags
  - Audience questions

Succeeding with Next-Generation AMI Models & Analysis

Panelists

- **Stephen Scearce, Cisco**

- **Justin Butterfield, Micron**

- **Walter Katz, MathWorks**

- **Hsinho Wu, Intel**

- **Ken Willis, Cadence**

Introductions

Introduce yourself and your role at your company.

Outline your company's and your personal involvement with AMI models.
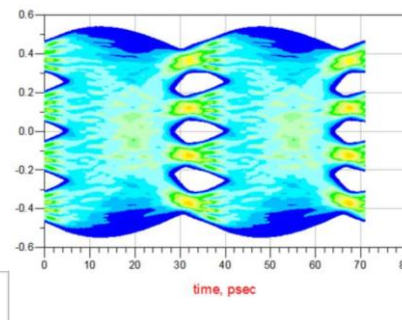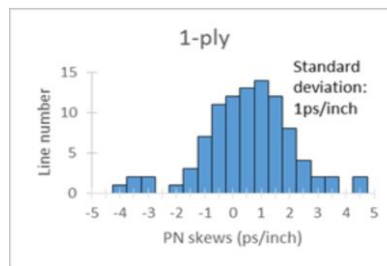
Stephen Scearce

Engineering Manager Cisco

SI/PI/EMC focused for 19 years

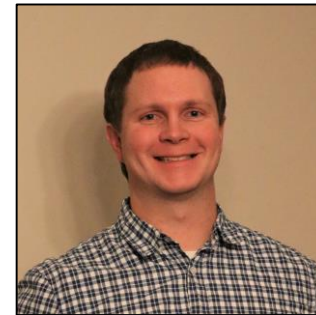- **Pre- Post Route: NRZ- > 56/112G Pam4**

- **System architectural investigation**

- **PCB Material selection**

- **Connector selection**

- **Potential VE Solutions**

- **HW Bringup settings**

- **Glass weave/skew effects**

Justin Butterfield

Senior Engineer,
Micron

Justin Butterfield, Senior Engineer for Micron Technology on the Silicon Signal Integrity team, has over 12 years of experience developing IBIS and HSPICE models for DRAM and NAND products. Throughout his career, Justin has created buffer models for aiding in the development and adoption of new memory standards, including ONFI 4, LPDDR4, LPDDR5, and DDR5. Justin is currently leading Micron's development efforts with IBIS-AMI models for DDRx interfaces. He received both his BSEE and MEEE degrees from Boise State University.

Walter Katz

Chief Scientist,
MathWorks (formerly SiSoft)

- I was one of the original developers of the IBIS-AMI standard along with Cadence, IBM, Texas Instruments
- I was part of team that developed QCD, an early and leading-edge IBIS-AMI simulator.
- SiSoft has been developing IBIS-AMI models for 12 years.
- Initially, SiSoft IBIS-AMI models were written in "C".
- For the last 4 years we have been working with MathWorks on a MATLAB/Simulink tool to develop IBIS-AMI Models.
- SiSoft has been acquired by The MathWorks
- We are demonstrating at our booth a third generation MathWorks IBIS-AMI model development tool "SerDes Toolbox" that supports both "Top Down" and "Bottom Up" SerDes Design and IBIS-AMI Modeling.
  - You do not often get the chance to start all over three times with a blank sheet of paper!

Hsinho Wu

Design Engineer,
Intel

Dr. Hsinho Wu is a design engineer at Intel Corporation's Programmable Solutions Group. He presently works on high-speed communication systems of FPGA products. His development and research interests include signal integrity, clock and data recovery, equalization, device and system modeling, simulation techniques, and software architecture.

Special thanks for contributions from Michael Mirmak, Mike Peng Li, and Masashi Shimanouchi

Ken Willis

Product Engineering Architect, Cadence

Ken Willis is a Product Engineering Director focusing on SI solutions at Cadence Design Systems. He has over 25 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

Overview of Cadence Involvement with IBIS-AMI

- Introduced the first commercial channel simulator in 2004
- Co-authored definition of the AMI extension to IBIS in 2007
- Helped customer develop and correlate the industry's first AMI model
- Currently develop and distribute IBIS-AMI models for Cadence SerDes and DDR IP
- Help customers use SystemSI and AMI Builder to develop and simulate with IBIS-AMI models

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AGENDA

- **Panelist Questions**

  ○ AMI Accessibility

  ○ AMI & IBIS 7.0

  ○ AMI & Serial Links

  ○ AMI & DDR5

- **Audience Questions**

IBIS-AMI Panel Discussion

Question 1

AMI ACCESSIBILITY

**Now that AMI models are generally available,
when will they become accessible using click agree/download?**

…what can be done to move towards this?

AMI ACCESSIBILITY – Intel's view

- **Now that AMI models are generally available, when will they become accessible using click agree/download?**
  - Probably *never*, because:
    - AMI models always contain some sensitive info, e.g. IP, margins
    - AMI is said to be safe but never guaranteed
    - Legal protection, e.g. using NDA, plus user authentication, e.g. register/login, still remain the best option

AMI Accessibility

- **Seeing some progress, and some conflict**
- **Cadence IP still requires NDA to provide AMI models**
- **Provided typically as part of IP purchase deliverables**
- **IP customers (provide chips) want to pass those AMI models along to systems customers with minimal hassle, post on websites, etc.**
- **This is an area where IBIS could add lot of value, encouraging suppliers to post models on IBIS website as central repository**

Question 1, AMI ACCESSIBILITY -> Never!

- **Executable models with IP protection**

- **Exposes the basic capability of the Serdes**
  - AGC/CTLE/DFE/RXFFE/….
  - Compensation/Jitter/Adaptation
- **IP competitive advantage $$**

- **Can't track usage or users**
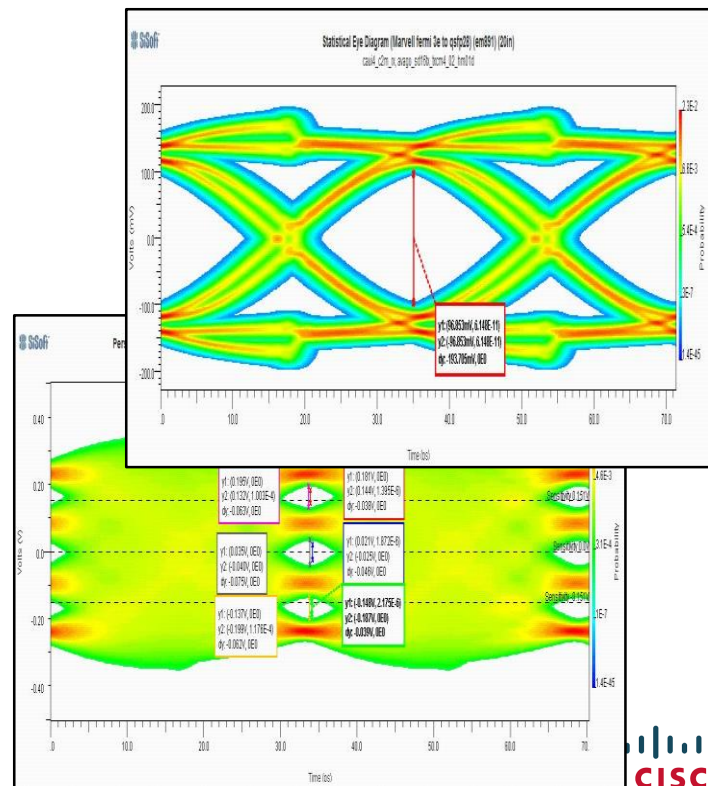
Micron IBIS-AMI Availability

DDR5

Models available with silicon

Models will be posted on micron.com
- Dependent on DDR5 JEDEC specification release

Design ins starting in 2020
- https://www.micron.com/ddr5 for more info

LPDDR5

Models will be on micron.com
- Require an account and NDA

GDDR6

Models on request through Micron representative

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1: AMI ACCESSIBILITY

- **Short answer: Never for all vendors.**
- **Using NDA/download IC**
  - Here now.
- **Using click agree/download**
  - Here now (varies by vendor)
- **Generic model available from EDA vendors.**
  - Here now

Question 2

AMI & IBIS 7.0

IBIS 7.0 recently released significant changes for component-level interconnect modeling. How will this change improve next-generation models and analysis? Are enough noise sources included in the models and analyses? What's working, and what's missing?
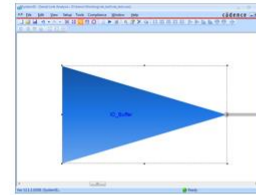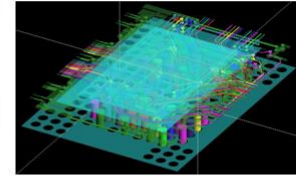
Interconnect Modeling

- **IBIS does not add value by legislating format for this, should stick to active device modeling**
- **Spice & S-parameters around for a half century**
- **No need to re-invent interconnect modeling**
- **Leave interconnect modeling and hookup to the EDA tools**

• IO Buffer

• Interconnect

← IBIS spec domain | EDA tool domain →

Question 2 AMI & IBIS 7.0

Improve next-generation models and analysis? **- >> YES**

- Formalization of what EDA vendors have used work arounds to support
- Adds structure/good habits for all EDA tools
- Increases model portability between tool platforms
- Improved PDN modeling on Die/Package [New Bird 198 needed to further improve this]
- Supports Touchstone and IBIS-ISS
- Link Training/ Backchannel support

▪ Are enough noise sources included in the models and analyses?

- Need to define the spectral content or of the Rj Components
- Noise sources for ADC/SA-ADC, quantization, voltage ref, Circuit Noise, RX-FFE noise gain

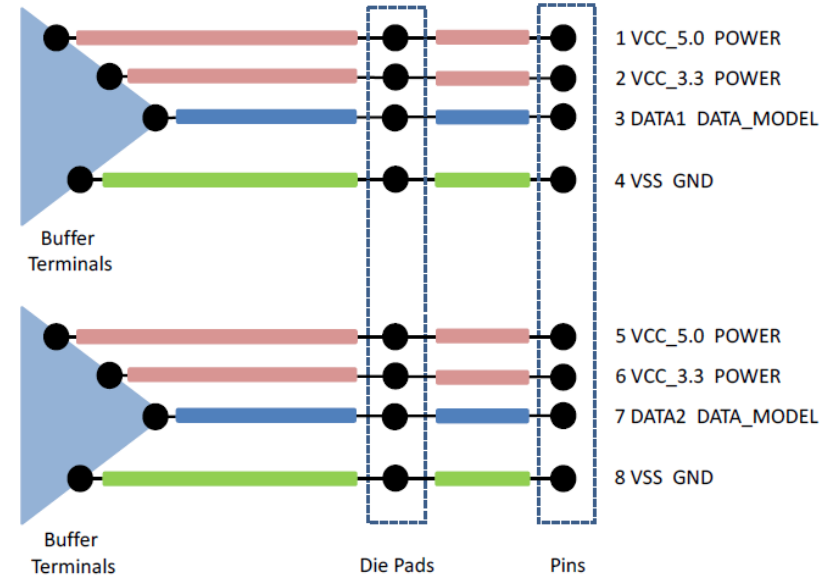# Much Needed IBIS 7.0 Features

Interconnect modeling

Enables IBIS to reference interconnect Spice and S-parameter models

Separate package and on-die interconnect models

- LPDDR5 will utilize on-die interconnect signal breakout

PDN modeling

- Power supply rail connections across package pins, die pads, and buffer terminals
- Decoupling models connected directly with the new syntax

Buffer Terminals		1 VCC_5.0 POWER
		2 VCC_3.3 POWER
		3 DATA1 DATA_MODEL
		4 VSS GND
		5 VCC_5.0 POWER
		6 VCC_3.3 POWER
		7 DATA2 DATA_MODEL
Buffer Terminals	Die Pads	8 VSS GND
		Pins

http://www.ibis.org/ver7.0/ver7_0.pdf

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2: AMI & IBIS 7.0

- **IBIS 7.0 recently released significant changes for component-level interconnect modeling. How will this change improve next-generation models and analysis?**
  - With IBIS 7.0 we will have accurate broadband package models.
  - In IBIS 7.1 we will have accurate broadband models for 112 Gbps modules.
- **Are enough noise sources included in the models and analyses? What's working, and what's missing?**
  - Maybe.
    - ADC/DSP introduce possible new jitter and noise sources due to four or more ADCs at1 UI spacing.
  - With IBIS 7.1 enhancements we will have all of the tools necessary to analyze DDR5 and 112Gbps and 224Gbps channels.

AMI & IBIS 7.0 – What's working / missing?

- **Component-level interconnect modeling in IBIS 7.0**
  - o Right time for the right technology!
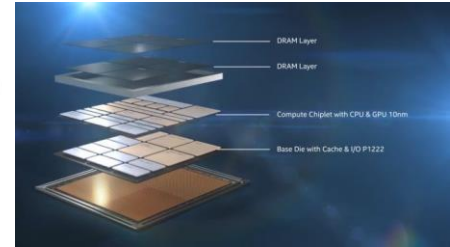
- **IBIS-AMI should beef-up noise modeling support**
  - o PAM-n is constrained in both timing and amplitude margins
  - o Can I simulate interference tolerance test using IBIS-AMI platform?

Platform	Noise Parameter	Description	Unit	Distribution/ Bandwidth
IBIS-AMI	Rx_Noise, Rx_GaussianNoise	Receiver output noise	V_{rms}	White Gaussian, no bandwidth specification
	Rx_UniformNoise	Receiver output noise	V_{peak}	Uniform distribution, no bandwidth specification
	n/a	Crosstalk	n/a	Crosstalk is directly simulated in IBIS-AMI
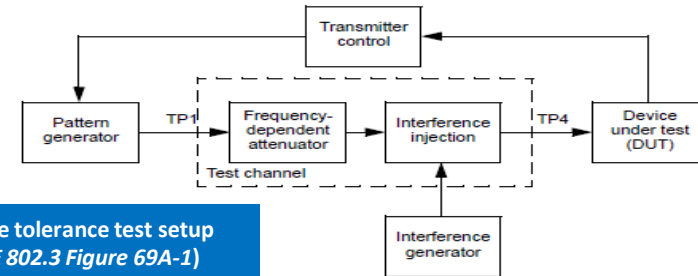
Interference tolerance test setup
(*from IEEE 802.3 Figure 69A-1*)

Question 3

AMI & SERIAL LINKS

What is the new thing in SerDes? How is Rx FFE changing analysis and performance? Will back-channel / system-level optimization help us ratchet up data rates? …and can it be modeled efficiently and effectively?

112 Gbps PAM4. What changes will be handled internally by the models and tools? How can attendees prepare for this?

What about the needs of ADC-based SerDes, will clock-centered sampling work or should the Rx model determine link margin internally?

AMI & SERIAL LINKS

- **The new things in SerDes?**
  - Statistical back channel optimization
  - RX ADC/DSP
  - Quantized FFE/DFE with ADC architectures
  - Floating DFE taps
- **How is Rx FFE changing analysis and performance?**
  - Optimizing an FFE not as easy as optimizing a DFE
  - Rx FFE preferred over Rx DFE to improve performance, especially with ADC/DSP
  - FFE + DFE + CDR convergence in time domain is a challenge.
- **Will back-channel optimization help us ratchet up data rates?**
  - Yes. Back channel control loop software will be used to design training algorithms to get better solutions. We are exploring different optimization methodologies including gradient search, artificial intelligence, machine learning, and simulated annealing in addition to intelligent sweeps.
- **…and can it be modeled efficiently and effectively?**
  - Yes. This is a problem we are focused on, but it is challenging. What is the metric being optimized? What kind of metrics can be implemented in the hardware?
- **112 Gbps PAM4. What changes will be handled internally by the models and tools? How can attendees prepare for this?**
  - Control loops/training will change. Metric will use COM (Signal/Noise ratio) instead of eye height or eye area.
  - Many FFE, DFFE taps (up to 100).
  - ADC/DSP
  - Until vendors supply AMI models, use EDA tool supplied generic models.
- **What about the needs of ADC-based SerDes, will clock-centered sampling work or should the Rx model determine link margin internally?**
  - ADC part is easy. Outputting 1 sample per UI in GetWave breaks the standard AMI time domain flow. In software we can do N samples per UI, and then pick the one sample per UI in the center of the eye. Hardware CDR not so simple.
  - Challenge is to model noise and jitter using time-interleaved ADCs, common in 112Gbps architectures,
  - Does the Rx determine the link margin, or does the AMI standard need to be enhanced to enable the simulator to determine the link margin.

AMI & SERIAL LINKS – Intel's aspects

▪ **Transition of SerDes and EQ architecture at 106/112Gbps**
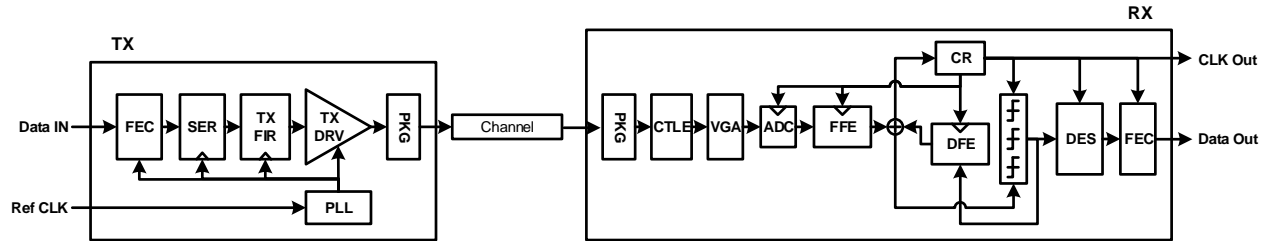
○ Analog-based ⇒ ADC-based; DFE heavy ⇒ FFE heavy; FEC's dependency on EQ types/characteristics
  • *To achieve required link performance with shortened symbol width under PPA* consideration*
○ Will not impact IBIS-AMI simulation/analysis flow as long as standards still have per-FEC BER spec.

▪ **FFE is LTI which can be modelled/simulated using convolution in waveform (analog) or in symbols (DSP)**

○ No new "skills" is needed for modeling or analysis

*: Power, Performance, and Area

- **ADC-based RX is run on ADC clock so no physical eye diagram, but**
  - o An equivalent eye diagram can be generated using post-FFE/DFE symbol output
    - *assuming that it is already centered at RX's recovered clock ticks*
  - o IBIS-AMI simulator, therefore, can show the eye and perform post-sim analysis
    - *However, RX model can do the analysis internally without generating the equivalent eye diagram…*

RX DSP Output

RX Equivalent Eye

ADC / CDR Clock
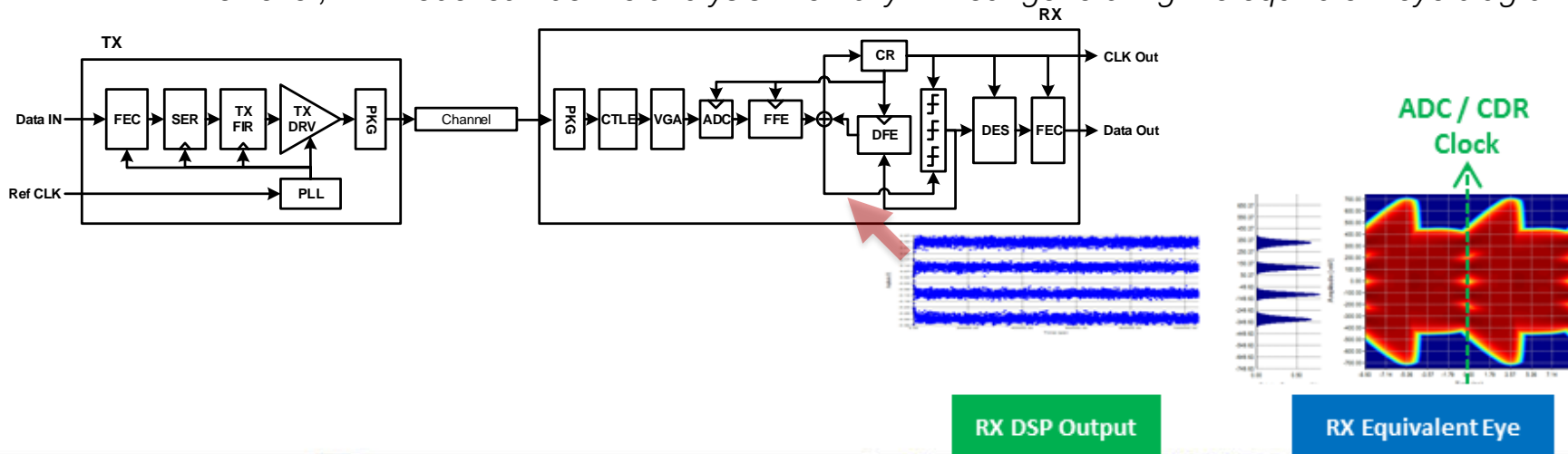
What's New in SerDes-land?

- **PAM4 – capable AMI models are a challenge**
- **FFE in Rx changes the game**
  - ○ Lots of FFE taps, fewer DFE taps
- **Tx FFE remains critically important to give the Rx something to work with**
- **If Tx does not have strong self-optimization, backchannel also becomes very important**
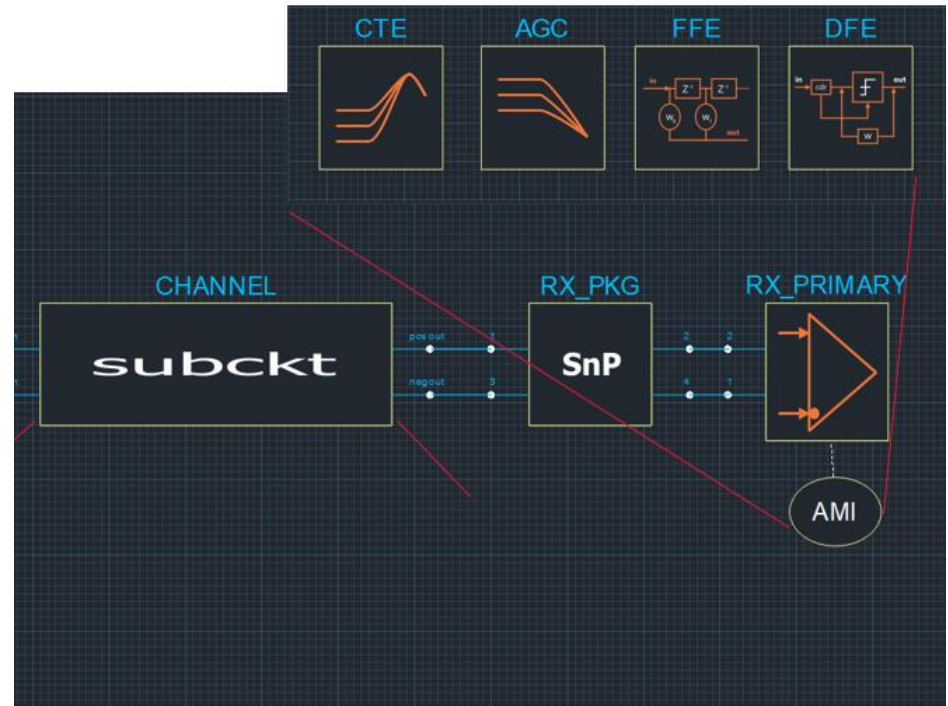


Over-arching driver remains PPA (power/performance/area)

112Gbps PAM4

- **Expect 112Gbps data rate to have long shelf-life**
  - Unclear after that for copper PCBs
  - Interposer-based interconnect may become more prominent
- **ADC is power-hungry**
- **Clock-centered digital sampling is the name of the game**
- **CDR is absolutely critical to pick optimum sampling point**
- **AMI models can output insightful data**

RX Center Plot
len17_agc_adapt_P4

RX Center Plot, Histogram
len17_agc_adapt_P4
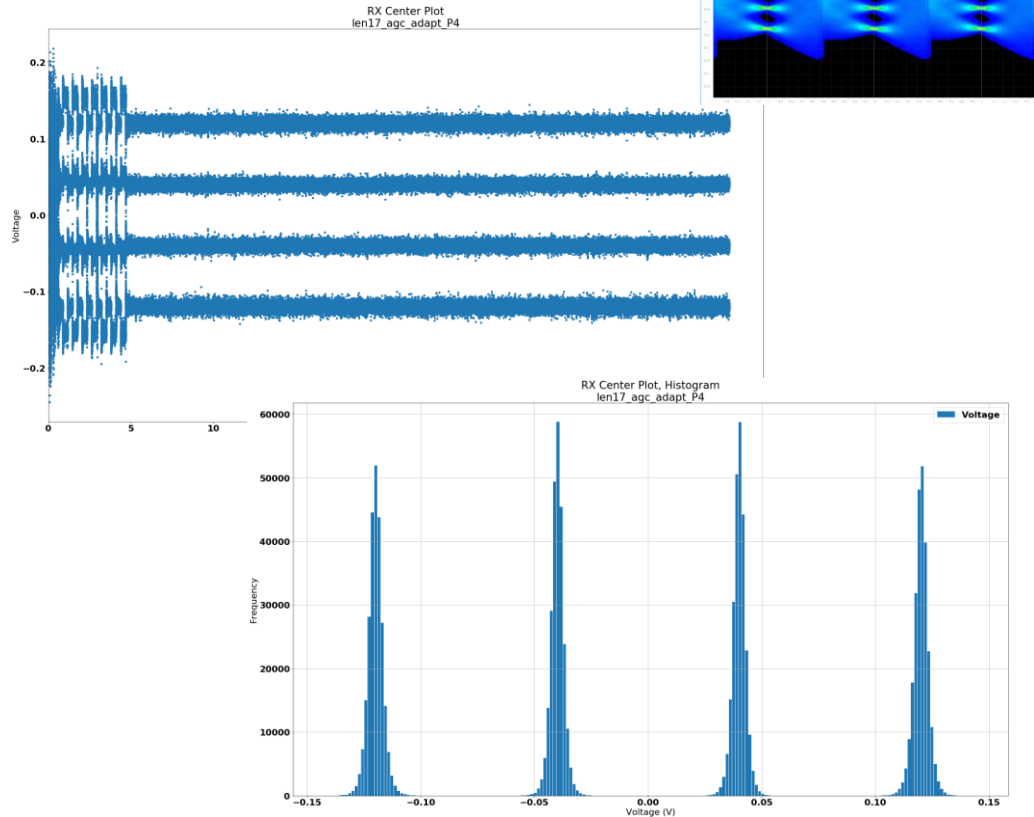
All About Errors

- **IEEE standards allow 4 bit errors per 10k bits**
- **DFEs can create burst errors, hence shift to more FFE-based Rx**
- **Errors are expected, and it's expected that FEC will handle them**
- **Virtual BERT becomes gospel vs. traditional bathtub analysis**
- **Should see more innovation (i.e. machine learning) around new EQ architectures**

Question 3, AMI & SERIAL LINKS
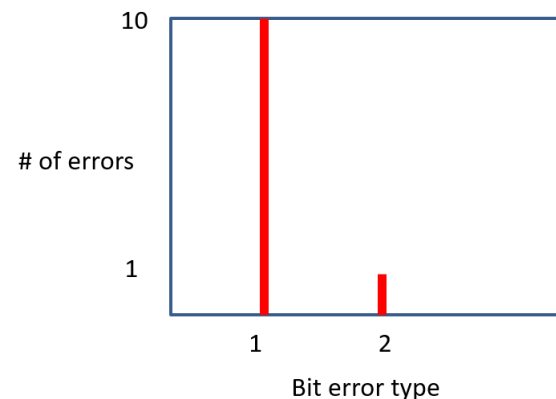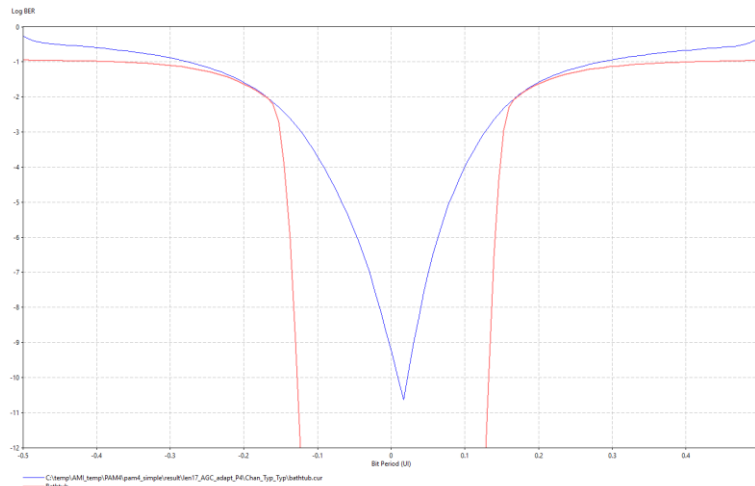
- ■ **Industry Serdes Focus:**
  - Power optimization/ channel type   * Focus on multi rate /10-56, 56-112/224Gbps
  - XSR, USR for MCM/Multi die   * ADC-DSP architectures

- ■ **Receive Equalization DFE (Mixed Signal) vs Rx-FFE (ADC) :**
  - Mid Loss High Crosstalk- DFE Based   *High Loss/Skew Low Crosstalk-ADC/FFE Based
  - Ami facilitates modeling of the higher level RX functions for both DFE/RxFFE
  - Backchannel-> FFE and DFE Co-Adapting, not as critical for systems with RX-FFE

Question 3, 112+ Gbps PAM4 Cisco View

Channel Optimization Margin - > Channel Evaluation
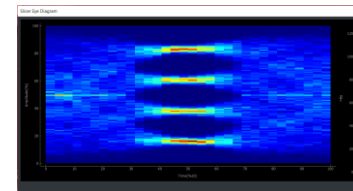
SERDES Test Chip Evaluation ->Temp/Voltage/Channel
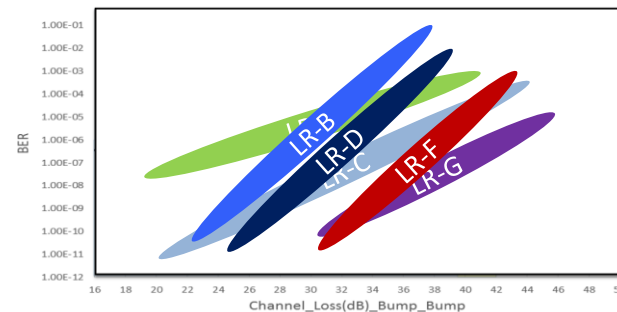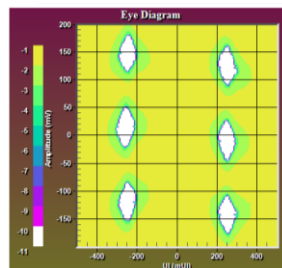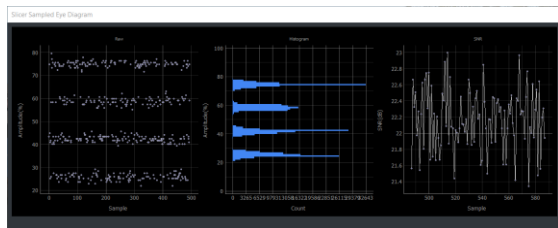
www.ieee802.org/3/ck/public/tools/tools/mellitz_3ck_adhoc_01_120419_COM2p76.zip

Intersecting of SerDes and DDR

Next generation DDR target data rates
DDR5 – 6.4Gbps
LDDR5 – 6.4Gbps
GDDR6 – 16Gbps

Why in the world are we still using single-ended signaling for memory interfaces?

DDR is starting to look more like SerDes
Equalization
BER
Jitter terms
Statistical simulation / PDA

Yet it's still different
Single-ended
Forwarded Clock
Multi drop channels restricted by reflections/ISI
Non-linear drivers

DRAM Channel Insertion Loss

https://ieeexplore.ieee.org/document/8741253
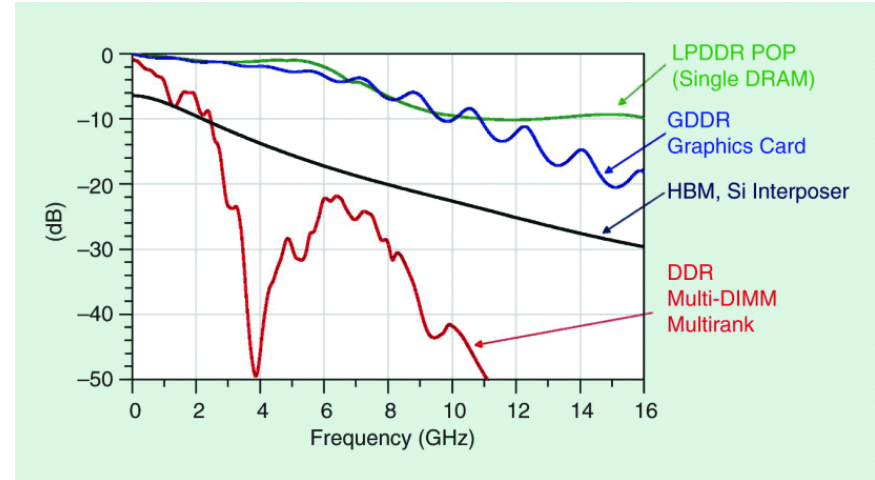
Required IBIS Features
For SerDes and DDR

- Interconnect modeling for subsystems
  - IBIS 7.0 interconnect models are limited to single die per channel packaged components
  - EMD (Electrical Module Description)
    - Replacement for EBD
    - Multi-chip packages, System in Package, DIMMs, SSDs, etc.
    - Models internal interfaces
- Backchannel for statistical
  - Co-optimize the Tx and Rx EQ in the statistical simulation flow
  - Can allow for much faster optimization searches
  - Support ability for the optimization to be controlled by either the Rx or the Tx
- Jitter spectrum
- Mechanism for modeling the frequency spectrum of jitter
- Jitter amplification in the device
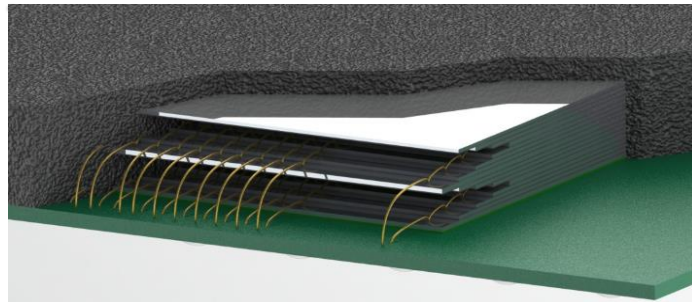
Question 4

AMI & DDR5

What is the timeframe for DDR5? …and is AMI responding quick enough to succeed as an analysis solution?

What is the correct solution for modeling DDR5's clock forwarding? Is there unanimous agreement on a single solution? …or do attendees need to be prepared for different methodologies?

3 min, jb, 4:30

DDR Forwarded Clock

Current Modeling Approach

DFE requires slicing of the data

Problem: DDR uses a forwarded clock to slice the data

Jitter alignment between data and clock result in an effective jitter

CDR can be used as approximation

Need to ensure CDR does not filter the jitter

Existing jitter parameters can be used as an approximation

Rx jitter for data + *Rx_Clock_Recovery* jitter for clock

As jitter budget is reduced, these approximations and worst case modeling reduce the simulation accuracy

- ~1ps accuracy not expected with current approach

Simulation methodology may depend on use case and level of detail required

- Jitter specifications vary per technology

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DDR Forwarded Clock
Looking Ahead

- Memory Jitter Characteristics
- Effective jitter is a function of the correlation between input clock and data jitter
  - Unmatched receiver forwarded clock
  - Multiple UI delay between clock (DQS) and data (DQ) slicer
- May be complicated and not represented by simple jitter terms
  - Jitter amplification in clock tree
  - PLL to synthesize the clock
- Challenges Including the Clock
- How to generate the clock
- Clock alignment
- Simulation flow
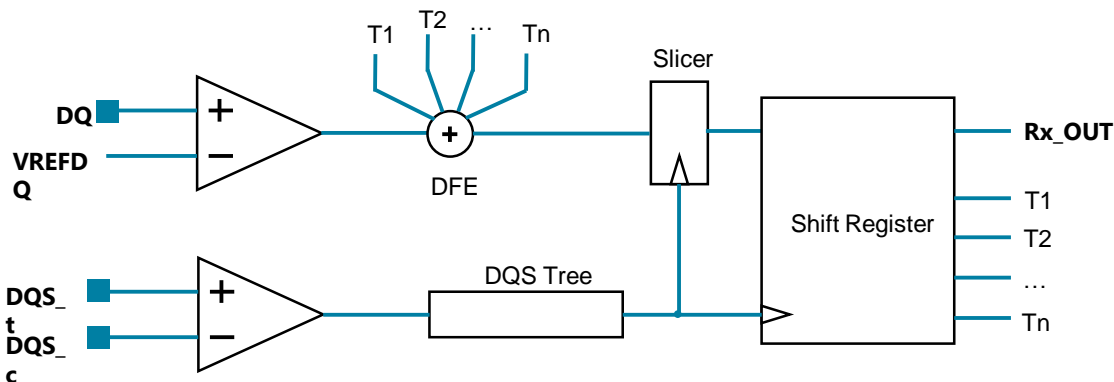
AMI & DDR5

- **What is the timeframe for DDR5?**
  - JEDEC compliant DDR5 IBIS-AMI(models available.
  - IC vendor memory and controller DDR5 AMI models expected in 2020
- **…and is AMI responding quick enough to succeed as an analysis solution?**
  - Yes!
  - DC_Offset BIRD has been approved, targeted for IBIS 7.1, Q3 2020
  - Statistical back channel BIRD, targeted for IBIS 7.1, Q3 2020
    - DDR5 DQ Protocol and independent task, not gated by IBIS release. Targeted for Q2 2020.
- **What is the correct solution for modeling DDR5's clock forwarding? Is there unanimous agreement on a single solution? …or do attendees need to be prepared for different methodologies? Solutions and methodologies.**
  - Today,
    - Characterize the DQS jitter with existing AMI parameters
  - Future BIRD enhancements
    - EDA tool supplies a DQS waveform along with DQ waveforms
      - Requires BIRD, none proposed at this time
    - AMI committees have asked controller and memory vendors for direction.

AMI & DDR5 – Intel's *request/preferences*

Our request/preferences in these areas

- **DC Offset solution**
  - BIRD 197

- **Clock (strobe) solution**
  - Separate buffer model or included in DQ?

- **Configure EQ with back channel and link margin assessment**
  - In Empirical (GetWave, supported in IBIS 7.0) mode, or Analytical (Init, BIRD 201) mode?
  - Who performs eye calculation: RX or tool? Who determines EQ is done?
  - Should perform optimization under noisy condition, i.e. include crosstalk (and jitter?)
  - Who performs eye calculation? Who should know jitter/noise details

AMI & DDR5

- **Introduced first DDR5 AMI models last DesignCon with Micron**
- **"True Strobe Timing" looks like right approach for DDR5**
  - o IBIS having trouble keeping up
- **At 16-20 Gbps may see phase interpolation in Rx to augment external strobe to mimic CDR functionality**
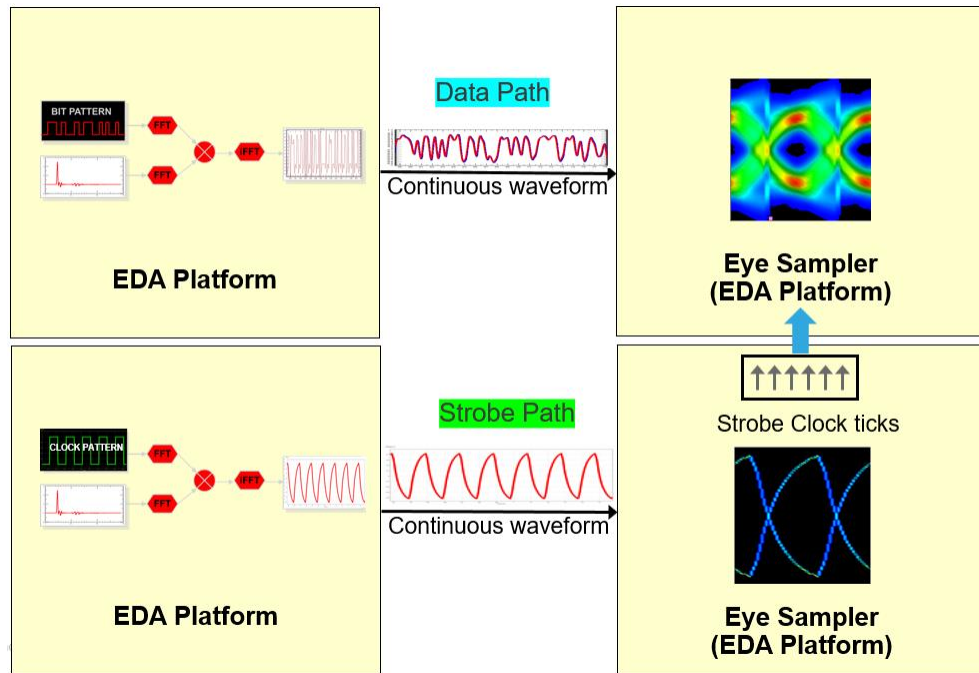
Question 4 AMI & DDR5

DDR5, Coming, Coming, …….Here!!

Channel A
DQ<40:0>

CA<13:0>

Channel B
DQ<40:0>
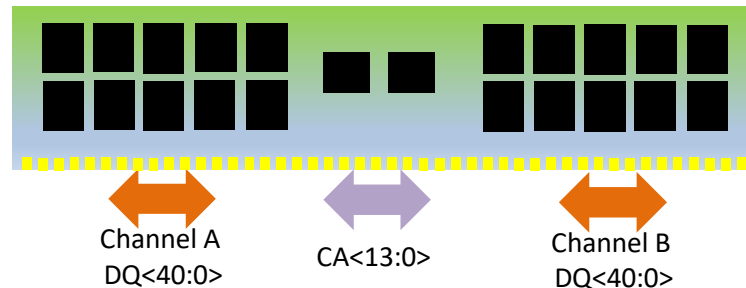
SEPTEMBER 2017
RAMBUS
ANNOUNCED A
WORKING DDR5
DIMM

NOVEMBER 15, 2018,
SK HYNIX
ANNOUNCED ITS
FIRST DDR5

FEBRUARY 2019,
SK HYNIX
ANNOUNCED A
6400 MT/S CHIP
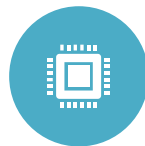
CES 2020: MICRON
ANNOUNCED
RDIMM SAMPLING
FOR SERVER

CES 2020: SK
HYNIX
DEMONSTRATED
RDIMM 4800
MT/SEC/PIN

JEDEC'S JC-42 IS
EXPECTED TO
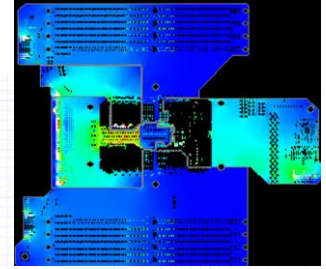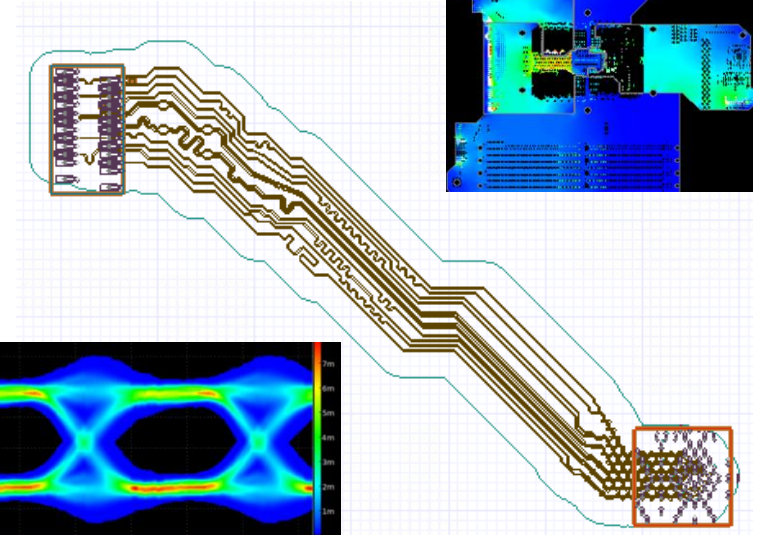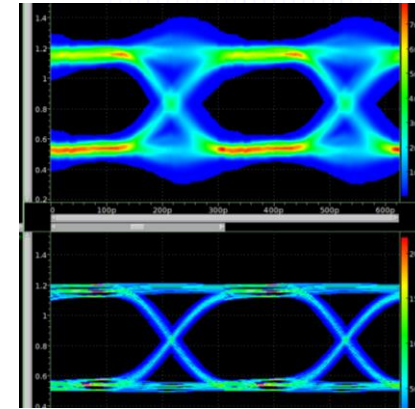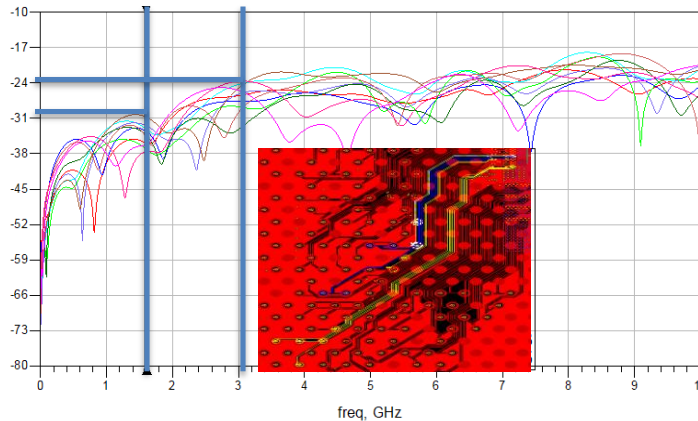CLOSE ON 1.0
MARCH 2020

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Question 4 AMI & DDR5

- DDR5 AMI forwarded clock CDR with but little jitter rejection/tracking

- Rx_Clock Recovery_Dj/Rj/Sj/DCD, RX jitter/RX_CLK_PDF

- BCI_Training_Mode (IBIS BIRD201) optimization/training

- Statistical sims required (1e-16 BER), need multi edge pulse response and transient bursts to match time domain data

- Track of absolute voltages, voltage offsets (IBIS BIRD197.7)

- Variation between rise and fall transitions, DCD correction
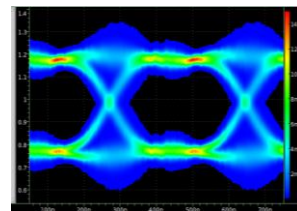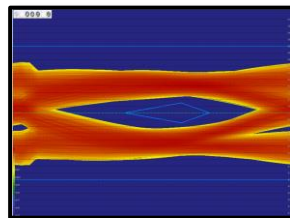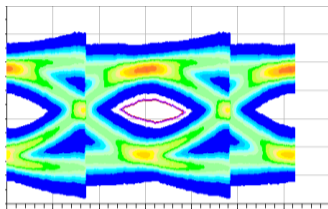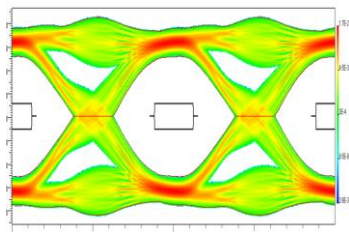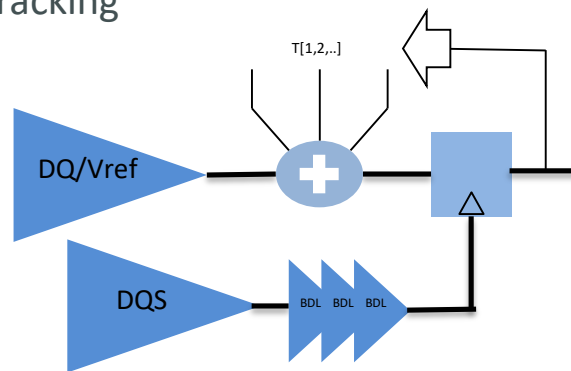
Question 4 AMI & DDR5 Challenges

- Single ended crosstalk for high density 3.2Ghz channels
- SSO effects
- PSI Jitter increase due to DQ to DQS Offset

AUDIENCE QUESTIONS

Thank you!