Welcome to

DesignCon® 2022

WHERE THE CHIP MEETS THE BOARD

Conference
April 5 – 7, 2022

Expo
April 6 – 7, 2022

Santa Clara Convention Center

AMI Models and the Seven-Year Itch

Panel Discussion: Tuesday April 5 2022, 4:45-6pm

Moderator: Donald Telian, SiGuys

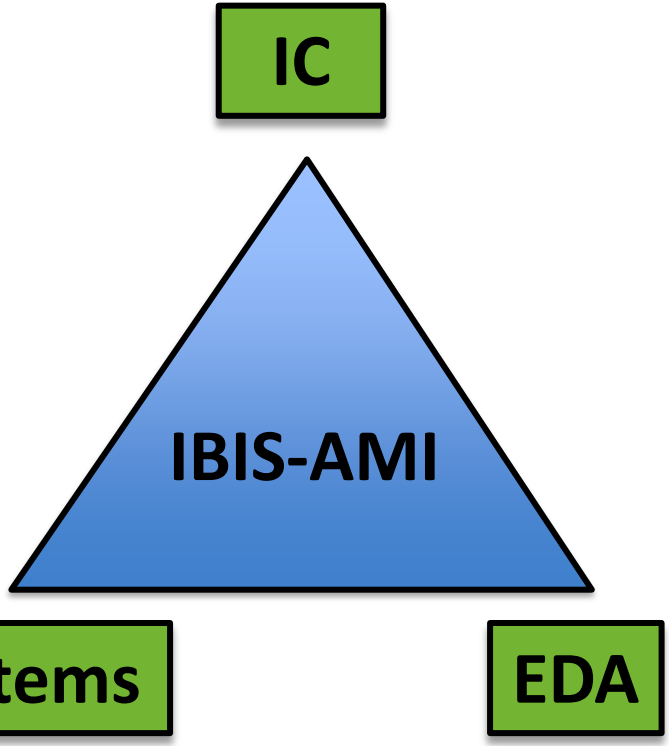
Welcome to the 2022 AMI Panel Discussion

- **Moderator:**
  - Donald Telian, Signal Integrity Consultant / Owner, SiGuys

- **Panel Format:**
  - 5 Panelists
  - 4 questions
  - Timed response
  - Interruptions - flags
  - Audience questions

AMI Models and the Seven-Year Itch

Yearly AMI Panel –
this is our ***7th year***



Cooperation

Collaboration

Panelists

- Ken Willis, Cadence
- Michael Mirmak, Intel
- Walter Katz, MathWorks
- Randy Wolff, Micron
- Aleksey Tyshchenko, SeriaLink Systems

Introductions

Introduce yourself and your role at your company.

Outline your company's and your personal involvement with AMI models.

kw 1 4:50

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Ken Willis

Product Engineering Group Director, Cadence

Ken Willis is a Product Engineering Group Director focusing on SI solutions at Cadence Design Systems. He has over 30 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

Michael Mirmak

Platform Applications Engineering Manager, Intel

Michael Mirmak is a Platform Applications Engineering manager and Technical Lead with Intel's Data Center and AI Group, supporting signal integrity (SI) modeling and analysis. He has been involved with SI since 1996. He is a past chair of, and an active participant in, the IBIS Open Forum, the organization that manages the I/O Buffer Information Specification and the Touchstone specification. He is co-author, with Dave Coleman, of the book Mastering High Performance Multiprocessor Signaling. Michael received a BSEE from the University of Pennsylvania.

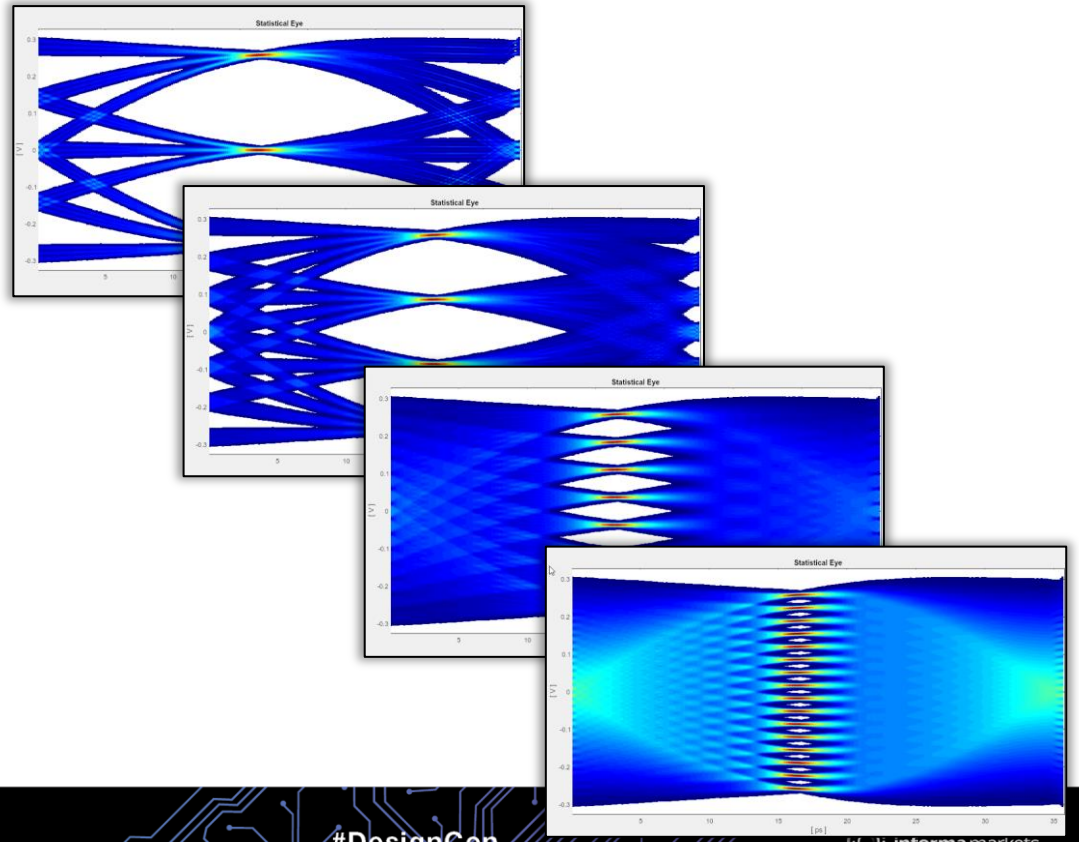
Walter Katz

Chief Scientist, MathWorks

- I was one of the original developers of the IBIS-AMI standard along with Cadence, IBM, Texas Instruments
- I was part of team that developed QCD, an early and leading-edge IBIS-AMI simulator.
- MathWorks/SiSoft has been developing IBIS-AMI models for 14 years.
- Initially, IBIS-AMI models were written in “C”.
- For the last 6 years we have been working with MathWorks on a MATLAB/Simulink tool to develop IBIS-AMI Models.
- We are demonstrating at our booth a third generation MathWorks IBIS-AMI model development tool “SerDes Toolbox” that supports both “Top Down” and “Bottom Up” SerDes Design and IBIS-AMI Modeling.

Introduction – What I Have Been Working on

- IBIS Standard Improvements
  - PAM-n
  - Interconnect modeling
    - Package
    - Modules (EMD)
    - PCB
  - DDR5, GDDR7, & AMI modeling
  - Statistical backchannel
- Optimization/Training Algorithms



Randy Wolff

Principal Engineer,
Micron

Randy Wolff is a principal engineer at Micron Technology within the Silicon SI team of Micron's Signal Integrity R&D group. He developed Micron's IBIS and SPICE modeling program and most recently is creating IBIS-AMI models for multiple products. He is currently the Chair of the IBIS Open Forum committee and served in the Secretary role from 2003-2019. Randy graduated cum laude from Montana State University with a BSEE degree in 1999 and is a senior member of IEEE.

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Aleksey Tyshchenko

Co-Founder,
SeriaLink Systems

Aleksey Tyshchenko, Ph.D., is a co-founder of SeriaLink Systems – a consulting team focusing on system modeling of high-speed serial links, IBIS AMI modeling, model correlation and system validation. SeriaLink Systems is working on building a configurable modeling flow to support SerDes projects through their entire life cycles: from architecture definition, through analog and digital design, to design validation. He has been working on behavioral modeling of high-speed SerDes systems, architecture analysis, adaptation and signal integrity with multi-standards SerDes IP teams at V Semi and Intel. His Ph.D. research at the University of Toronto, Canada, focused on CDR systems for high-speed ADC-based receivers.

AGENDA

- **Panelist Questions**
  - AMI 7-Year Report Card
  - AMI & Serial Links / 112 Gbps
  - AMI & DDR5
  - AMI Swimming Upstream?
- **Audience Questions**

Question #1

7-year Report Card:

How is AMI doing? A+ or D-?

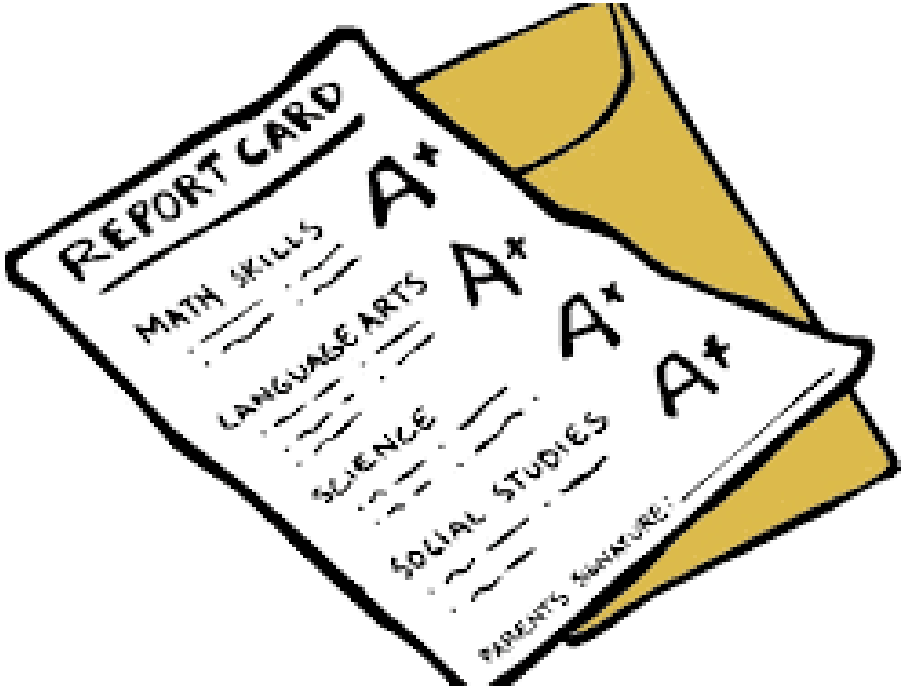
Can we count on AMI going forward?

We envisioned AMI reference models from Serial Standards and use of AMI executables within T&M tools, but it hasn't happened. Why? Or has it?

mm 2 4:55

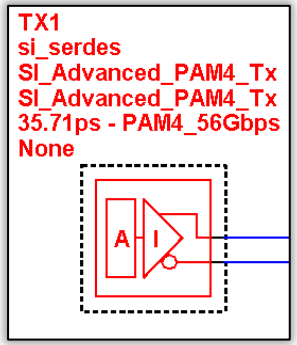
Responses from Michael Mirmak

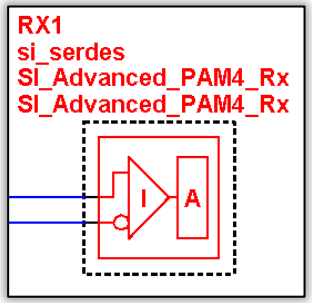
- **Personally, I would give IBIS a B**
- **It helps to keep some perspective**
  - Mid-2015: industry still operating on IBIS 6.0
  - Since then, added backchannel statistical and bitstream operation, and PAM4 support
  - Traditional IBIS was expanded to add complex C_comp, plus IBIS-ISS and Touchstone support for packages
- **Why not an A+?**
  - Re-driver and re-timer support have lagged industry needs (arguably since PCI Express* 3.0 in 2010 and 4.0 in 2017)
  - Our problems are now more in what IBIS does not define explicitly, such as backchannel protocols
  - More on this later in the panel discussion…



IBIS-AMI: 7-year Report Card

- How is AMI doing, and can we count on it going forward?
  - A+: Assuming good AMI models are delivered





- We've envisioned AMI reference models from Serial Standards and use of AMI executables within T&M tools, but it hasn't happened. Why?
  - Serial link standards do not want to include in their standard simulation
  - T&M tools already have generic equalization built into the hardware

MathWorks

7-year Report Card

- Micron is a relative newcomer to the IBIS-AMI ecosystem
  - SerDes NAND FLASH interfaces
    - Model user experience
    - Grade: A- (IP protection issues)
  - DDRx single-ended signaling with equalization
    - Model developer experience
    - ~3 years into development in close collaboration with EDA vendors and IBIS community
    - Grade: B (Clock modeling needs attention)

Q1: 7-year Report Card

- How is AMI doing? A+ or D-?
  - A
  - AMI serves its main purposes very well: it enables simulation-based technical interaction between teams
  - Better compatibility and consistent results across EDA tools would make it A+
- Can we count on AMI going forward?
  - Definitely
  - AMI needs to keep evolving to reflect emerging SerDes architectures and link topologies
- We envisioned AMI reference models from Serial Standards and use of AMI executables within T&M tools, but it hasn't happened. Why?
  - Standards remain implementation neutral
  - That is a blessing and a curse at the same time
  - Configurable or parametric approach to AMI modeling might be the right compromise here
  - If the AMI model could have a switch between "Reference" and "Actual Design" operating modes…

Question 1: 7 Year Report Card

- **A to A+ overall !**
- **Modeling has moved from a couple consultants building models to multiple tools that enable whole industry**
  - Biggest challenge seems to be understanding high-level behavioral modeling vs. circuit-level minutia
- **AMI simulation support is widespread**
- **Reference EQs are described in specs, but have to build models ourselves**
  - Cooperation with other standards bodies would be a big benefit
- **Too much hard-coded constructs and "death by keyword" in recent IBIS**
- **Should keep original principle to separate EQ and interconnect**

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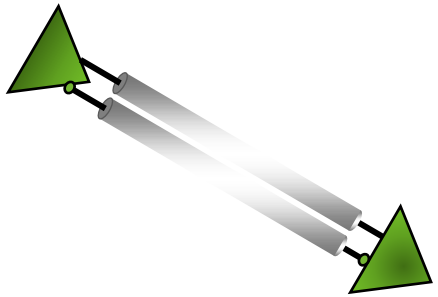
Question #2



Serial Links / 112 Gbps:

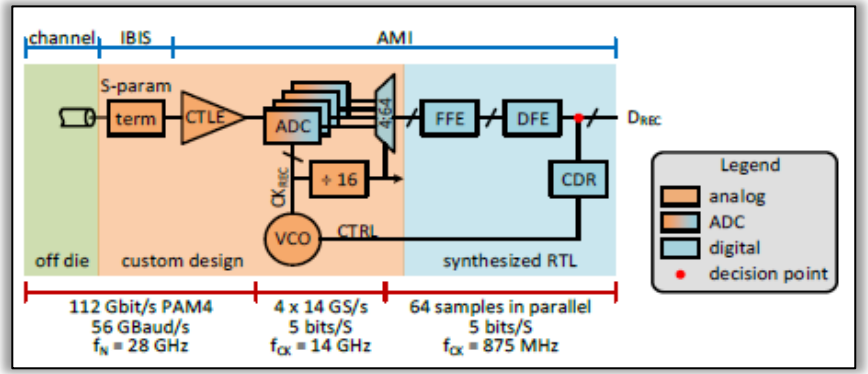
Tell us about the new problems and solutions here.

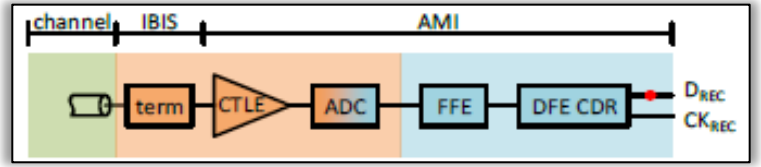
What do we need to know about developing products using these next-generation standards?

wk 3 5:05

IBIS-AMI: 112 Gbps

- Tell us about the new problems and solutions here. What do we need to know about developing and using these next-generation models?
  - 112 Gbps Rx equalization
    - CTLE front end
    - Multi-tap FFE and a DFE
  - There are two classes of Rx AMI models
    - Complex AMI models
    - Simpler behavioral models
  - A significant problem is how does the hardware, firmware, or EDA tool optimize/train channel with ~30 knobs to train?





Serial Links

- Making use of Ts4file for SerDes (UFS/PCIe FLASH sub-system interfaces)
  - Capturing all on-die analog characteristics including ESD loading, T-coils, terminations, routing parasitics

10.10.1 TRANSMITTER ANALOG CIRCUIT

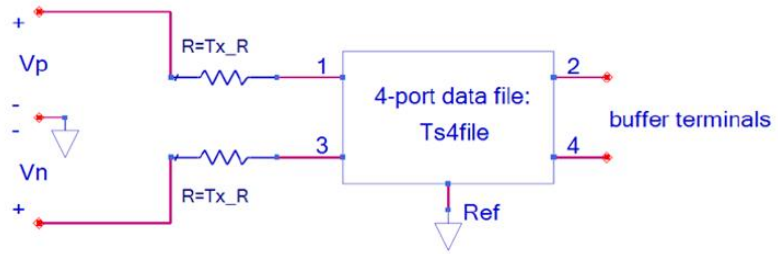


Figure 42 – Transmitter Analog Circuit

10.10.2 RECEIVER ANALOG CIRCUIT

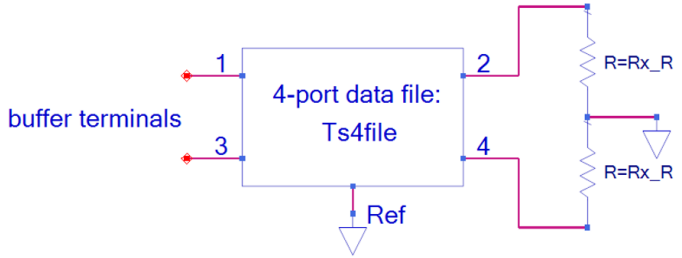
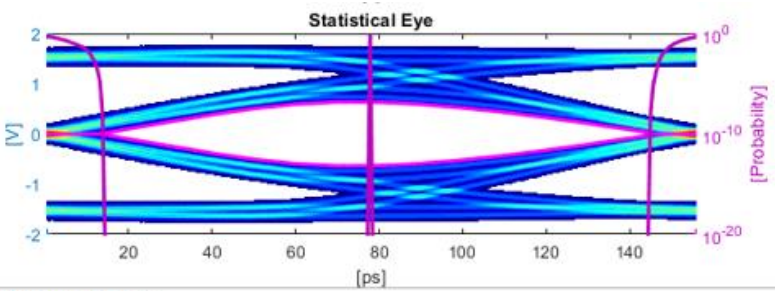


Figure 46 – Receiver Analog Circuit

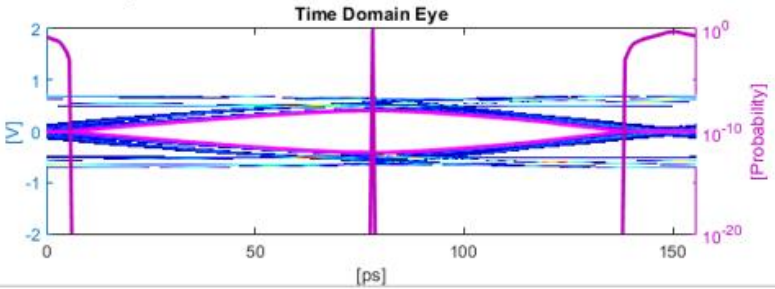
Serial Links

- Equalization adaptation algorithms in Init vs. GetWave
  - A non-linear effect such as gain saturation can make a large difference in adaptation solution and final eye characteristics
  - SerDes Rx may have small gain saturation due to limited voltage swing
  - Single-ended Rx (e.g., DDR5) can have significant gain saturation depending on Vref bias level



Statistical Metric	Data
Eye Height (V)	1.2435
Eye Width (ps)	132.5666
Eye Area (V*ps)	104.5662
COM	6.4645
VEC	5.5983

Time Domain Analysis



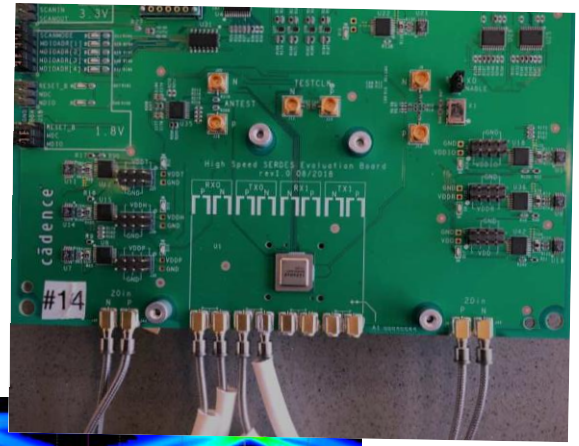
Time Domain Metric	Data
Eye Height (V)	0.7858
Eye Width (ps)	133.0576
Eye Area (V*ps)	64.5841
COM	11.8682
VEC	2.5572
Minimum BER	5.2632e-04
Ignore Symbols	100
Total Symbols	2000

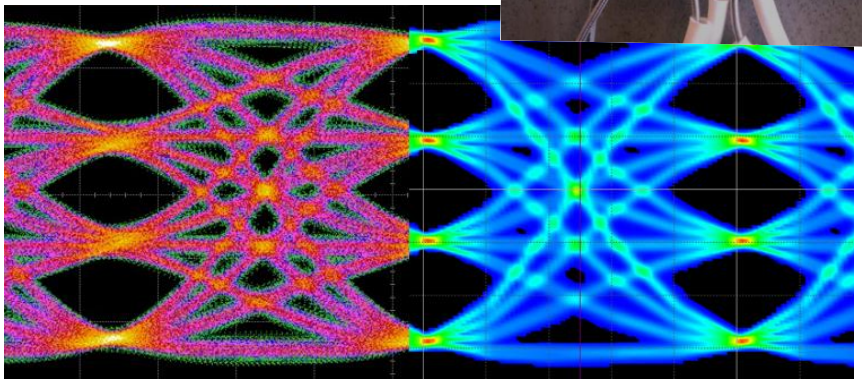
Q2: Serial Links / 112 Gbps

- **Tell us about the new problems and solutions here**
  - **ADC-based SerDes architectures are a challenge for AMI**
  - **We took two alternative approaches to work through these challenges**
    - **Functionally-representative models abstract the RX architecture to simplify the model interface**
    - **Architecturally-representative models capture the RX architecture with a non-trivial interface solution**
  - **MLSE adds a new dimension of challenges to ADC-based SerDes modeling**
  - **Join us on Thursday at 3pm to hear all about it**
- **What do we need to know about developing products using these next-generation standards?**
  - **It's not going to get any easier as we keep pushing the data rates**
  - **SI workflow must be responsive to SerDes architectural trends, new equalization techniques, link topologies**
  - **Interaction between FEC and SerDes, opto-electrical co-simulations, SerDes – channel co-optimization**
  - **Earlier AMI model availability is likely to be highly appreciated**
  - **AMI models need to evolve with SerDes and channel development throughout the project**

Question 2: Serial Links / 112 Gbps

- **Most of the EQ principles from PAM2 are applicable to PAM4**
- **Some new wrinkles for multi-level signals**
  - Multiple feedback loops
  - FFE inside of DFE module
  - Eyes can be closed and still meet spec!
- **Some questions remain:**
  - Include FEC in sims or not?
  - BERT approach?
- **Expect PCI Express Gen6 to bring some of these issues to the mainstream**





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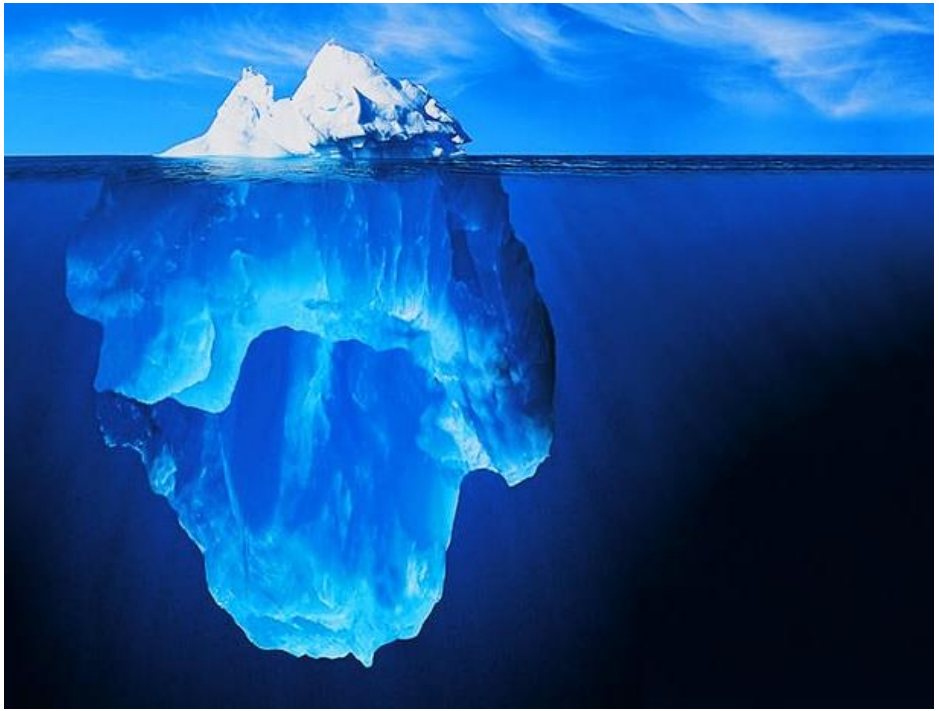
Responses from Michael Mirmak

- **Big problems are still present at lower speeds (e.g., PCI Express* 5.0 at 32 GT/s)**
  - Use: Simulation times for bitstream operation can make models unusable for HVM studies
  - Generation: Not everyone knows how to create dual models that have a high degree of correspondence between modes… and this isn't easy to achieve!
  - Specification: Can't yet make direct trade-offs in the same simulation between data and clock for any clocking architecture



Question #3

DDR5:

Is single-ended DDR5 a square peg in a round differential AMI hole?

Is AMI responding quick enough to succeed as an analysis solution?

What do we need to know about implementing DDR5 in our systems?

rw 3 5:20

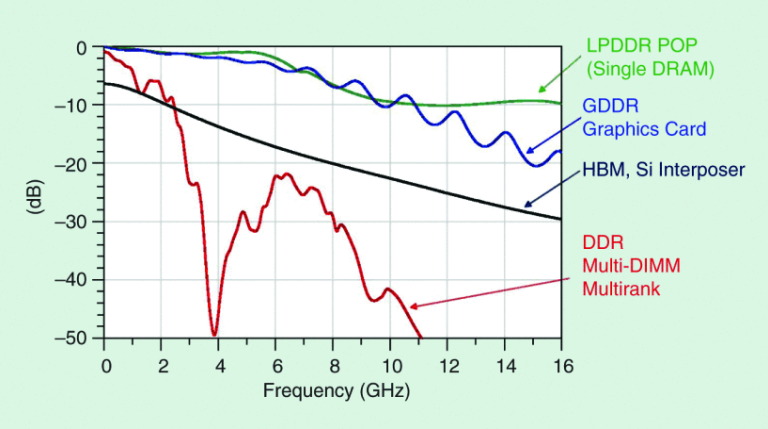
DDR5 Progress

- IBIS 7.1 improves IBIS-AMI support for DDR5
  - AMI Reserved Parameter DC_Offset for inherent signal DC bias
  - C_comp Model for analog model improvement
  - GetWave Clock input for forwarded clocking (DQS)
  - AMI Reserved Parameters Component_Name and Signal_Name for DQ-level buffer model tuning
  - Backchannel Statistical Training
- EDA Tools
  - Capturing system non-linearities for Init and/or GetWave functions
  - DDR5-specific EDA tool support for IBIS-AMI model setup, bus analysis, sweeps, and validation

DDR5 Design Challenges

- EDA tool implementation of all IBIS 7.1 features
- Clocked AMI models
  - Clocked AMI models in development
  - Simulation methodology in development
  - Do we need to implement backchannel training to emulate real system equalization training algorithms?
- DDR5 System Design
  - It's not SerDes! No channel specification to tell you if the Tx/Rx EQ can fix everything
  - Requires co-optimizing channel with limited DRAM EQ capabilities

DRAM Channel Insertion Loss



https://ieeexplore.ieee.org/document/8741253

Q3: AMI and DDR5

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- **Is single-ended DDR5 a square peg in a round differential AMI hole?**
  - **Seems like it at first glance**
  - **But does not have to be that way**
  - **Maybe the side view of that peg is not that square after all**
  - **Non-linear filtering might be required**
  - **Statistical analysis limitations must be respected**

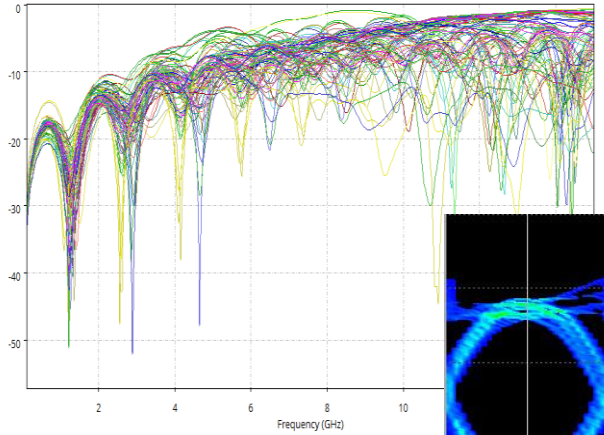
- **Is AMI responding quick enough to succeed as an analysis solution?**
  - **Another example where AMI needs to reflect architectural trends**
  - **Other signaling schemes are possible…**

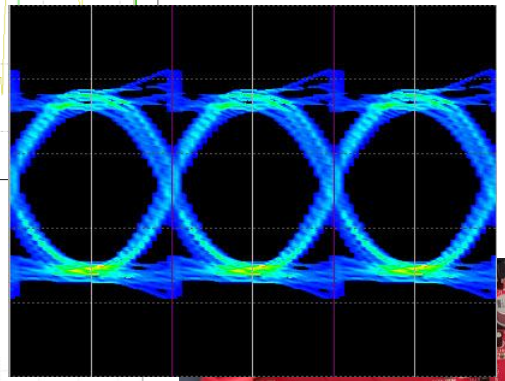
*Melissa & Doug Shape Sorting Cube

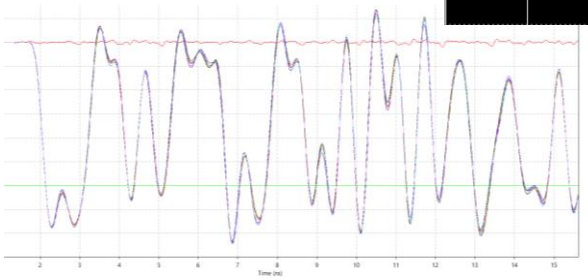
P.S.: The kid needs to be either smart or strong to put the pieces into the box

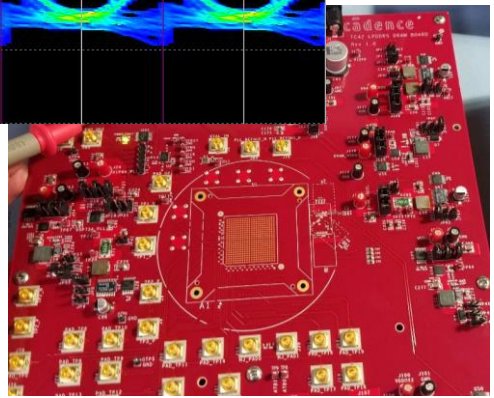
Question 3: DDR5

- **Have to account for rise / fall asymmetry**
- **SSN can be significant**
  - Robust extraction becomes key enabler
- **But AMI can work on waveforms, shouldn't matter if differential or single-ended**
- **Curve ball is external clock / strobe signal**
  - Requires tool functionality to handle that
- **Need to post-process those waveforms like the devices do**
  - Or make simplifying assumptions









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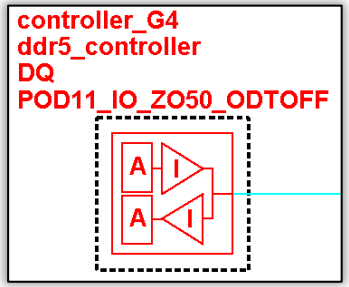
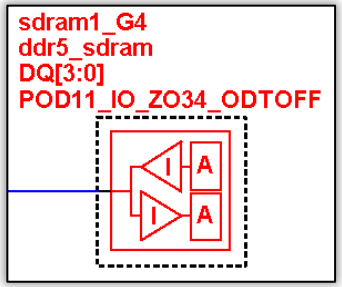
Responses from Michael Mirmak

- **DDR5 IBIS-AMI models do exist!**
  - … and they work!
- **The specification added support slowly and incompletely, but…**
  - New features indeed enable single-ended operation
  - Clocking still needs work but is being defined
- **The biggest unseen feature is shared with SerDes…**
  - Where are the backchannel equalization models?
  - Have any interface standards organizations produced some examples?

DDR5 and GDDR7 (PAM 4)

- Is AMI responding quickly enough to succeed as an analysis solution?
  - Generic DDR5 AMI models exist



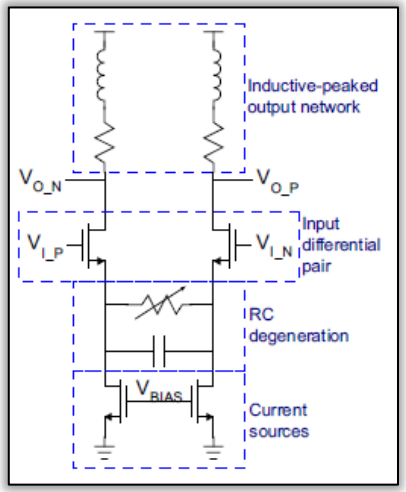


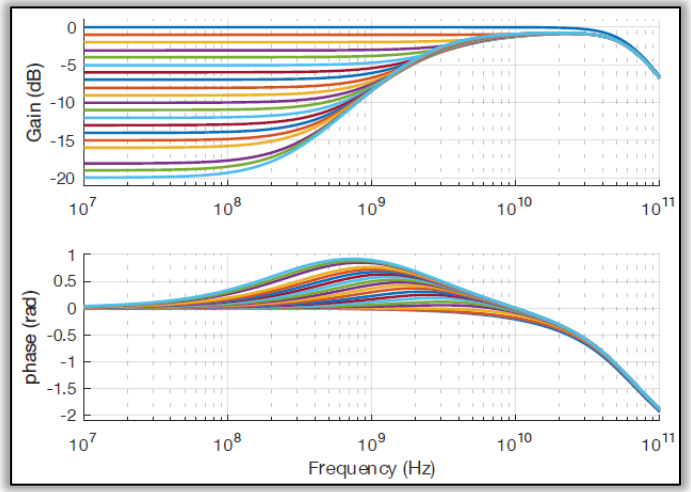
- Are single-ended I/O a square peg in a round differential AMI hole?
  - DDR5 receivers and DC Offset
  - Nonlinearity of single-ended drivers vs. LTI channels for AMI models

MathWorks

DDR5 and GDDR7 (PAM 4)

- How are we practically implementing DDR5 in our systems?
  - Equalization and the clock forwarding
  - Develop training algorithms for:v
    - Optimize FFE, CTLE, DFE, and On-Die Termination (ODT) settings
    - Genetic search algorithms are being evaluated to run parallel analog channel simulation to search the ODT space and IBIS-AMI simulations to search the AMI equalization space





Figures: Halupka, D. *et al*, "Validation Shift-left: Enabling Early SerDes Mixed-signal Validation," *DesignCon 2022, Tech. Proc.* April 2022

Question #4

Is AMI swimming upstream?

The idea of one ubiquitous AMI model for standards, architecture, design, implementation, verification and industry hand-off makes sense, but is it happening?

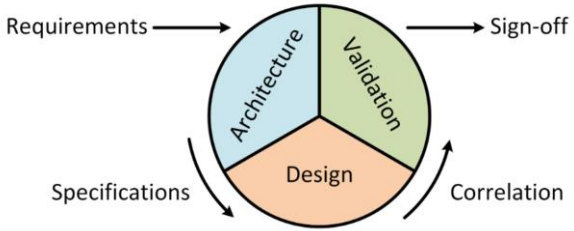
Success stories? …what are the issues and solutions here?

at 2 5:35

Q4: Is AMI Swimming Upstream?

SERIALINK SYSTEMS

- **The idea of one ubiquitous AMI model for standards, architecture, design, implementation, verification and industry hand-off makes sense, but is it happening?**
  - **AMI models? Not really**
  - **Unified SerDes system models? Definitely**



- **Success stories?**
  - **We successfully developed parametric models for ADC-based and analog-centric SerDes architectures**
  - **Our models have been correlated to 112 Gb/s SerDes**
  - **We extended support to SerDes with MLSE**
  - **These parametric SerDes models are then exported to AMI format as the customer-facing collateral**
- **What are the issues and solutions here?**
  - **Analog-centric architectural assumptions embedded to AMI interface**
  - **High modeling overhead and limited observability in AMI**
  - **AMI as auto-generated external view of more generic system models seems to be the right approach**

Q4: Is AMI Swimming Upstream?

- The concept of an eye diagram is central to IBIS standard, AMI modeling, and SI analysis
- But that concept is inherited from conventional analog-centric SerDes architectures
- Things are a bit more challenging when it comes to ADC-based SerDes

Q4: Is AMI Swimming Upstream?

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- **Things are a bit more challenging when it comes to ADC-based SerDes**

Do not try and bend the spoon — that's impossible

Instead, only try to realize the truth

There is no spoon

– The Matrix

Q4: Is AMI Swimming Upstream?

- **The concept of an eye diagram is central to IBIS standard, AMI modeling, and SI analysis**
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Do not try and bend the spoon — that's impossible
Instead, only try to realize the truth
There is no spoon

– The Matrix

Do not try and plot the eye — that's impossible
Instead, only try to realize the truth
There is no eye, it's only the SNR

– SeriaLink Systems

Question 4: Swimming Upstream?

- **No, not swimming upstream. And starting to see a shift in the current.**
- **AMI modeling used to be a necessary evil after IP design is done**
- **Now seeing some users building AMI models pre-design to include in feasibility / trade-offs at system-level**
  - Missing opportunity by not doing more of this
  - Figuring out EQ specs needed to run specific types of channels at a desired BER

Everybody wants to move "up and to the left"

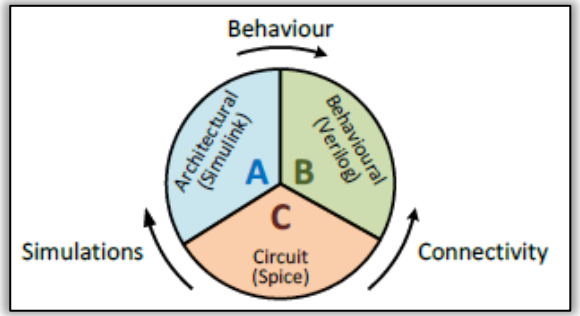
cadence

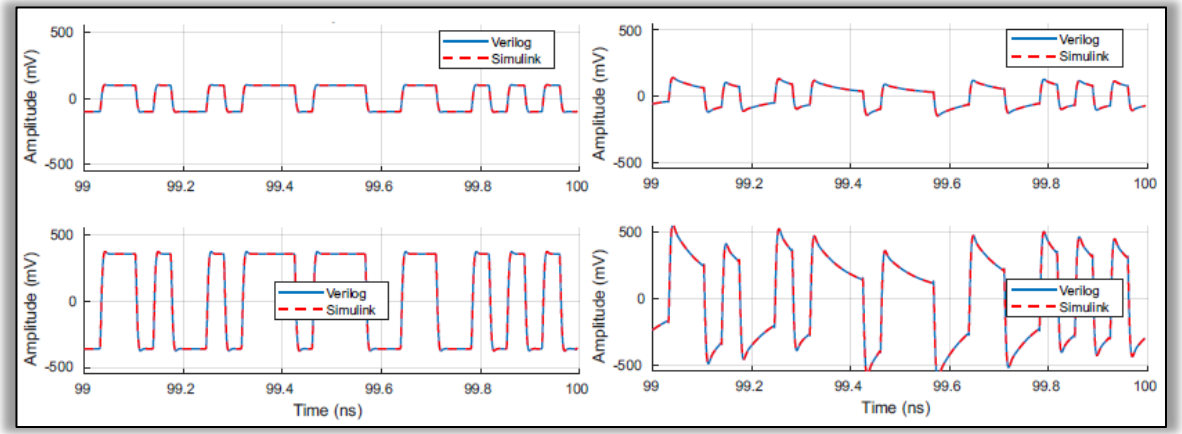
Responses from Michael Mirmak

- **Where IBIS works**
  - Exploring interface interoperability and platform design involving specific devices
  - Solution space examination and limit finding (assuming dual-models)
- **Inappropriate uses**
  - Architectural development (also true of traditional IBIS)
- **“Jury’s still out”**
  - High-volume manufacturing coverage – statistical data is outside the IBIS format today
  - Operation above the PHY layer

Is AMI swimming upstream?

- The idea of one ubiquitous AMI model for standards, architecture, design, implementation, verification, and industry hand-off makes sense, but is it happening? Success stories? What are the issues and solutions here?
  - IBIS-AMI models have been behavioral
  - Modeling is shift left

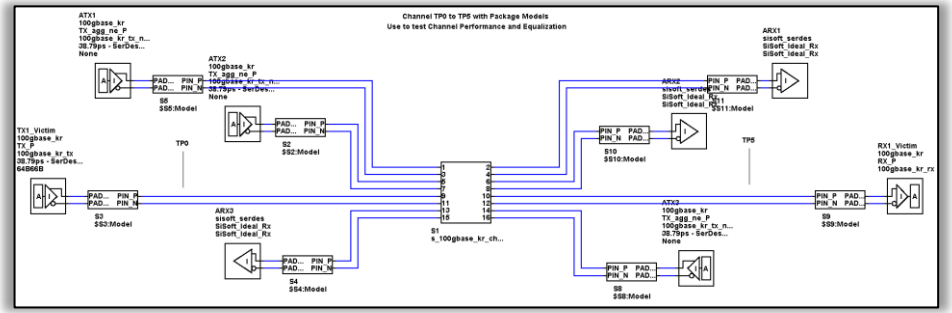


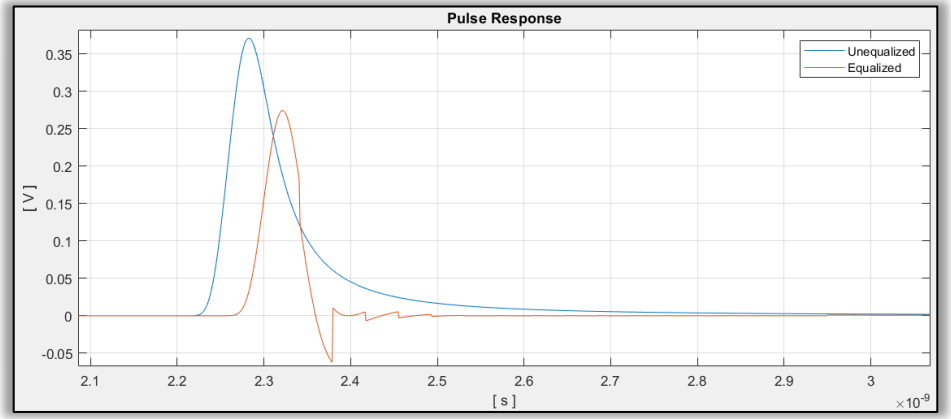


Figures: Halupka, D. *et al*, "Validation Shift-left: Enabling Early SerDes Mixed-signal Validation," *DesignCon 2022, Tech. Proc.* April 2022

COM vs. AMI Modeling

- Similarities
  - Use same channels
  - Both use equalization models
- Differences
  - AMI model describes the details of the actual equalization
  - COM uses generic CTLE and FFE and DFE taps zero out the ISI





AMI Successes

- Micron models
  - IC-vendor approach focuses on device-specific models and realistic silicon variation
  - More DDRx systems designed around specific devices vs. spec-based compliance – LPDDR vs. DDR vs. GDDR tradeoffs
  - IBIS-AMI successfully enables this approach
- Successes
  - Micron DDR5 DIMMs, designed with IBIS-AMI models, validated and working in real systems
  - Micron LPDDR5 components designed into many mobile products with the use of IBIS-AMI models – close collaboration with chipset vendors

AUDIENCE QUESTIONS

DESIGNCON 2022 WHERE THE CHIP MEETS THE BOARD
APRIL 5 – 7, 2022
SI GUYS
#DesignCon
informa markets

Thank you!

Question

AMI Model Correlation

Are AMI models correlated to silicon?
What's the right way to do that? Is it done at all?
What happens when this isn't done?
Does physical layout change behavior?

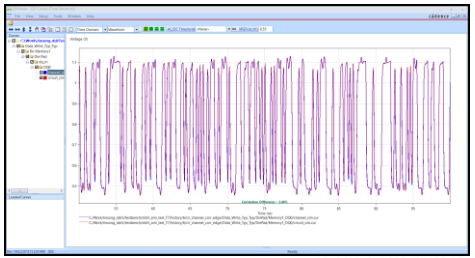
When correlating models to measurement, what constitutes "acceptable"?

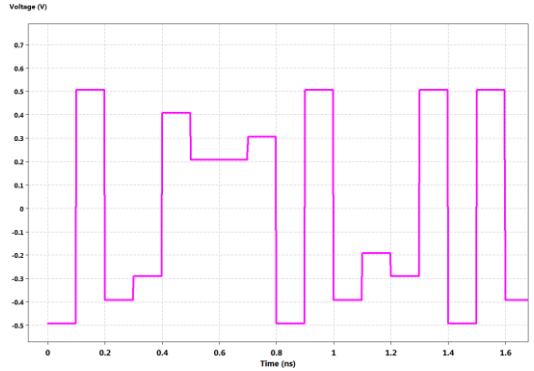
AMI Model Correlation

- Analog model effects
  - (Input capacitance, slew rate, output impedance, etc.)
  - Should be correlated to silicon
  - Micron supportive of this, providing detailed quality reports with correlation to silicon
- Equalization models should be correlated to silicon, where possible
  - Techniques not as straight forward as analog model measurement correlation
  - Limited ability to probe inside Rx equalization circuits
- Acceptable correlation criteria should consider
  - The specification, including Rx mask requirements
  - Model covers the corner variation
  - Model is useful for system designer to make engineering decisions

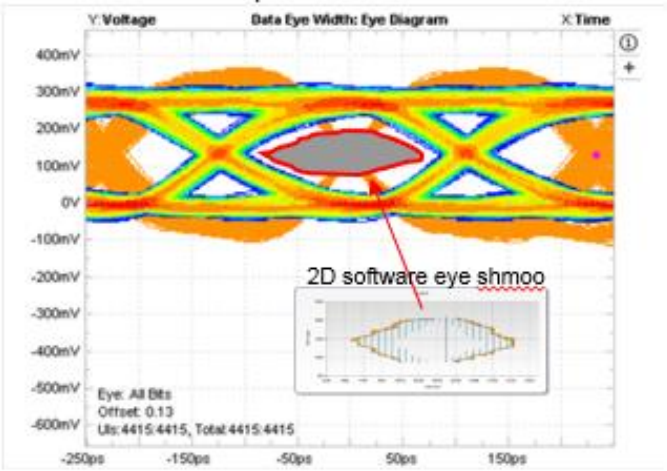
AMI Model Correlation

- Circuit / Channel Sim
  - Verify channel sim faithfully reproduces circuit sim results
- Transmitter
  - Drive into a 50 ohm test load
  - Waveform based correlation vs. transistor-level or measurement results
- Receiver
  - Eye contour or bathtub curves if simulator-based
  - Can compare final adapted coefficient values
  - Eye height and width to compare with measurement
  - Can use embedded eye plotter (if present) in IP from lab measurement
  - Can also utilize IBIS-AMI models in oscilloscope





Scope Measurement



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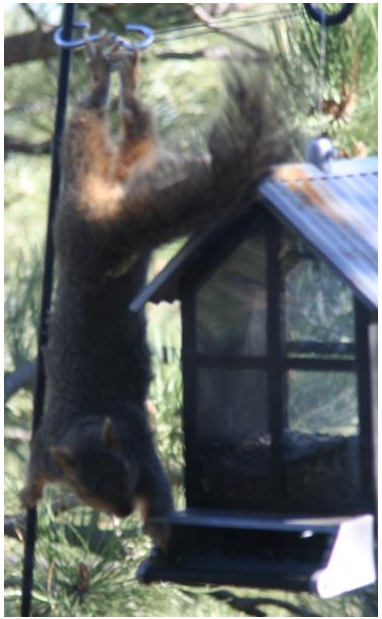
AMI Model Correlation

- Many of our customers require that AMI models are correlated to silicon.
- There are multiple ways to do that
  - Compare models with transistor SPICE simulations
  - Compare models with internal buffer metrics (e.g. Eye Scan)
  - Simulate with stressed eye and compare with lab measurements
- If correlation is not done, end up with failing channels

- Acceptable means the engineer can design a channel using the model that will not fail and have sufficient margin.

MathWorks

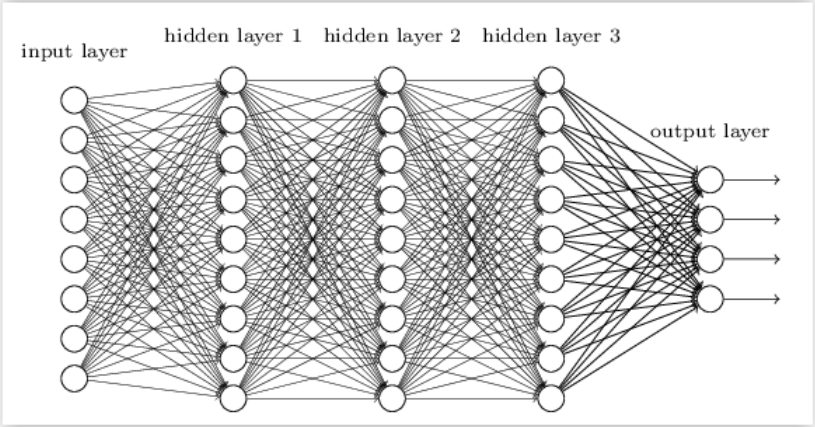
Can Machine Learning and Genetic Adaptation Algorithms be Applied to Training SerDes Channels?



MathWorks

Machine Learning and AMI Modeling

- ML is just a way to “mine” existing data and to enable quick prediction of new combinations of parameters
- No reason why ML models can’t be embedded inside an AMI model’s DLL model
  - Just a “black box”
- AMI could also could be architected to call multiple external MLs
- Expect wider innovation in this area in the next 3-5 years



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