



### 7 Challenging SI / PI Problems That Have NO Existing Solution

Donald Telian, SiGuys Signal Integrity Consultant



Introduction
 7 Problems
 Summary

Seven SI / PI Problems with NO Solution



## **Before We Begin**

- 7 problems, no solution
- Today, sound bites, pointers
- Practical, process, products



Maybe you know of a solution?
Or maybe you are the solution!



## Which Skills Do You Have?

- Math
- Lab work
- Creativity
- People
- Partnering



Miracles





### The Seven Problems, by Skill

#### **Ready for breakthrough**

- 1. Standardization of tem based SerDes AMI models
- 2. Validated analytical surface roughness which have not been appreciated analyticated analyticated
- 3. Adaptation of error correction codes to address the nonrandom behavior of the speed serial link ISI

#### Long-standing problems

4. Automated and orgentic solutions for interfacing SI/PI with Layout an arm are engineers

#### Lots of effort, but needs a fresh approach

- 5. Equalization, incluing speed serial link refer for the serial link refer for the series of the se
- 6. High bandwidth/
- 7. Fast, efficient solution for notified power reference effects of signal performance

### **The Seven Problems**

#### **Ready for breakthrough**

- 1. Standardization of template-based SerDes AMI models
- 2. Validated analytical solutions for conductor loss due to surface roughness / etch lamination
- Adaptation of error correcting codes to address the nonrandom behavior of high speed serial link ISI

#### Long-standing problems

4. Automated and organizational solutions for interfacing SI/PI with Layout and Firmware engineers

#### Lots of effort, but needs a fresh approach

- 5. Equalization, including adaptation, that targets highspeed serial link reflected noise in addition to loss
- 6. High bandwidth/density, low power solution for memory interfacing to replace DDRx
- 7. Fast, efficient solution for modeling non-ideal power reference effects on signal performance



Introduction
 7 Problems
 Summary

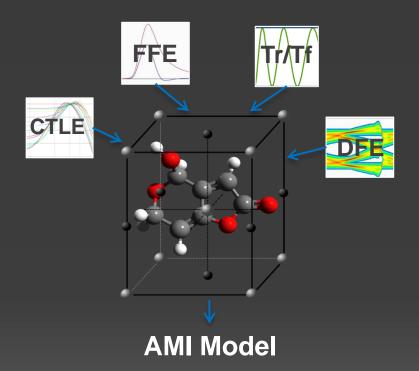
Seven SI / PI Problems with NO Solution





# #1: Standardize AMI Template

- IBIS is a template
  - AMI is not (yet)
- All EDA vendors have
  - proprietary AMI templates
- Need standard syntax
  - Propose with IBIS "BIRD"
- Match on dynamite

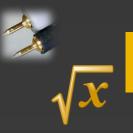


### Resource (DesCon 16):

<u>"Building IBIS-AMI Models from Datasheet Specifications"</u>



# #2: Conductor Roughness



<ul> <li>Dielectric Loss</li> </ul>
<ul> <li>Djordjevic, Sarkar, et. al.</li> </ul>
<ul> <li>Conductor Roughness Loss</li> </ul>
• Who to believe?
<ul> <li>Difficult to get data</li> </ul>
<ul> <li>The physics involved</li> </ul>
<ul> <li>Surface roughness or chemistry?</li> </ul>

Model	Description
Hammerstad	Statistical variation of conduction path length
Huray	"Snowball" model of variation of conduction path length
Koledintseva et. al.	Thin layer of lossy dielectric on surface of conductors.

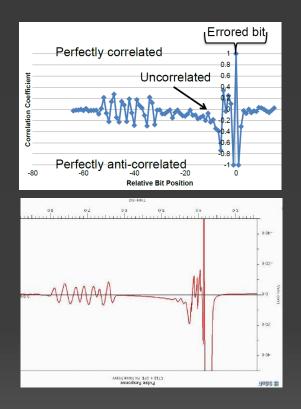
#### Resources (DesCon 16):

- "Effect of conductor profile structure on propagation in transmission lines" Horn, LaFrance, et. al.
- "A Material World" Nwachukwu, Shlepnev, McMorrow



# #3: Adapt FEC for Links

- Existing FEC
  - Pattern independent
- But serial link errors
  - Pattern dependent
- Or, remove bad patterns
  - Self-correcting



#### Resources:

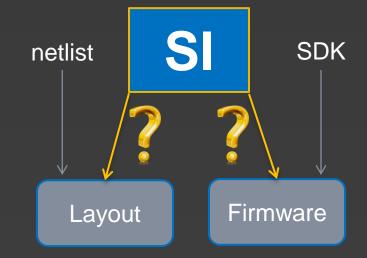
- Michael Steinberger, <u>msteinb@sisoft.com</u>
- "<u>A Brief Tour of FEC</u>", DesignCon '15, Lin, Liu, et. al.





# #4: SI Automation / Hand-offs

- SI / PI Rules
  - Must get implemented
- Optimal equalization
  - Must get implemented
- Little/no automation exists
  - Big source of SI problems

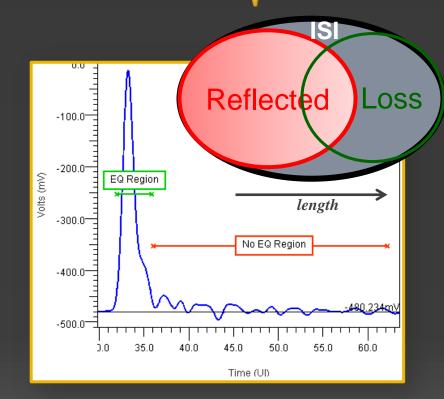


#### Resources:

- EDA-specific files/formats (e.g., Cadence topology files)
- Rules Augmented Interconnect Layout IBIS initiative

## #5: EQ for Reflected ISI

- Existing EQ targets loss
  - Problem on longer links
- Links also fail due to noise
  - Problem on shorter links
- What can be done?
  - Uls 5 to 45, adaptation too



#### • Resources:

- S. Quan, F. Zhong, W. Liu, P. Aziz et al, "A 1.0625-to-14.025Gb/s Multimedia Transceiver with Full-rate Source-Series-Terminated Transmit Driver and Floating Tap Decision Feedback Equalizer in 40nm CMOS", *Digest of Technical Papers, IEEE Intl. Solid States Circuits Conf.*, pp. 348-349, Feb, 2011.
- "Ripple Analysis, Identify and Quantify Reflective Interference..." SPI 2016, Allred, Katz, Furse
- <u>A SerDes Balancing Act: Co-Optimizing Tx and Rx EQ</u> (SiSoft webinar)



## #6: Next-Gen Memory

- Memory standards driven by density
   Not SI / PI
- SI is overly complex and fragile
  - Tolerance is major issue
- When will it end?



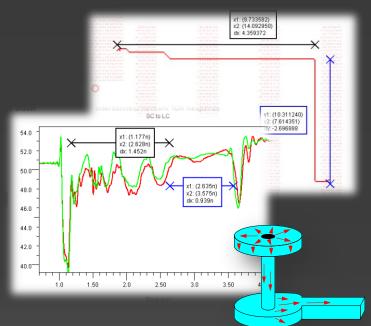
#### • Resources:

- HMC-Hybrid Memory Cube, HBM-High Bandwidth Memory, Wide I/O
- devabpro.sandia.gov



# #7: Non-ideal Reference

- Generalized solutions are slow
  - To configure and solve
- Approximation /= Bad
- Missing metal
  - Raises L, Iowers C
- Simplify?



#### Resources:

- Fast, efficient, and accurate: via models that correlate to 20 GHz
- <your name here>

14



Introduction
 7 Problems
 Summary

Seven SI / PI Problems with NO Solution



© 2016 SiGuys SI Consulting

## Summary

• SI / PI – still plenty of problems to solve

- Some go unresolved
  - Lack of partnership, creativity, ...
- We all are part of the solution

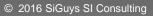






# THANK YOU

PERSONAL PROPERTY AND IN THE PERSON PROPERTY AND INTERPORT AND INT





# **Questions**?

Colores -