IBIS-AMI: New Users, New Uses

Panel Discussion: Wednesday January 31, 2018, 3:45-5pm

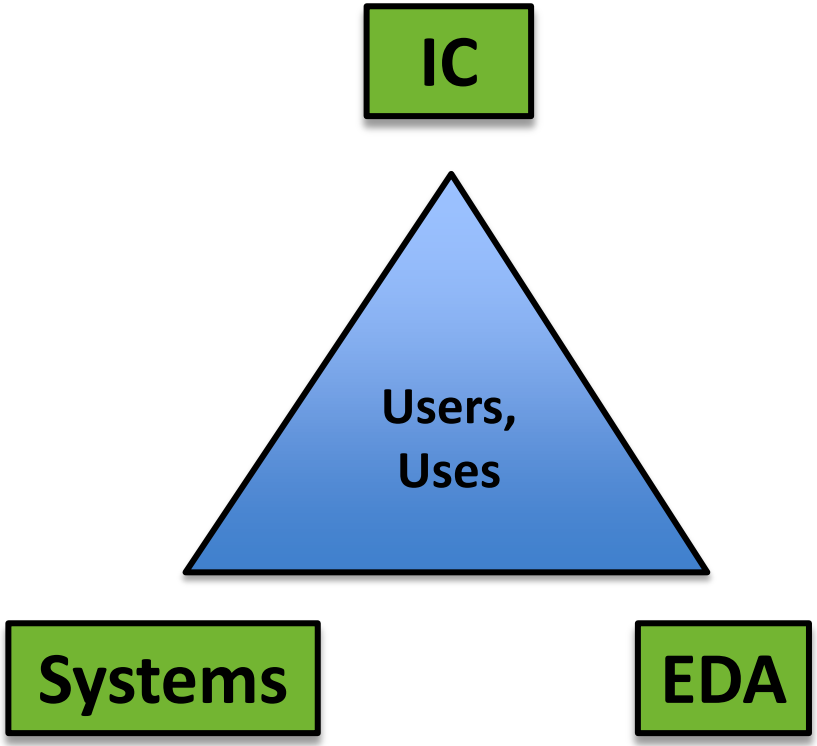
Moderator: Donald Telian, SiGuys

Welcome to the 2018 AMI Panel Discussion

- **IBIS-AMI: New Users, New Uses**
  - Donald Telian, Owner / Signal Integrity Consultant, SiGuys

- **Panel Format:**
  - 5 Panelists
  - 5 questions
  - Timed response
  - Interruptions - flags
  - Audience questions

IBIS-AMI Panel: New Users, New Uses



PANEL:

1.5 IC

1.5 Systems

2 EDA

Panelists

- Todd Westerhoff, SiSoft
- Stephen Scearce, Cisco
- Steven Parker, GlobalFoundries
- Ken Willis, Cadence
- Michael Mirmak, Intel

Introductions

Introduce yourself and your role at your company.

Outline your company's and your personal involvement with AMI models.

1 min - Westerhoff

Todd Westerhoff
VP/Semiconductor Relations
SiSoft

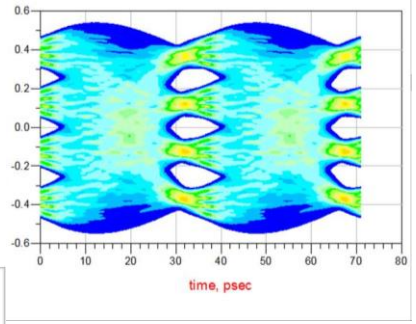
- We provide Quantum Channel Designer (QCD) and Quantum SI (QSI)
- We provide IBIS-AMI model development tools
- We develop IBIS-AMI models for customers
- We validate IBIS-AMI models developed by others
- We perform design work under contract using IBIS-AMI
- We actively drive changes to IBIS and IBIS-AMI

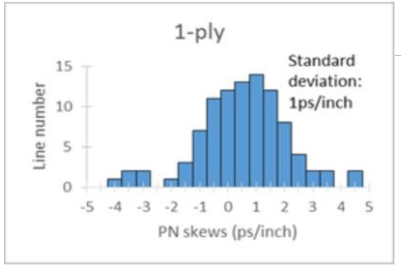
Stephen Scearce

Engineering Manager Cisco

SI/PI/EMC focused for 17 years

- **Pre- Post Route: NRZ- > 56/112G Pam4**
- **System architectural investigation**
- **PCB Material selection**
- **Connector selection**
- **Potential VE Solutions**
- **HW Bringup settings**
- **Glass weave/skew effects**





Steven Parker

Principal Member of Technical Staff, GLOBALFOUNDRIES

Steve Parker is a Principal Member of Technical Staff for GLOBALFOUNDRIES in East Fishkill, New York, USA. He has worked for GLOBALFOUNDRIES since its merger with IBM Microelectronics Division in 2015. Prior to the divestiture he worked at IBM Microelectronics for 19 years across such hardware as Hard Drive Controllers, DDR3/DDR4 memory solutions, and High-Speed Serial Links. He represents the company in the IBIS Open Forum. Currently he develops simulators and models for GLOBALFOUNDRIES' High Speed Serial Link customers. Steve can be reached at: steven.parker@globalfoundries.com

Ken Willis

Product Engineering Architect, Cadence

Ken Willis is a Product Engineering Architect focusing on SI solutions at Cadence Design Systems. He has over 25 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

Overview of Cadence Involvement with IBIS-AMI

- **Introduced the first commercial channel simulator in 2004**
- **Drove definition of the AMI extension to IBIS in 2007**
- **Helped customer develop and correlate the industry's first AMI model**
- **Support Cadence IP division to adopt, develop, and distribute IBIS-AMI models for SerDes IP**

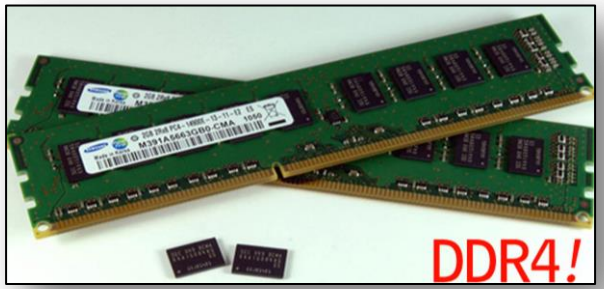
Michael Mirmak

Senior SI Technical Lead, Intel

Michael Mirmak is a Senior Technical Lead for Signal Integrity at Intel, in the Data Center Group's Platform Applications Engineering (DCG PAE), where he supports customer SI modeling and simulation for Data Center platforms. Michael has been involved with IBIS and SI since 1996, developing design guidelines, simulation methodologies, and models for Intel-based platforms. For 11 years between 2003 and 2015, Michael was chair of the IBIS Open Forum, the organization that manages the IBIS, IBIS-ISS and Touchstone standards. He is currently chair of the IBIS Interconnect Task Group and the IBIS Editorial Task Group, which are working on IBIS 7.0 development. He is co-author, with Dave Coleman, of the book "Mastering High Performance Multiprocessor Signaling". He has also written and presented on IBIS in a variety of venues, including the EE Times, the IBIS Summit series and at DesignCon.

AMI: New Users, New Uses

AMI enters DDR4 and DDR5 analyses



Serial Links vs DDR Signals - AMI?

- Differential
- Long and lossy
- Point to point
- Continuous, balanced
- ~Deterministic
- Static impedances

- Single-ended too
- Short and ringy
- Multi-loads, multi-drivers
- Stops, starts, hand-offs
- ISI in many flavors
- Dynamic impedances

Question 1

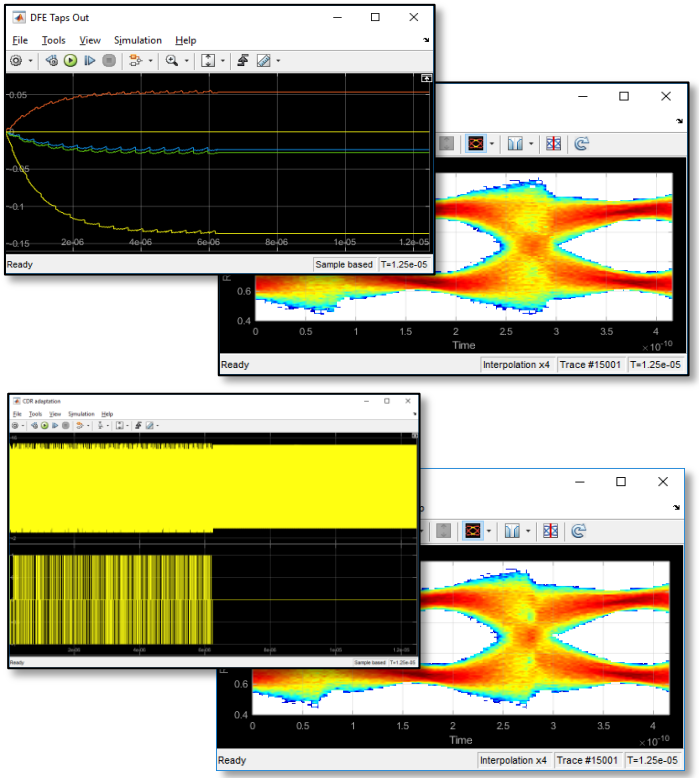
Can AMI models be applied to DDRx analysis?

How will this be done, and what barriers must be solved?

How will DDRx expand the AMI user base?

2 min, Westerhoff, 3:55

DDR5 and AMI

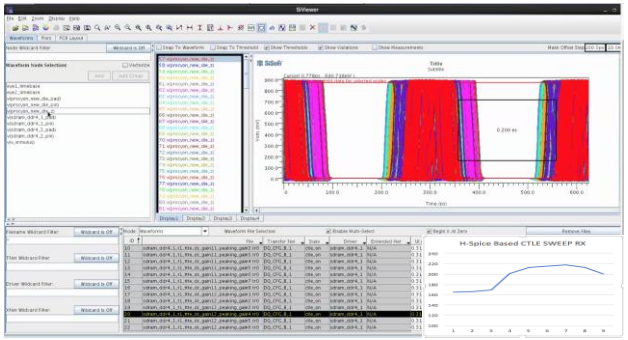


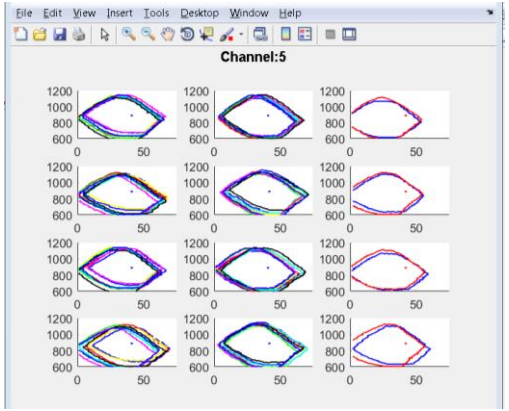
- I/O linearity: AMI assumes it
- Is impulse response enough for single-ended analysis?
- Statistical or Time-Domain?
- DRAM DFE training
- Clock forwarding

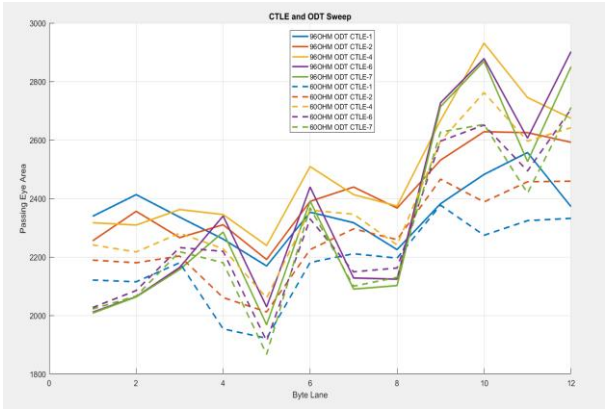
Westerhoff

Can AMI models be applied to DDRx analysis?

- IBIS-AMI Modelling of High-Speed Memory Interfaces, Yan/Rambus 2015, EPEP
  https://ibis.org/summits/jan16/yan.pdf
- Sisoft OSQ - **EDI CON USA 2017,** http://www.sisoft.com/elearning/secure/files/AMI%20DDR%20-%20v5.pdf
- Sigrity SystemSI Parallel Bus Analysis, http://schedule.designcon.com/session/ddr5-modeling-using-automated-ibis-ami-modeling-technology/856180
- Mentor, Fast Eye -> Verilog A - > IBIS Summit Friday
- Keysight DDR-kit with EQ, ~ 2014, but not AMI



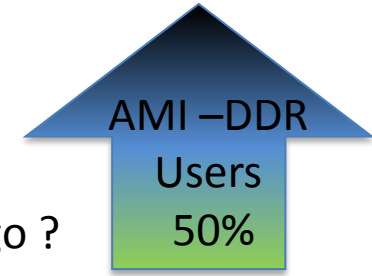




Scearce

What barriers must be solved?

- EDA Vendors - > Creation of New EDA flows/ Tools to facilitate AMI analysis for memory
  - AMI flows that facilitate multi-pair bus interaction
  - Encapsulate channel with ODT Terms, and provide Point to Point work flow for AMI friendly environment.
- Memory Controller Vendors and Memory Suppliers to invest in creating models
  - Spice available now, 100-1000x Slower for optimization, (Cadence, Sisoft Micron, …?)
- Topology/technology barriers
  - Stubs, Multi Ports/drop , Low Loss channels Long transient response,
  - Rise/Fall mismatch could require multiple impulse response characterization
- Single ended is AMI suited to tackle Source Sync interfaces
- Statistical analysis for Source Sync interfaces, where did the clock PDF go ?
- Acceptance of AMI for parallel simulations
- Address Power/SSO as part of the DDRx AMI flow, or a secondary flow



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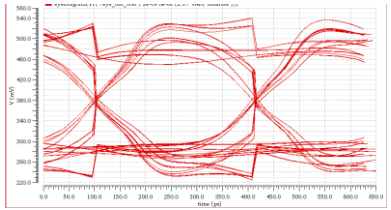
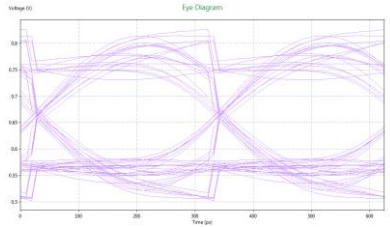
Can AMI models be applied to DDRx analysis?

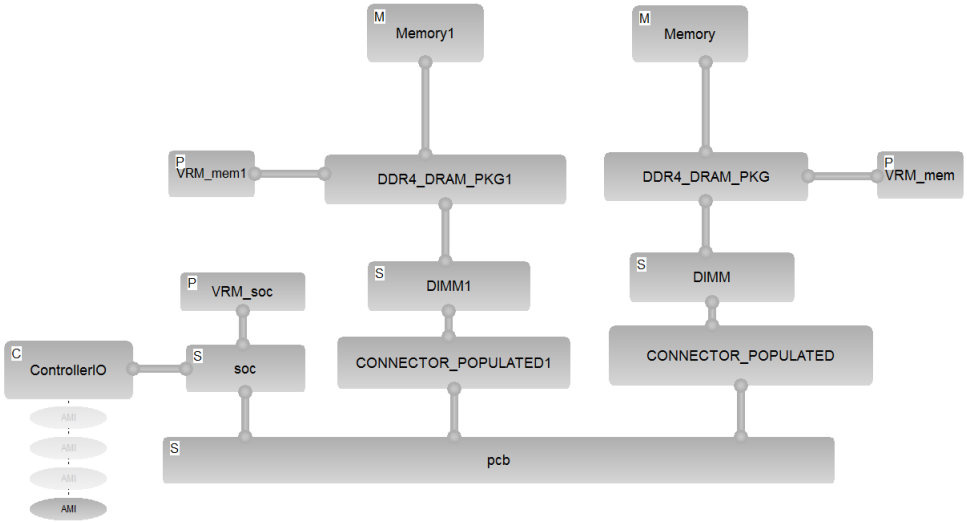
- **Delivered industry's first DDR4 IBIS-AMI model to customer mid-2017 for Cadence DDR4 IP**
- **Correlated to transistor-level simulations**
- **Currently used in live project**

transistor



IBIS-AMI





Willis

Question 1

Can AMI models be applied to DDRx analysis?

How will this be done, and what barriers must be solved?

How will DDRx expand the AMI user base?

Question 2

What about measurement tools?

When AMI was introduced we realized scopes could also load AMI models to display an equalized eye.

Has this happened?
If not, why not and what can we do help this happen?

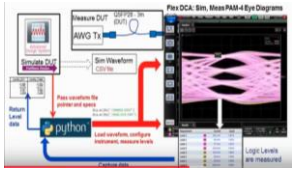
2 min – Scearce, 4:05

Scope Based AMI?

- **Tektronix ->** 2014 DesignCon2014_Correlation of measurement and simulation results using IBIS- AMI models on measurement instruments, Sarah Boen
- SDLA Visualizer, (**AMI),**
  - https://www.tek.com/datasheet/option-sdla64-dpofl-sdla64-real-time-and-jnb02-sampling

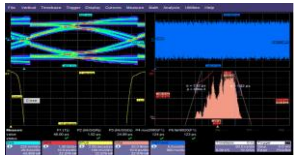
- Keysight, SCPI/pyvisa Matt Ozalas, Potential in Future products
  - Entry of FFE and DFE coefficients, Clock recovery, CTLE…

KEYSIGHT TECHNOLOGIES



- Teledyne LeCroy. , Potential in Future, RX capability to mimic RX Eq (**Eye Doctor)**
  - Entry of FFE and DFE coefficients, Clock recovery, CTLE**…**

TELEDYNE LECROY Everywhereyoulook™



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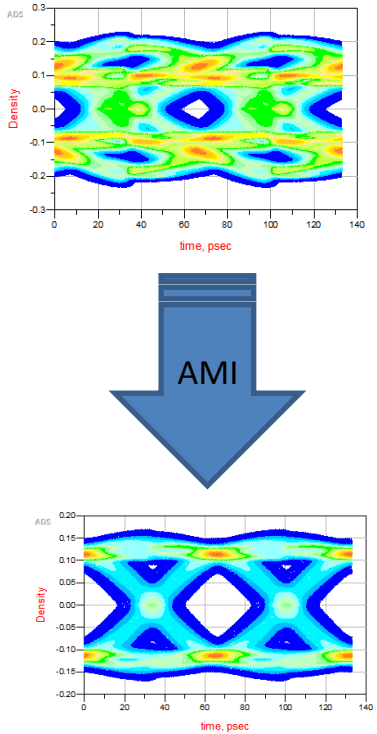
Benefits of AMI/Measurement Integration

- Improved correlation to system modeling Serdes/DDRx
- Scope based RX Equalization -> based on actual Silicon behavior
- Channel compensation & Receiver Equalization in 1 step.
- Adaptive EQ updates based on the receiver
- Real time feedback on RX metrics



Scearce

Question 2

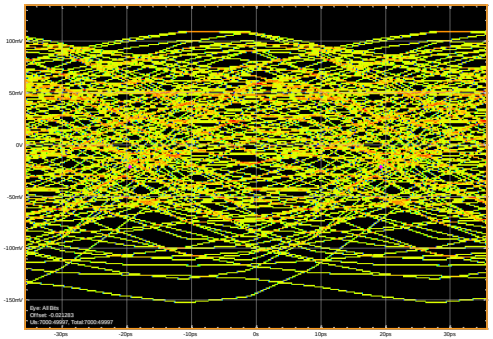
What about measurement tools?

When AMI was introduced we realized scopes could also load AMI models to display an equalized eye.

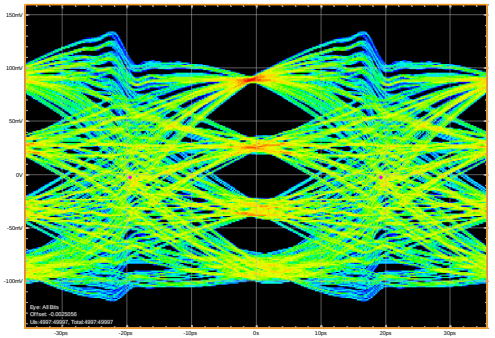
Has this happened?
If not, why not and what can we do help this happen?

How do AMI models relate to measurement tools?

- **Can use same AMI models in simulation and in the oscilloscope**
- **Post-processes raw waveforms in scope to “virtually” probe inside the chip, post-equalization**
- **Co-presented with Tektronix at DesignCon 2016 for PAM4 case**



Before RX



RX equalized

Willis

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Has this happened?
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Measurement Equipment and AMI

- **AMI Rx models return an equalized waveform and clock “ticks” to the simulator**
- **AMI does not specify how the simulator should post-process and display this information**
  - Eye diagrams, eye contours, BER estimates
  - Extrapolation
- **This was a conscious decision – to allow EDA vendors to add value through custom post-processing**
  - Revisiting this decision could help improve model portability and increase use of AMI models in other markets

Question 3

Serial Links.

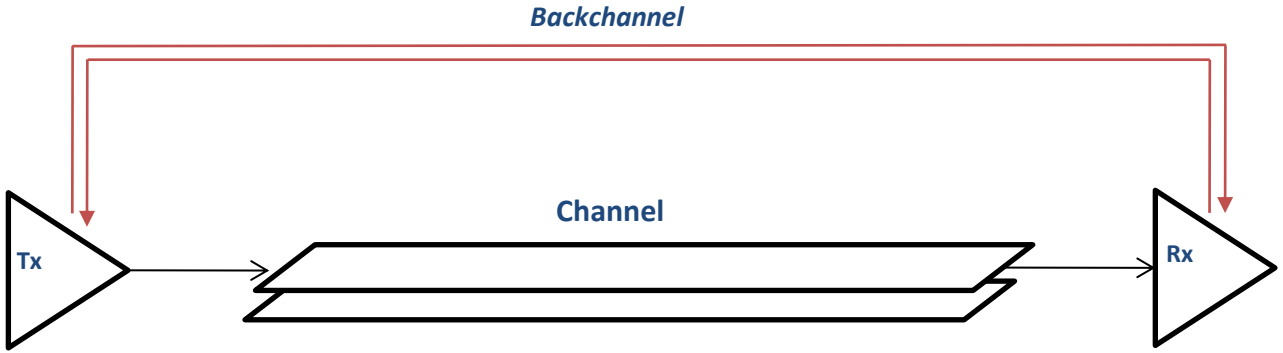
What are the new features there, and how they are impacting AMI?

2 min – Parker, 4:15

What are the new features related to serial links?

Backchannel Support

- Ability for a SerDes receiver in a serial link to automatically tune the equalization settings of its SerDes transmitter
- Automates simultaneous co-adaptation and co-optimization of both transmitter and receiver equalization (emulating how real hardware behaves)



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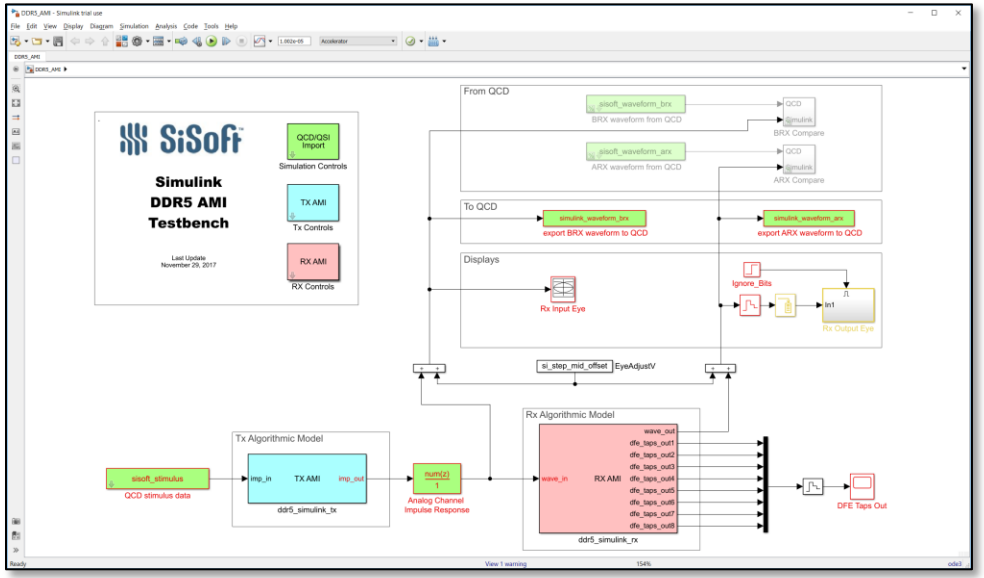
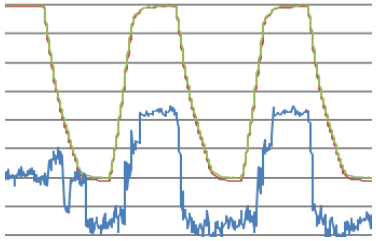
New Features in AMI for Serial Links

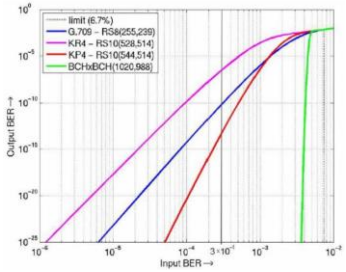


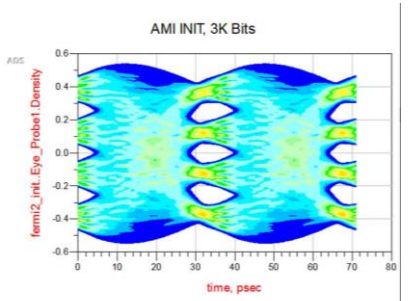
- PAM4 adoption continues
- AMI backchannel modeling BIRD
- Simplifying AMI model generation

Serial links, New Features/AMI



- Dynamic adaptation, Temperature ramp, RX EQ, CTLE
- Precoding, Error Tracking, Error correlation , FEC Encoding
- FEC Modeling and pre VS Post FEC BER
- FEC performance WRT error signatures, Error Tracking, Error correlation, Encoding,
- Random/Burst/Mixed error handling
- Re-timers with FEC capability





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Question 4

There are many papers on 56 and 112 Gbps this year.

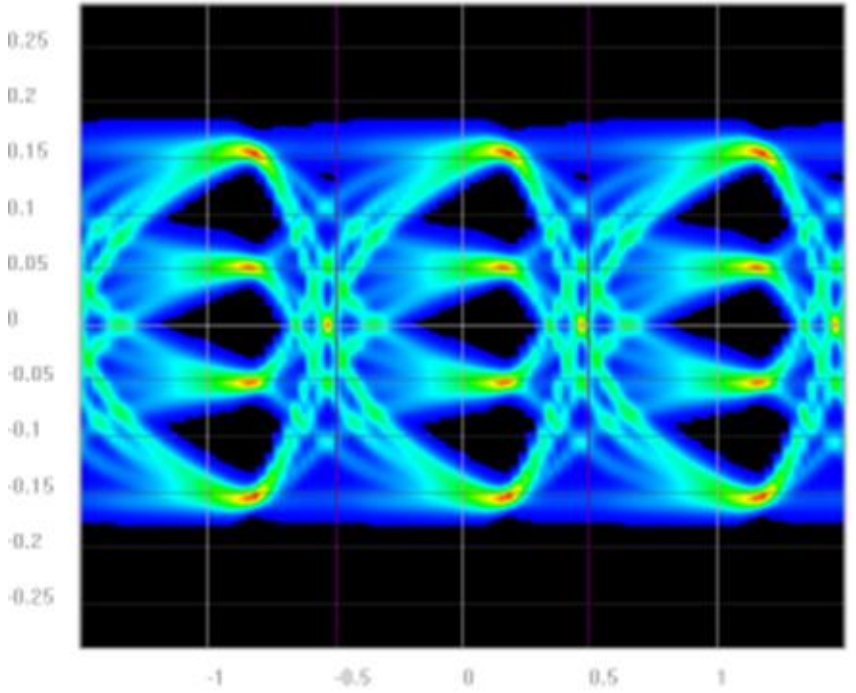
What has changed in AMI for these data rates?

How has AMI helped us get to these speeds?

2 min, Willis, 4:25

What has changed in AMI for 56/112 Gbps?

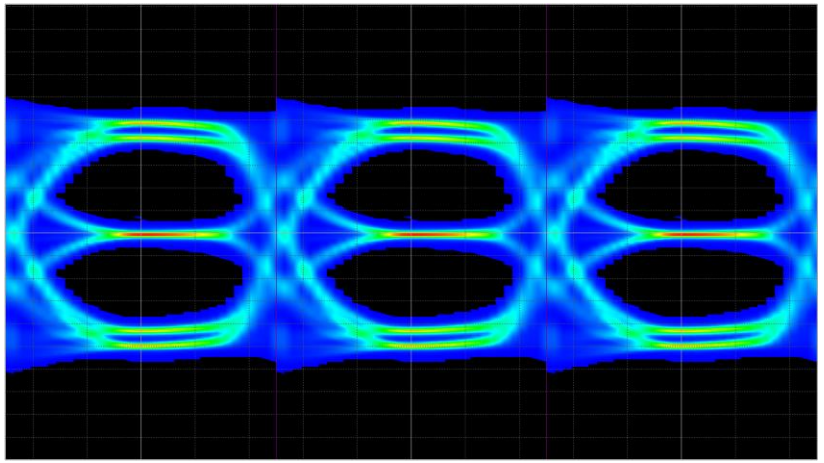
- No changes needed for spec
- Had to figure out how to make Rx equalization multi-level aware

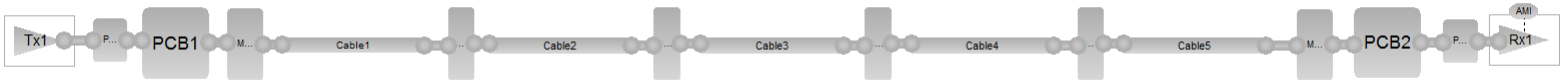


Willis

Another new user – automotive Ethernet

- **100BASE-T1 mainstream use today**
- **1000BASE-T1 has significant activity**





Willis

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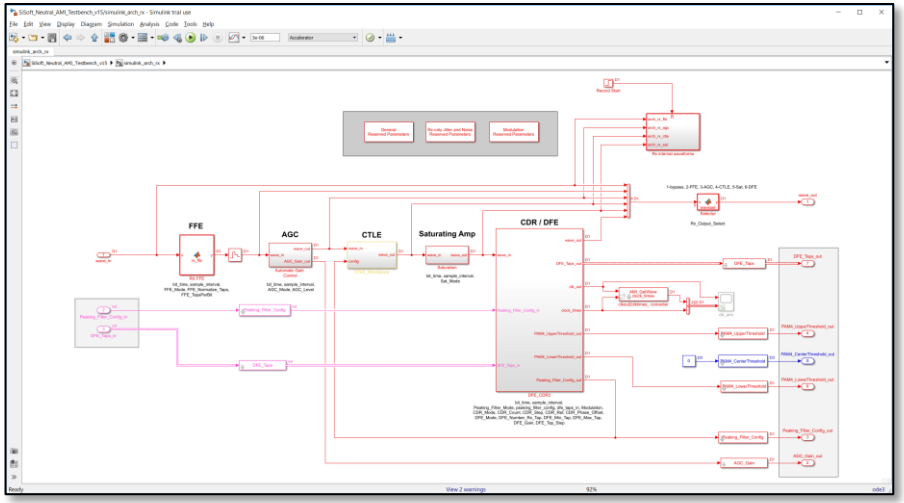
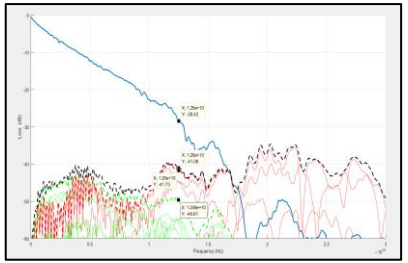
56G/112G and AMI

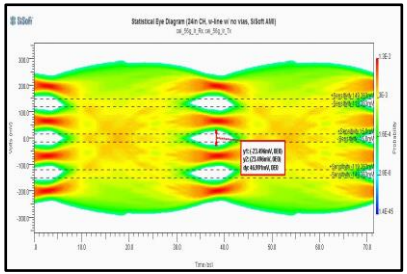


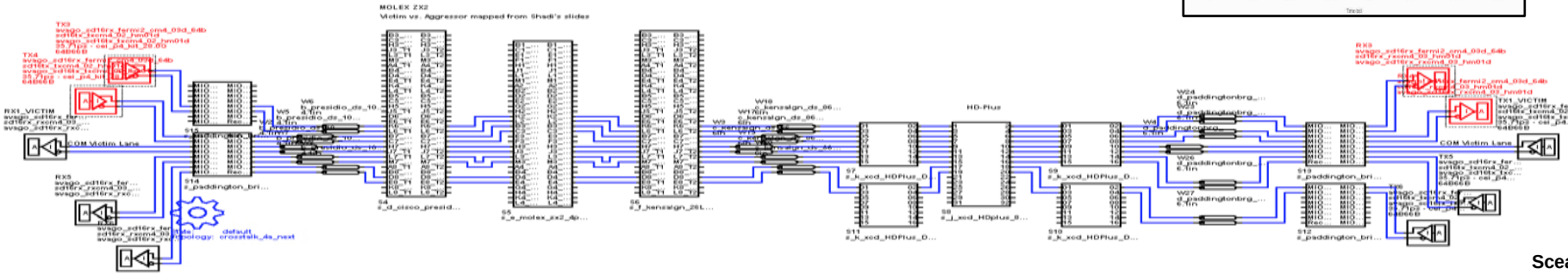
- **Exploring ADC/DSP architectures**
- **AMI models allow**
  - Fast access to customer channels
  - Exploration using commercial EDA tools

How has AMI helped us get to these speeds

- Acceptance
- System Design Feasibility
- Component/Material selection
- Comprehensive channel budgeting







Scearce

Question 4

There are many papers on 56 and 112 Gbps this year.

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Question 5

What else do you want to tell the audience that will help them better understand and apply AMI models and analysis in new ways?

2 min, Mirmak, 4:35

“All Models are Wrong…”

George Box

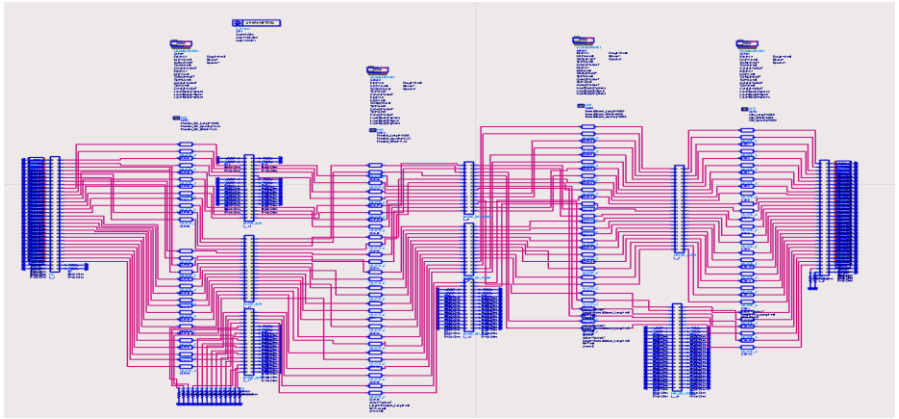
Born	18 October 1919 Gravesend, Kent, England
Died	28 March 2013 (aged 93) Madison, Wisconsin
Residence	United Kingdom, United States
Alma mater	University College London

- **“All models are wrong, but some are useful”**
- **Know the analytical methods you’re using and the assumptions they’re based on**
- **Validate your models before using them**
- **Understand the limits of the models you’re using (as best you can)**
- **Start simple and add complexity incrementally**

Westerhoff

AMI Understanding

- Leverage simple simulations to build intuition
- Focus on lab results and correlation to simulation
- Leverage generic technology models
- Strive to understand how far AMI can take you
- Engineering common sense



Scearce

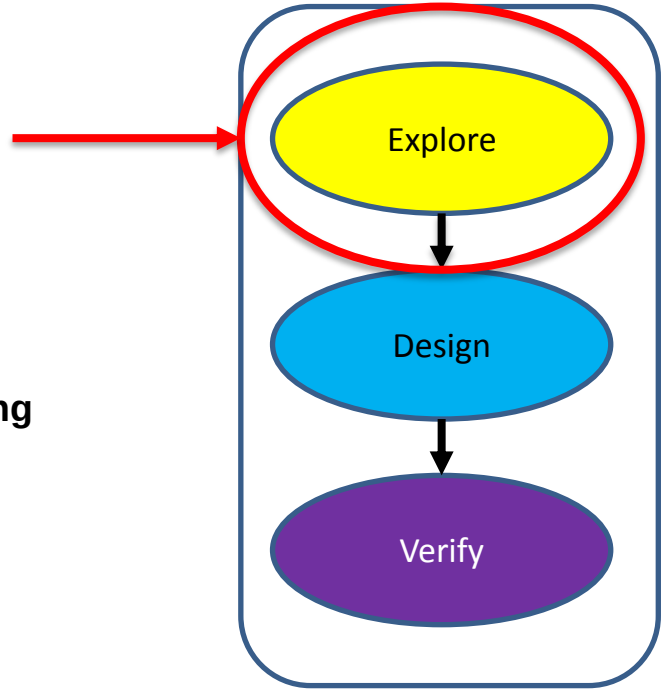
Question 5

What else do you want to tell the audience that will help them better understand and apply AMI models and analysis in new ways?

Parker

What else do you want to say about AMI?

- **AMI model usage is moving upstream into the IP exploration stage**
- **AMI is convenient to quickly experiment with different types of equalization and all their interactions, and explore the limits, *pre-silicon***
- **Want to understand that solution space before investing in detailed IP implementation**



Willis

AUDIENCE QUESTIONS

Question

Engineers need a clear process/metric to judge AMI analysis results (internal Rx eye after equalization).

What should that be?

Is 0mV/0pS eye at 1e-?? BER a reasonable target?
Should we just use COM?

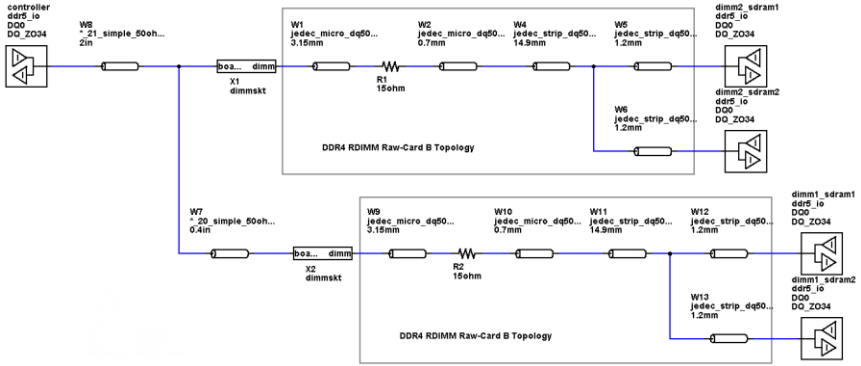
Question

Are there differences between the AMI spec and the actual models?

What is “portability” meant to achieve?

Thank you!

AMI for DDRx Drivers, Termination & Equalization?



- I/O driver strength & receiver termination settings were complicated already
- How do we trade-off termination and equalization settings?

```
Each transaction:
     (Driver) * (Receiver) * (Terminator)**3
     = 3 * 8 * 8**3
     = 12,288 combinations per transaction
* 4 transactions
     = 49,152 total possible termination settings (!)
```