DesignCon® 2019
WHERE THE CHIP MEETS THE BOARD

Which Model When? Succeeding with IBIS-AMI

Panel Discussion: Thursday January 31 2019, 3:45-5pm

Moderator: Donald Telian, SiGuys

This session was presented as part of the
DesignCon 2019 Conference and Expo
For more information on the event, please go to DesignCon.com

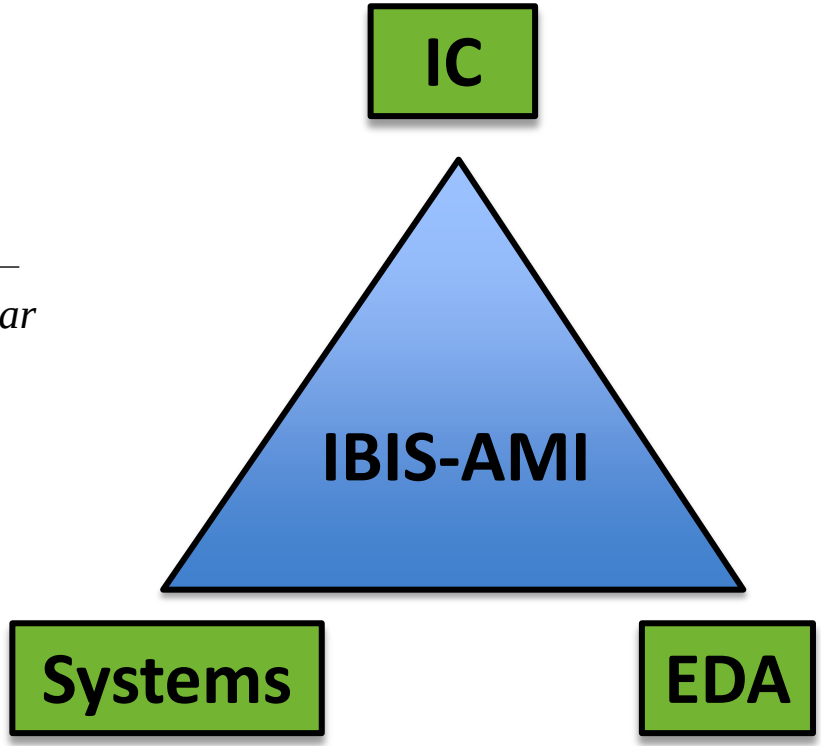
Welcome to the 2019 AMI Panel Discussion

- **Moderator:**
  - Donald Telian, Signal Integrity Consultant / Owner, SiGuys

- **Panel Format:**
  - 4 Panelists
  - 4 questions
  - Timed response
  - Interruptions - flags
  - Audience questions

Which Model When? Succeeding with IBIS-AMI

Yearly AMI Panel – this is our 5th year



Cooperation

Collaboration

Panelists

- Michael Mirmak, Intel
- Walter Katz, MathWorks
- Justin Butterfield, Micron
- Ken Willis, Cadence

Introductions

Introduce yourself and your role at your company.

Outline your company's and your personal involvement with AMI models.

1 min - mm

Michael Mirmak

Senior SI Technical Lead, Intel

Michael Mirmak is a Senior Technical Lead for Signal Integrity at Intel, in the Data Center Group's Platform Applications Engineering (DCG PAE), where he supports customer SI modeling and simulation for Data Center platforms. Michael has been involved with IBIS and SI since 1996, developing design guidelines, simulation methodologies, and models for Intel-based platforms. For 11 years between 2003 and 2015, Michael was chair of the IBIS Open Forum, the organization that manages the IBIS, IBIS-ISS and Touchstone standards. He is currently chair of the IBIS Interconnect Task Group and the IBIS Editorial Task Group, which are working on IBIS 7.0 development. He is co-author, with Dave Coleman, of the book "Mastering High Performance Multiprocessor Signaling".

Walter Katz

Chief Scientist, MathWorks

Dr. Walter Katz, Chief Scientist for MathWorks, is a pioneer in the development of constraint driven printed circuit board routers. He developed SciCards, the first commercially successful auto-router. Dr. Katz founded Layout Concepts and sold routers through Cadence, Zuken, Daisix, Intergraph and Accel. More than 20,000 copies of his tools have been used worldwide. Dr. Katz developed the first signal integrity tools for a 17 MHz 32-bit minicomputer in the seventies. In 1991, IBM used his software to design a 1 GHz computer. Dr. Katz is active in the IBIS Open Forum, is one of the original developers of the IBIS-AMI Standard, and has focused on developing AMI Modeling software and SerDes channel analysis software. Dr. Katz holds a PhD from the University of Rochester, a BS from Polytechnic Institute of Brooklyn (Tandon School of Engineering, NYU) and has been awarded 5 U.S. Patents.

Walter Katz, The MathWorks (formally SiSoft)

- I was one of the original developers of the IBIS-AMI standard along with Cadence, IBM, Texas Instruments
- I was part of team that developed QCD, an early and leading-edge IBIS-AMI simulator.
- SiSoft has been developing IBIS-AMI models for 10 years.
- Initially, SiSoft IBIS-AMI models were written in “C”.
- For the last 4 years we have been working with MathWorks on a MATLAB/Simulink tool to develop IBIS-AMI Models.
- SiSoft has been acquired by The MathWorks
- We are demonstrating at our booth a third generation MathWorks IBIS-AMI model development tool “SerDes Toolbox” that supports both “Top Down” and “Bottom Up” SerDes Design and IBIS-AMI Modeling.
  - You do not often get the chance to start all over three times with a blank sheet of paper!

Justin Butterfield

Senior Engineer,
Micron

Justin Butterfield, Senior Engineer for Micron Technology on the Silicon Signal Integrity team, has over 11 years of experience developing IBIS and HSPICE models for DRAM and NAND products. Throughout his career, Justin has created buffer models for aiding in the development and adoption of new memory standards, including ONFI 4, LPDDR4, LPDDR5, and DDR5. Justin is currently leading Micron's development efforts with IBIS-AMI models for DDRx interfaces. He received both his BSEE and MEEE degrees from Boise State University.

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Ken Willis

Product Engineering Architect, Cadence

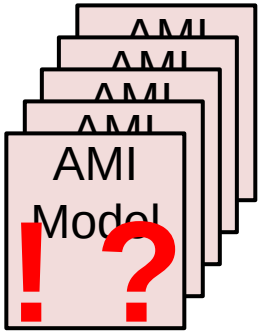
Ken Willis is a Product Engineering Architect focusing on SI solutions at Cadence Design Systems. He has over 25 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

Overview of Cadence Involvement with IBIS-AMI

- Introduced the first commercial channel simulator in 2004
- Co-authored definition of the AMI extension to IBIS in 2007
- Helped customer develop and correlate the industry's first AMI model
- Currently develop and distribute IBIS-AMI models for Cadence SerDes and DDR IP

Which Model When? Succeeding with IBIS-AMI

- **IBIS-AMI Standard entering its 2nd decade**
- **Models more readily available**
- **Various types / formats**
- **DDR5 ?!?!**



AGENDA

- **Panelist Questions**
  - AMI Model Options
  - AMI Model Building
  - AMI Model Features
- **Audience Questions**

Question 1

AMI MODEL OPTIONS:

How often is the vendor's AMI model unavailable?

Template AMI models are now available in all EDA tools. How useful are they? When should I use them? When should I not?

Can I build AMI models from a library of elements? Can I enter CTLE curves and how many taps my DFE has? When is this not advisable?

What happens if and when I need to write a new algorithm?

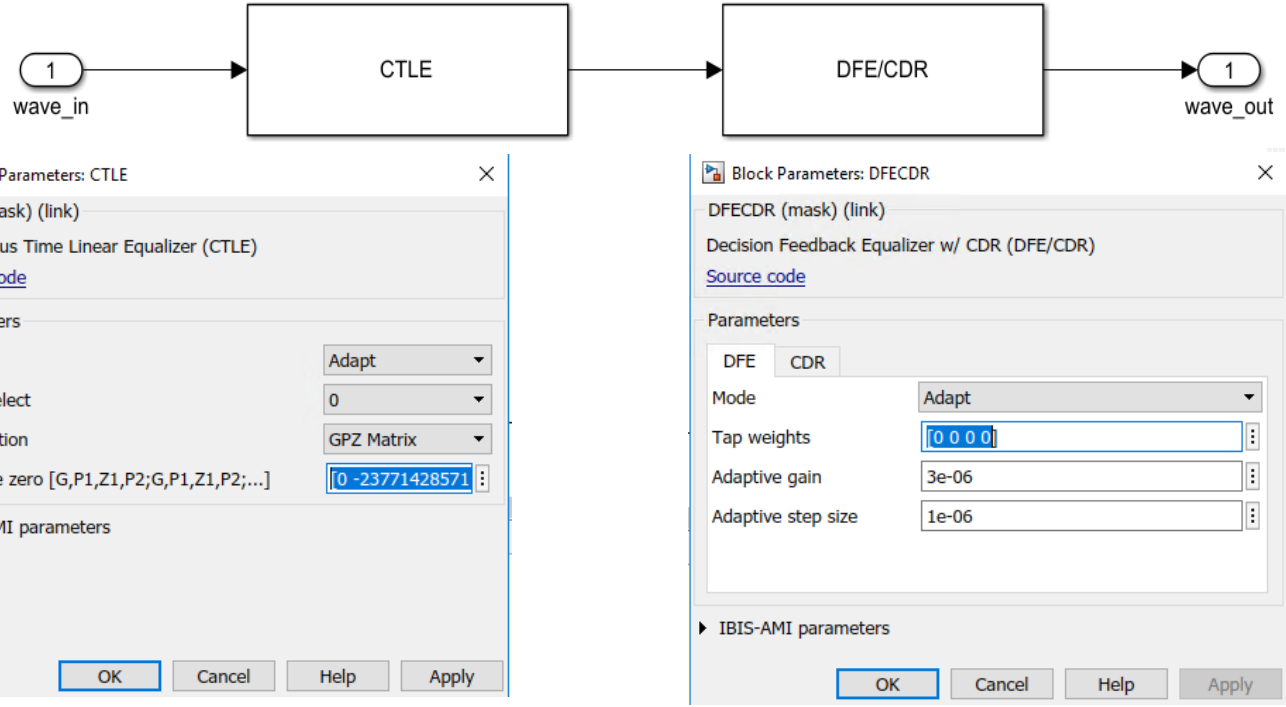
4 min, wk, 3:55

Q2.1: AMI MODEL OPTIONS: How often is the AMI I need unavailable? Template AMI models are now available in all EDA tools. How useful are they? When should I use them? When should I not?

- SiSoft/MathWorks market IBIS-AMI model development tools, IBIS-AMI simulators and consulting services to IC vendors and systems houses developing next generation SerDes designs.
- For our consulting work, AMI models are often not available. We have had to configure our internal Tx and Rx models in accordance to the data sheets available.
- **When margins are tight,** we need to get accurate models for the IC vendor, and often have worked with them using measured data or SPICE simulation data to refine these models.

Q2.2: Can I build AMI models from a library of elements? Can I enter CTLE curves and how many taps my DFE has?

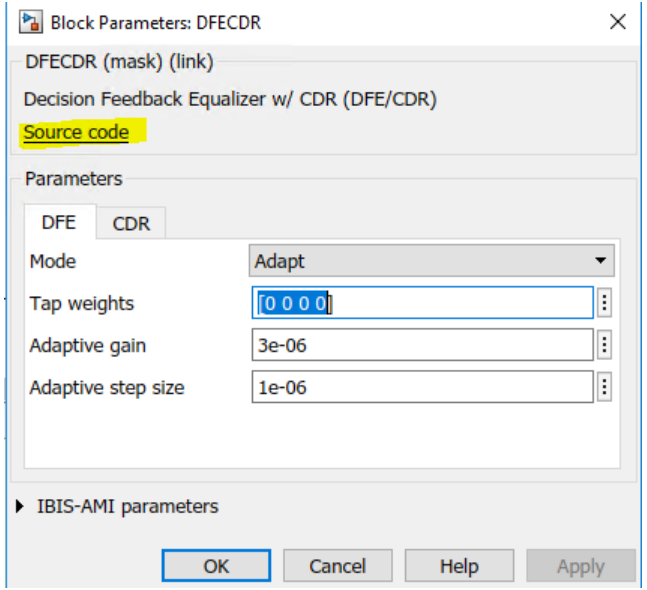
Yes, Yes, Yes.



Q2.3: When is this not advisable? What happens if and when I need to write a new algorithm?

- When you need to enter families of CTLE curves for process corner and temperature.
- When you need to change a DFE adaptation algorithm.
- When you need to create a DSP algorithm.

- Source Code is MATLAB!
- MATLAB is the language that SerDes Designers were using before IBIS-AMI was invented



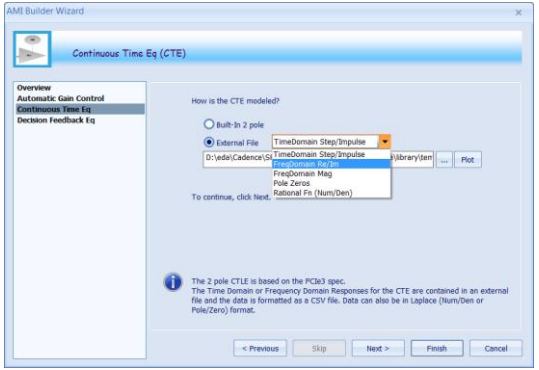
AMI Model Options

- Preface: Our perspective is from the DDR (parallel) bus stand point
- IC Vendors should provide models
  - Micron supports IBIS
  - We plan to support IBIS-AMI in ways that make sense
- Timing of model releases can sometimes be an issue
  - System designers may want to begin work before Silicon has taped-out
  - Template models can be very useful in the early stages
- Need to consider your design's solution space
  - Spec based models may account for all possible specification conditions
    - May be difficult for DDR
    - Some specs may be too wide to be useful

AMI Model Options

- Usefulness of template and spec based models depends on available info
  - Equalization characteristics need to be well defined in the specification
    - DFE number of taps, tap ranges, tap step size
    - Pre/De-Emphasis, FFE
    - Actual CTLE curves may be difficult to obtain
  - Analog characteristics
    - Input capacitance, slew rate, output impedance, etc.
    - May be defined in the specification
    - But, could have a very wide range
- Template models would be based on some assumptions
  - Assumptions need to be understood
  - Can be useful for answering some system design questions
  - Using IC vendor models could allow the system to be tuned for best performance

AMI Model Options



- Availability
  - Often not available for up front feasibility / trade-off analysis
  - Typically available now for design and verification stages
- Template models
  - Particularly useful for standards-based interfaces, use when you need a model for “the other end”
  - Compliance kits with simulation testbenches and spec-level AMI models readily available for common standards
- AMI models easily built from existing building blocks today
  - Need to know a little about the SerDes features, ex. type of EQ, # of taps, etc.
  - Can import data to describe CTLEs in time domain, frequency domain, rational function, pole zero
  - Custom algorithms can be imported in code snippets, but needed less as modeling tools mature

AMI Model Options

Templates and wizards can definitely help ease model creation

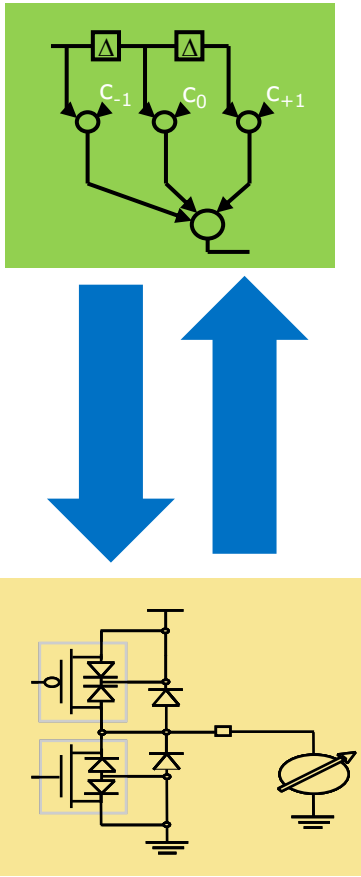
Two critical questions should be asked by users

1) Can statistical models be created?

2) Are models created from architectural designs ("top-down") or from schematic extraction ("bottom-up")?

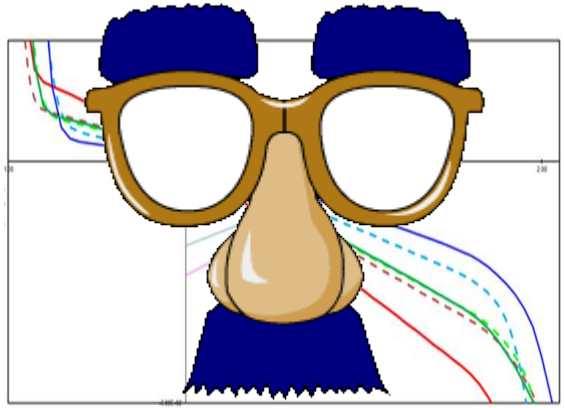
Your trade-off…

- Extracted models are likely GetWave (Bitstream) only
- Statistical models, if created through a template, will make architectural assumptions involving algorithms and LTI-ness
- More on this dual-model issue later…



Beyond Single AMI Models

For system design simulations where multiple device combinations can be supported, two items are needed



- Generic, specification-compliant models
- Statistical models (both senses of the word)

Specification-compliant *point* models are not sufficient – generic models ideally should cover the full supported range of the specification

Can interface specification/standards bodies provide generic IBIS-AMI models?

Image courtesy https://commons.wikimedia.org/w/index.php?curid=63518739

Question 2

AMI MODEL BUILDING:

Can a mere human succeed at developing an AMI model? It seems creating AMI models requires a lot of non-SI skills like memory management, manipulating libraries of mathematical functions, C++ programming and compilation, etc.

Do we need dual (getwave/init) models? When? Why? Do model development and simulation environments support both?

What are the most important AMI model features when simulating at the system level? What model elements need to be precise?

4 min – jb, 4:15

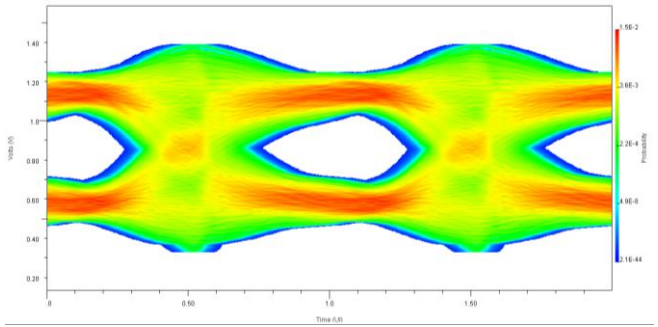
AMI Model Building

- Succeeding at developing IBIS-AMI
  - (SI Engineer perspective)
  - Available EDA Vendor model development tools / flows
    - Support is available for developing models
    - Tools can export portable IBIS-AMI models
    - Example code
    - Libraries with functions and building blocks
  - Some C++ programming knowledge helpful, but not required
  - In depth understanding of equalization circuits and algorithms is required
    - Circuit limitations
    - Non-linearities
    - Jitter contributions

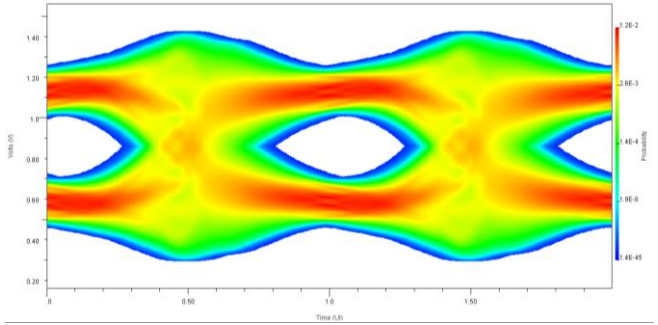
AMI Model Building

- Dual models
  - Could be useful in some cases:
    - No time varying effects, e.g. Rx DFE taps are fixed
    - Model some non-linearities with AMI_GetWave
    - Perform deep BER analysis with AMI_Init
  - For DDR, we are currently looking into this by comparing:
    - Running long transient analysis and extrapolating down to desired BER
    - Running a fully statistical flow
  - More support is necessary in model development flows and simulation flows

AMI_GetWave



AMI_Init

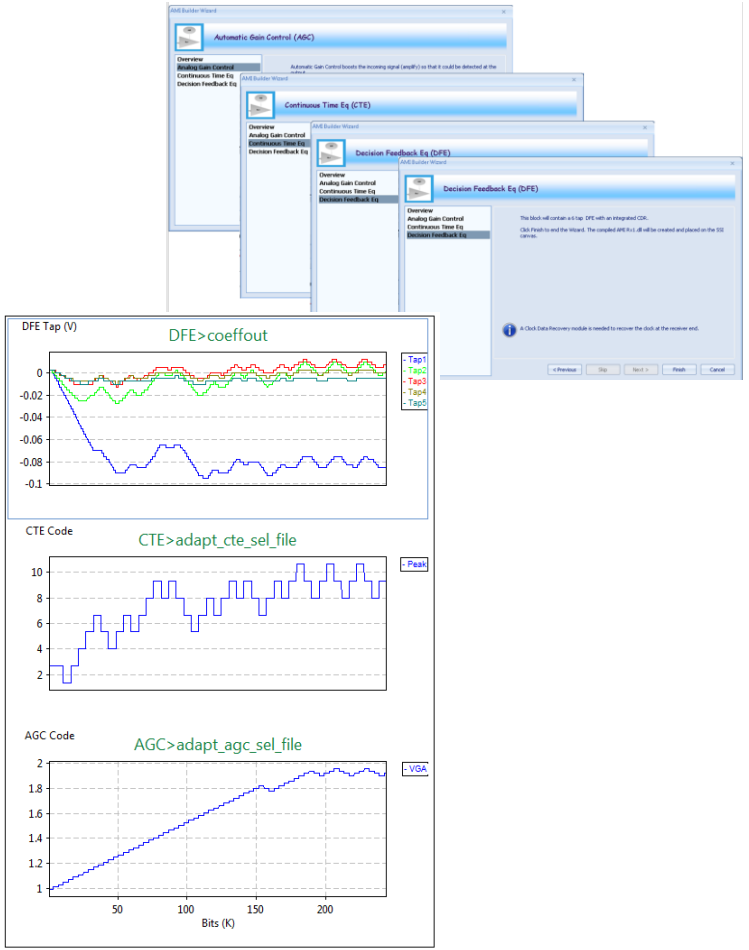


AMI Model Building

- Model features that need to be precise:
  - Anything that effects the analog signal at the Rx input
  - Analog buffer characteristics (input capacitance, slew rate, output impedance, etc.)
- Model features that must be statistically accurate:
  - Corner variation
  - Some Rx equalization characteristics
    - May have some random silicon effects more suited to Monte-Carlo simulation
    - Consider the Rx Mask, Rx_Receiver_Sensitivity, etc.

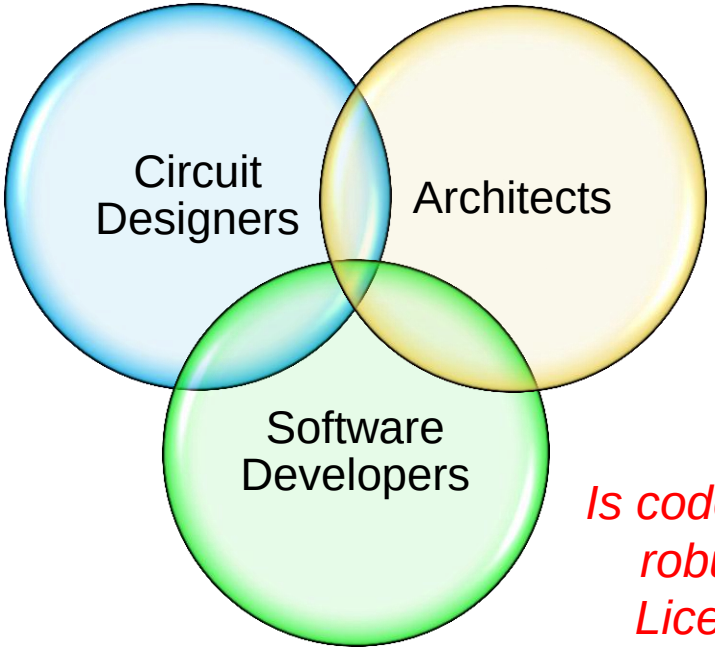
AMI Model Building

- Can a mere human succeed at developing an AMI model?
  - Yes, easy today, wizard-driven
  - Robust building blocks for all common modules (FFE, AGC/VGA. CTLE, DFE) already exist
- Do we need dual getwave / init models?
  - NO! Unnecessary complexity
- What are the most important AMI model features?
  - IBIS part > C_comp
  - Number of taps and tap limits
  - Curve descriptions for peaking filters (CTLE)
  - Adaptation times for the different sub-modules



A Model for IBIS-AMI Model Building

What are the buffer noise parameters? What are the analog characteristics?



How does equalization, adaptation work? What control parameters exist, with what ranges?

Is code correct, efficient, robust and secure? Licensed? Signed?

… leaving aside documentation, testing in simulation software.
Ideally, all three people above are… one person.

Do We Need Dual Models?

YES

- Statistical‡ studies require statistical‡ models
  - *Repeaters are a particularly critical application, and an IBIS gap exists*
- The SPICE problem from 25 years ago still applies: how much are you willing to trade off simulation accuracy (and coverage) for simulation speed?

An underlying question: how non-LTI is your device in reality?
Can you use an LTI model in your system simulations, and with what margin targets or allowances?

‡Statistical as in Design of Experiments or high-volume manufacturing variation, and statistical as in contrast to bit-by-bit

Statistical Coverage in Models

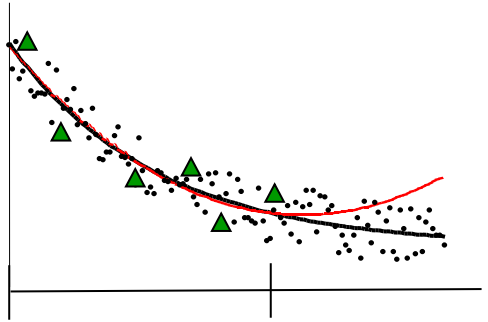
Devices vary over process, voltage, temperature…

Realistic solutions are not just based on worst-case behavior

- Viable solution spaces comprehend the likelihood of corner combinations – DOE and model fits are useful, fast techniques

Device behaviors, including configuration settings, must be covered in system analyses

- What settings are optimal across process, environmental, and manufacturing variations?
- If the device is self-adaptive, do the final settings assure robust operation?



See Mirmak, 2010:
http://ibis.org/summits/jun10/mirmak.pdf

Statistical (e.g., DOE) simulation coverage strongly implies fast Statistical (Init) models

Q3.1: AMI MODEL BUILDING: Can a mere human succeed at developing an AMI model? It seems creating AMI models requires a lot of non-SI skills like memory management, manipulating libraries of mathematical functions, C++ programming and compilation, etc.

- In the beginning, NO
  - SerDes Architects designed and verified equalization algorithms in MATLAB
  - Silicon Designers implemented the algorithms in in silicon
  - AMI Modelers then wrote “C” AMI models to match what the Silicon Designer did
  - Converting the MATLAB code to “C”, dealing with memory management has been very difficult, especially as equalization methods and adaptation methods have become more complex.

Yes, with SerDes Toolbox

- SerDes Toolbox deals with all of the memory management issues required by IBIS-AMI.
- SerDes Architects: Yes
- Signal Integrity Engineers: Yes
- IBIS-AMI Modelers: Yes

Algorithmic development language: MATLAB

Q3.1: Do we need Dual (GetWave/Init) models? When? Why?

- Yes
  - What is the model user to do when his Tx is GetWave Only and his Rx is Init Only?
  - Some IC vendors generate Init Only models.
  - Some IC vendors generate GetWave Only models.
  - Some EDA vendor tools generate Init Only models.
  - Some EDA vendor tools generate GetWave Only models.
  - There are 9 combinations of Tx and Rx Dual, Init Only and GetWave Only configurations.
  - There are 81 combinations of Tx, Repeater Rx, Repeater Tx and Rx Dual, Init Only and GetWave Only configurations.
- Many of these combinations are problematic, and there is ongoing debate within IBIS on how to deal with them.
- SerDes Toolbox generates can generate Init Only and GetWave Only models, but SerDes Toolbox excels at generating Dual Models.

Q3.2: What are the most important AMI model features when simulating at the system level? What model elements need to be precise?

- Performance and *sufficient* accuracy.
- Co-optimization of Tx and Rx models
  - What are the best equalization settings to optimize the channel performance?
  - How close do the adaptation algorithms in the hardware get to the best equalization settings?

Question 3

AMI MODEL FEATURES:

What is the new thing in a SerDes?

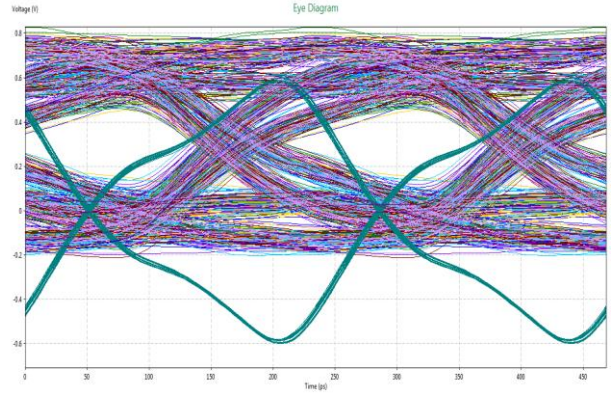
AMI compilation offers flexibility, but is it still useful?
It has been 10+ years since we added the DFE.

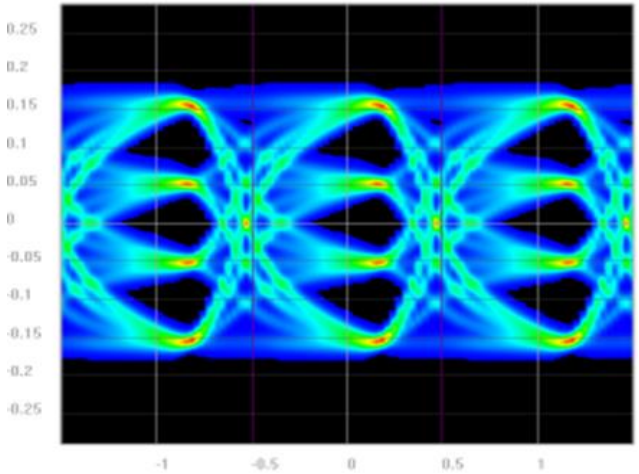
Does AMI adequately handle the new issues in DDR5? What do attendees need to know about modeling and simulating that?

4 min – kw, 4:30

New AMI Model Features

- DDR4 / DDR5
  - Uses external strobe signal vs. clock recovery
  - CDR useful approximation for now
  - AMI models will need to take that external strobe waveform in for clocking (jitter challenged)
  - Backchannel style training
- PAM4
  - Some syntax in IBIS 6.1 spec for PAM4
  - Building blocks and algorithms need to catch up to handle multi-level signaling
  - Shift toward receiver for EQ functionality as data rates skyrocket (ex. FFE in Rx due to DFE-induced burst errors)

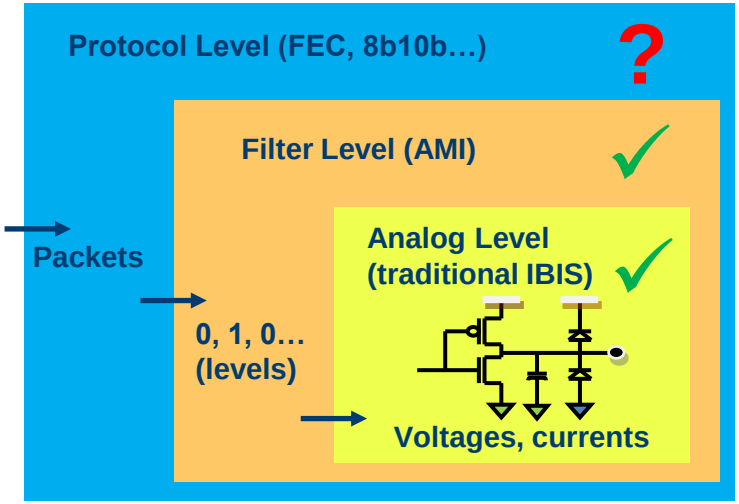




AMI Model Features – What's Missing?

SerDes Features in IBIS:

- PAM4 exists now, and is a template for PAM*n*
- Backchannel is in IBIS 7.0, finally!



Some in industry request FEC support

- Post-processing outside of today's IBIS-AMI
- Could be supported through model-level reporting to tool (LaBonte & Westerhoff, 2018)

Do we need IBIS to support protocol-level analysis?
Possible for Bitstream models, difficult for Statistical models

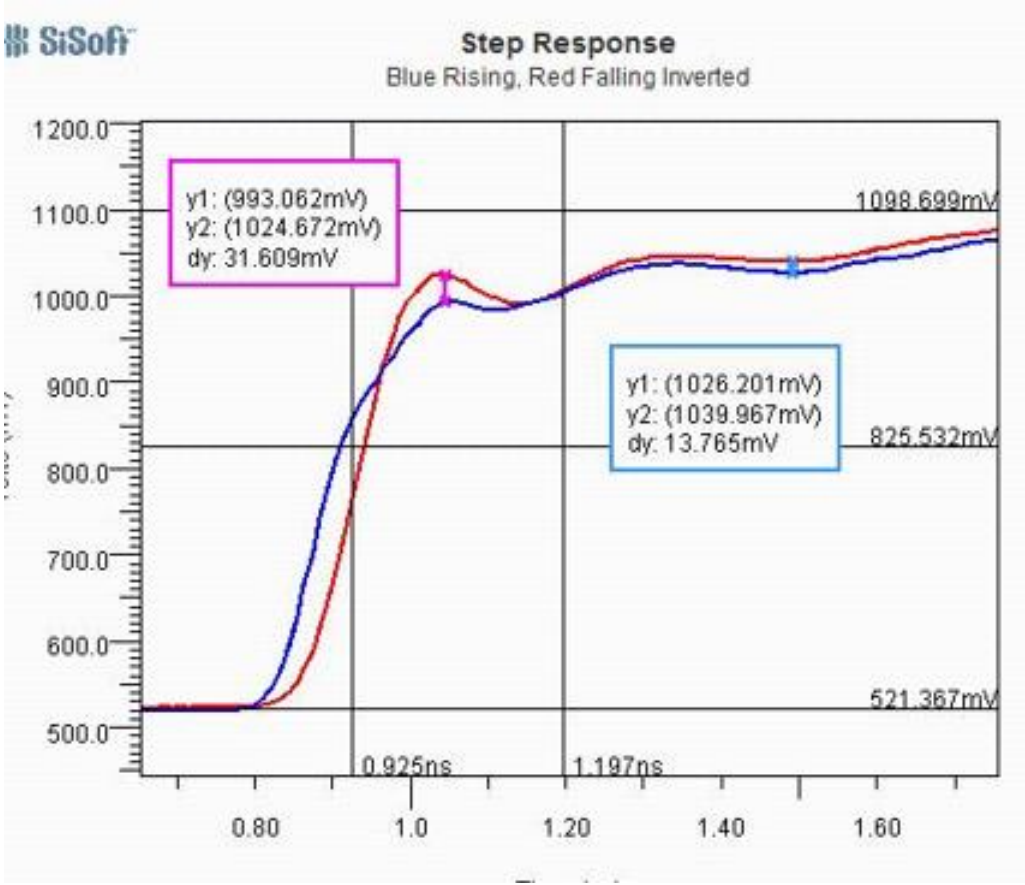
Q4.1: AMI MODEL FEATURES: What is the new thing in a SerDes? It has been 10+ years since we added the DFE. AMI compilation offers flexibility, but is it still useful?

- PAM4
- DDR5
  - Single-Ended signaling
  - Bi-Directional signaling
  - Multi-drop signaling
- Rx models that have an FFE or a DFFE
- Rx models that replace the DFE with an ADC (Analog to Digital Converter) and a DSP (Digital Signal Processor)
- Global adaptation methods.

Q4.2: Does AMI adequately handle the new issues in DDR5? What do attendees need to know about modeling and simulating that?

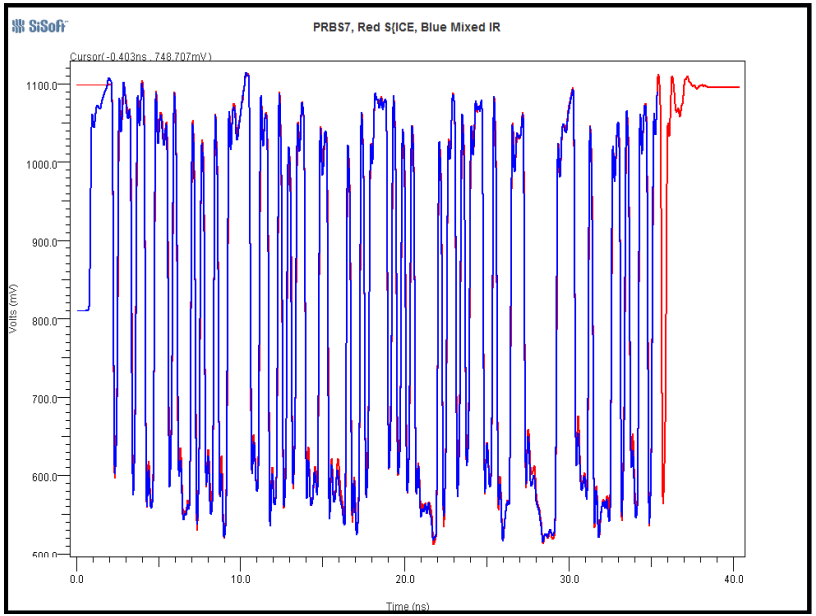
- DDR5 is different then traditional SerDes
  - Bi-Directional
    - IBIS enhanced to have different AMI models for reads and writes
  - Clock is forwarded, not recovered from data
  - The DQ/DQS skew is trained by the controller
  - The DFE Taps are determined by the controller
  - Hardware microcode algorithms rely on BER metrics to train the channel.
  - The SDRAM Rx AMI model can tell the controller Tx model how to adjust DQ/DQS skew and DFE taps by analyzing the channel impulse response. Single Ended, not differential
  - Assumption that signal inside Rx buffer is “differential” after VrefDQ is subtracted from the signal
  - Different rise and fall times and high and low drive impedance need to be accounted for.

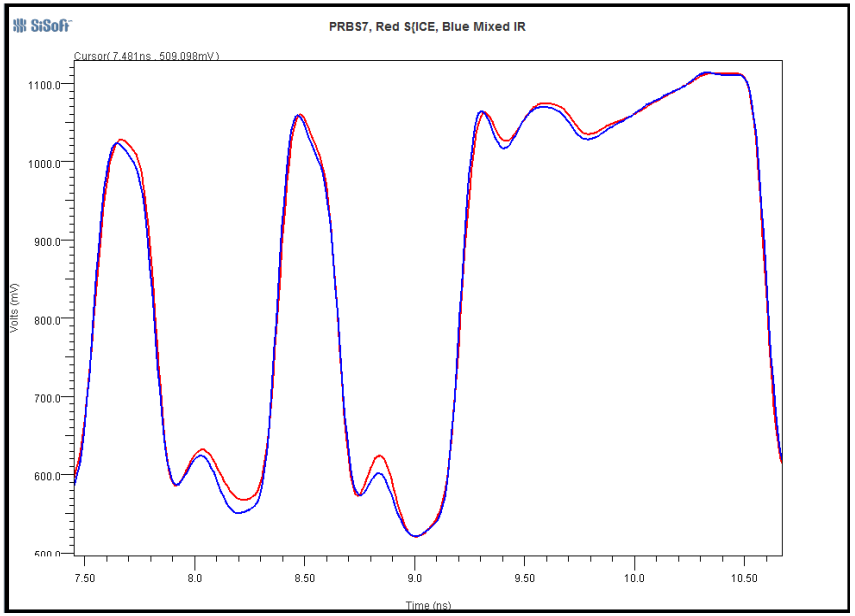
Q4.3: Rise and fall times are different
High and low Tx impedances are different



Q4.3: I am giving a paper at the IBIS Summit this Friday showing the magnitude of this affect and how it can be minimized.

- SPICE Simulations are very close to IBIS-AMI convolutions using both rising and falling impulse response.





AMI Model Features

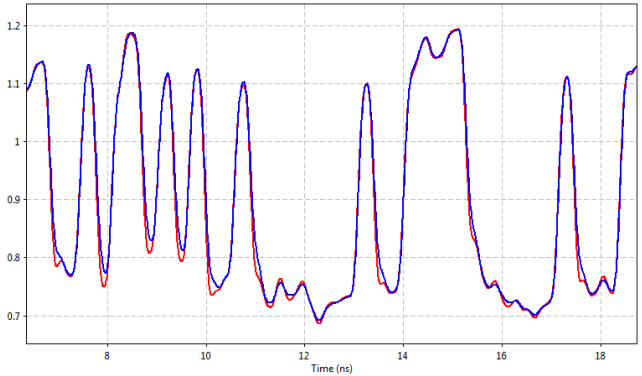
- Number of new things on the horizon:
  - Equalization capabilities expected for DDR5
  - Other DDR style interfaces with equalization
  - IBIS-AMI for single-ended
  - IBIS-AMI for forwarded clock (source synchronous) architectures
- DDR5 expected equalization
  - JEDEC Specification still in development
  - Requires new modeling and simulation approaches
    - Statistical simulation techniques
    - IBIS-AMI is useful, but only one piece
  - Micron still offering
    - IBIS with non-linear characteristics captured
    - Power-Aware IBIS

AMI Model Features

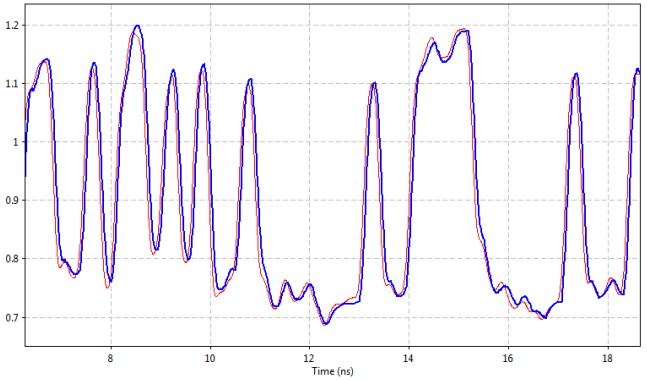
- Challenges with IBIS-AMI for DDR5
  - Common mode voltage / DC offset
    - IBIS-AMI flows remove DC common mode voltage
    - Proposed BIRD to address this
  - Non-linear characteristics
    - Driver mismatched Pullup / Pulldown impedances
    - Rise / Fall time differences
    - EDA tool solutions in progress
  - SSO / Power Supply Noise
    - May be necessary to analyze outside the AMI flow
    - Apply SSO impairments as jitter / noise PDF
  - Forwarded Clock
    - Existing jitter Reserved Parameters
  - Great work being done to address these challenges!

IBIS Transient vs. GetWave Simulation

Rise Step Response



PRBS Characterization



AUDIENCE QUESTIONS

Question

Are AMI models correlated to silicon? What's the right way to do that? Is it done at all? What happens when this isn't done? Does physical layout change behavior?

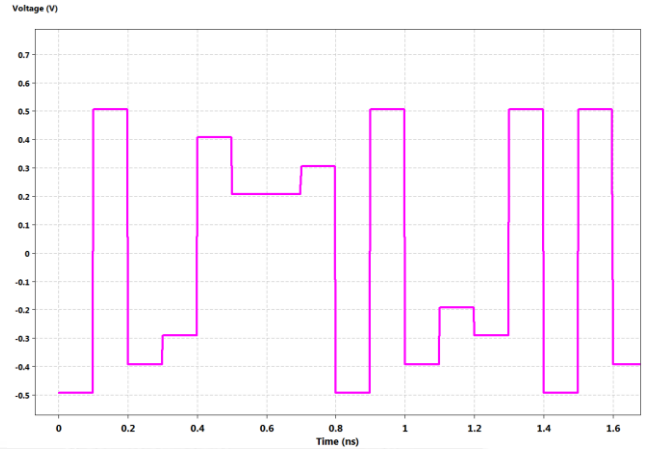
When correlating models to measurement, what constitutes "acceptable"?

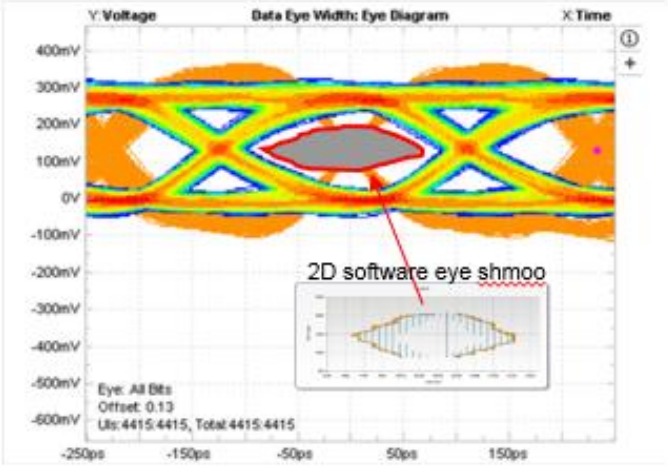
AMI Model Correlation

- Analog model effects
  - (Input capacitance, slew rate, output impedance, etc.)
  - Should be correlated to silicon
  - Micron supportive of this, providing detailed quality reports with correlation to silicon
- Equalization models should be correlated to silicon, where possible
  - Techniques not as straight forward as analog model measurement correlation
  - Limited ability to probe inside Rx equalization circuits
- Physical layouts can change characteristics
  - This depends on circuit design techniques
  - Model makers' engineering judgement
- Acceptable correlation criteria should consider
  - The specification, including Rx mask requirements
  - Model covers the corner variation
  - Model is useful for system designer to make engineering decisions

AMI Model Correlation

- Transmitter
  - Drive into a 50 ohm test load
  - Waveform based correlation vs. transistor-level or measurement results
- Receiver
  - Eye contour or bathtub curves if simulator-based
  - Can compare final adapted coefficient values
  - Eye height and width to compare with measurement
  - Can use embedded eye plotter (if present) in IP from lab measurement
  - Can also utilize IBIS-AMI model in oscilloscope (ex. Tektronix)





AMI Model Correlation

- Many of our customers require that AMI models are correlated to silicon.
- There are multiple ways to do that
  - Compare models with transistor SPICE simulations
  - Compare models with internal buffer metrics (e.g. Eye Scan)
  - Simulate with stressed eye and compare with lab measurements
- If correlation is not done, end up with failing channels

- Acceptable means the engineer can design a channel using the model that will not fail and have sufficient margin.

Question

Are the algorithmic techniques available in IBIS-AMI

useful for modeling the analog behaviors

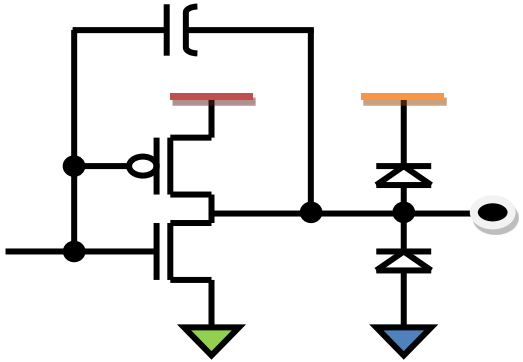
of other types of IOs

beyond those originally intended for AMI?

Challenges: New Whine in an Old Bottle

Can algorithmic techniques address analog problems?

- Analog buffer modeling is still needed and relevant
- IBIS's table-driven "snapshot" approach cannot capture effects such as feedback



This could be an actual design, or simply a representation of Miller capacitance effects

Can IBIS-AMI approaches (e.g., transfer functions) be used to model this kind of circuit?

Image from "The History and Evolution of IBIS Modeling", DesignCon 2016

Expanding AMI Uses

- Single-Ended
  - One example, although not exclusive analog behaviors
  - AMI Intentions:
    - Intended for differential
    - Intended to have CDR
    - Single-ended not explicitly prohibited
  - Already in the works with model makers and EDA tools
  - Some changes to IBIS necessary
    - BIRD197 in the works
    - Slight modifications to existing EDA flows
    - Possible changes to accommodate clock forwarding?

Are algorithmic techniques available in IBIS-AMI useful for modeling the analog behaviors of other types of I/O

- IBIS-AMI is based on the “high impedance interface” between generating the thumbprint of the analog channel and the equalization applied inside the buffer.
- On the buffer side of the “high impedance interface” IBIS AMI models could be used to more accurately represent the derating tables in the DDR4 specification.
  - On the analog channel side of the “high impedance interface”, IBIS AMI allows replacing the IBIS analog [Model] with a Touchstone model.
  - In IBIS 7.0, an on-die Touchstone model can be included with an on-die package model.
  - Currently under discussion is a new C_comp model BIRD which will also allow broadband analog models inserted between the [Model] pad and the die pad.

Question

How useful is IBIS-AMI to study pre-silicon (architectural) equalization implementation options?

AMI for Architectural Decisions

- We think this is going to become critical for the design of the next generation of Rx models
- Being able to compare the channel performance of Rx buffers with different CTLE, AGC, FFE, DFFE, ADC, and DSP algorithms, and do this on large data sets of different channels will require fast models using EDA tools that can run a large number of simulation in parallel.
- Top-Down design tools will be required to allow SerDes Architects to do these kinds of tradeoffs easily. Then refining the selected architecture using bottom up techniques while the actual silicon is being designed.

AMI for Architectural Decisions

- IBIS-AMI can be useful to study equalization implementation options
  - Models can be specially built for internal purposes
    - Include features up for consideration
    - Model users can enable / disable equalization features with AMI input parameters
  - Model users can perform large sweeps / DOE analysis
    - Compiled executables run faster
    - Leverage SI simulation tools for simulations
  - IBIS-AMI can be a good go between
    - Enable SI Engineers to give feedback to Chip Design Engineers
    - Each may have different simulation tools and methodologies

Question

Are there differences between the AMI spec and the actual models?

What is “portability” meant to achieve?

AMI Portability

- Goal of IBIS-AMI Portability
  - IBIS-AMI defines the interface for data to pass in and out of the AMI executable in a standard way
- IBIS “Triangle”
  - EDA Tool Vendors
  - IC Vendor / Model Makers
  - System Designer / Model Users
  - Model portability should be respected for each to achieve their goals
- Micron’s goal:
  - Diverse customers using many different tools
  - Enable one model to simulate in all tools

Differences Between the AMI Spec and Actual Models

- Yes, but the situation is getting better.
- We have an IBIS-AMI model certification process that identifies problems with models that do not behave according to the spec.
- Many of our customers require correlation of the results of AMI simulations in our tool with the results from other tools. This requires that the model is compliant with the spec and the tool is compliant with the usage of the model.

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THANK YOU