References

Donald Telian's Published Works

For additional information, see also: http://siguys.com/published-works/

All links accessed December 2021.

[1]   DesignCon AMI Panel: "Succeeding with Next-Generation AMI Models & Analysis"
       http://siguys.com/wp-content/uploads/2016/01/
       SLIDES_Track2Panel_SucceedingWithNextGenerationAMI_Telian.pdf

[2]   SiSoft SI Article Series: Signal Integrity, In Practice
       SiSoft's website has been fully transitioned to The MathWorks, Inc. ®

[3]   DesignCon AMI Panel: "Which Model When? Succeeding with IBIS-AMI"
       http://siguys.com/wp-content/uploads/2019/02/
       SLIDES_Track2_WhichModelWhenSuceedingAMI_TelianD.pdf

[4]   DesignCon Boot Camp Course: Pragmatic Signal Integrity
       http://siguys.com/seminars/

[5]   DesignCon AMI Panel: "IBIS-AMI: New Users, New Uses"
       http://siguys.com/wp-content/uploads/2018/02/
       2018_DesignCon_AMI_Panel_NewUsersNewUses.pdf

[6]   DesignCon AMI Panel: "Getting the Most from IBIS-AMI: Tips & Secrets from the Experts"
       http://siguys.com/wp-content/uploads/2017/02/
       2017_DesignCon_AMIpanel_TipsSecretsFromExperts.pdf

[7]   PCB Design Magazine July 2016: "New SI Techniques" (page 12)
       http://www.magazines007.com/pdf/PCBD-July2016.pdf

[8]   SPI Italy: "7 Challenging SI/PI Problems That Have NO Existing Solution"
       http://siguys.com/wp-content/uploads/2016/06/
       2016_7_SI_Problems_No_Solution_Telian_SPI_2016.pdf

[9]   European IBIS Summit: "Using IBIS-AMI Models to Maximize Performance Given SerDes EQ and Channel ISI & Loss"
       http://siguys.com/wp-content/uploads/2016/06/
       2016_UsingAMImodelsMaximizePerformance_IBISsummit.pdf

[10]   DesignCon Paper: "New SI Techniques for Large System Performance Tuning"
       http://siguys.com/wp-content/uploads/2016/01/
       2016_DesignCon_NewTechniquesPerformanceTuning.pdf

[11] DesignCon Paper: "Building Accurate IBIS-AMI Models from Datasheets and Lab Measurement"
http://siguys.com/wp-content/uploads/2016/01/
2016_DesignCon_BuildingIBISAMIModelsFromDatasheets.pdf

[12] DesignCon AMI Panel: "Accurate AMI Analysis - Whose Responsibility Is It?"
http://siguys.com/wp-content/uploads/2016/01/
2016_DesignCon_AccurateAMIAnalysisWhoseResponsibilityIsIt.pdf

[13] DesignCon Session: "A SerDes Balancing Act: Co-Optimizing Tx and Rx Equalization Settings to Maximize Margin"
http://siguys.com/wp-content/uploads/2017/02/
Slides-A_SerDes_Balancing_Act_Co-Optimizing_Tx_Rx-publish.pdf

[14] Video Interview on Signal Integrity
https://protoexpress.wistia.com/medias/8w5l5nt7kl

[15] EDN Article: Accurate AMI Analysis - Whose Responsibility Is It?
http://www.edn.com/electronics-blogs/designcon-central-/4441153/Accurate-AMI-Analysis---Whose-Responsibility-Is-It--

[16] DesignCon AMI Panel: "Can we use AMI analysis to predict meaningful BERs?"
http://siguys.com/wp-content/uploads/2016/01/
2015_DesignConPanel_CanWeUseAMIforBER_Slides.pdf

[17] DesignCon Best Paper Award: "Moving Higher Data Rate Serial Links into Production - Issues & Solutions"
http://siguys.com/wp-content/uploads/2016/01/
2014_DesignCon_MovingToHigherDataRates_paper.pdf

[18] DesignCon Paper: "Fast, efficient, and accurate: via models that correlate to 20 GHz"
http://siguys.com/wp-content/uploads/2016/01/
2013_DesignCon_FastEfficientAccurateVias_paper.pdf

[19] DesignCon Paper: "Simulating Large Systems with Thousands of Serial Links"
http://siguys.com/wp-content/uploads/2016/01/
2012_DesignCon_SimulatingThousandsofLinks_paper.pdf

[20] Tutorial: "Channel Eye Diagram Generation, Pre-Hardware"
http://siguys.com/wp-content/uploads/2016/01/
2012_DesignCon_EyeGenerationPreHardwareTutorial.pdf

[21] DesignCon Paper: "Simulation Techniques for 6+ Gbps Serial Links"
http://siguys.com/wp-content/uploads/2016/01/
2010_DesignCon_6GbpsSimTechniques_Paper.pdf

[22] Webinar: "Advanced Techniques for Channel Analysis"
http://siguys.com/wp-content/uploads/2016/01/
2009_Webinar_Advanced_CA_Techniques_Slides.pdf

[23] DesignCon Paper Award: "New Serial Link Simulation Process, 6 Gbps SAS Case Study"
http://siguys.com/wp-content/uploads/2016/01/
2009_DesignCon_6Gbps_Simulation_Paper.pdf

[24] XrossTalk Magazine: "A Process for Serial Link Signal Integrity Analysis"
http://siguys.com/wp-content/uploads/2016/01/
2009_XrosstalkMagazine_SerialLinkSI_Process.pdf

[25] CDNLive MVP: "New Technologies for 6 Gbps Serial Link Design & Simulation, a Case Study"
http://siguys.com/wp-content/uploads/2016/01/
2008_CDNLive_New_Tech_for_6Gbps_Serial_Link_Sims_SAS.pdf

[26] Article: "Signals on Serial Links: Now you see 'em, now you don't."
http://siguys.com/wp-content/uploads/2016/01/
2007_Article_SignalsOnSerialLinks.pdf

[27] EETimes Article: "Soaring data rates signal coming crisis"
https://www.eetimes.com/soaring-data-rates-signal-coming-crisis/#

[28] CDNLive: "Using Allegro PCB SI to make your Multi-GHz Serial Link work right out of the box"
http://siguys.com/wp-content/uploads/2016/01/
2007_CDNLive_MGH_Serial_Links_SATA.pdf

[29] CDNLive: "Adapting Signal Integrity Tools and Techniques for 6 Gbps and Beyond"
http://siguys.com/wp-content/uploads/2016/01/
2007_CDNLive_Adapting_SI_Tools_for_6Gbps.pdf

[30] DesignCon: "New Techniques for Designing and Analyzing Multi-GigaHertz Serial Links"
http://siguys.com/wp-content/uploads/2016/01/
2005_DesignCon_New_MGH_Techniques_ISP_CA_PCIe_SATA.pdf

[31] IBIS Summit: "Modeling Complex IO with IBIS 4.1"
http://siguys.com/wp-content/uploads/2016/01/
2005_IBIS_Summit_ModelingComplexIO.pdf

[32] EETimes/EDN Article: "IBIS can help model gigabit pre-emphasis"
https://www.edn.com/ibis-can-help-model-gigabit-pre-emphasis/

[33] Webinar: "New IBIS Techniques for Modeling Complex IO"
http://siguys.com/wp-content/uploads/2016/01/
2005_Webinar_Modeling_ComplexIO.pdf

[34] Paper: "S-Parameter Correlation of typical PCB interconnect structures"
http://siguys.com/wp-content/uploads/2016/01/2004_Paper_S-Parameter_Correlation_of_PCBs.pdf

[35] Cadence Webinar: "Introducing Channel Analysis for PCB Systems"
http://siguys.com/wp-content/uploads/2016/01/2004_Webinar_Introducing_Channel_Analysis.pdf

[36] Cadence Webinar: "Understanding and Using S-Parameters for PCB Signal Integrity"
http://siguys.com/wp-content/uploads/2016/01/2004_Webinar_UnderstandingUsing_S-parameters_for_PCB_SI.pdf

[37] "How to Build Fast and Accurate Multi-Gigabit Transceiver Models"
http://siguys.com/wp-content/uploads/2016/01/2004_Webinar_HowToBuild_Xcvr_MacroModels.pdf

[38] Xcell Journal: "Surf the Serial Wave to Success"
http://siguys.com/wp-content/uploads/2016/01/2003_XcellJournal_Surf_the_Serial_Wave.pdf

[39] ICUG: "Optimizing your Design Chain with Design Kits – Practical Advice for Kit Builders and Kit Users"
http://siguys.com/wp-content/uploads/2016/01/2002_ICUG_Optimizing_DesignChain_with_Design_Kits.pdf

[40] "Implementing Muilti-Gigabit Serial Links in a System of PCBs"
http://siguys.com/wp-content/uploads/2016/01/2002_ProgWorld_Implementing_Multi-Gigabit_Serial_Links.pdf

[41] Xcell Journal: "Get up to Multi-Gigabit Speed"
http://siguys.com/wp-content/uploads/2016/01/2002_XcellJournal_Multi-Gigabit_Speed.pdf

[42] IBIS Summit: "Behavioral Receiver Modeling"
http://siguys.com/wp-content/uploads/2016/01/2000_IBIS_Summit_Behavioral_Rx_Modeling.pdf

[43] "Definition of High-Speed"
https://www.qsl.net/wb6tpu/si-list3/0514.html

[44] DesignCon: "An Optimized Methodology for High-Speed Design"
http://siguys.com/wp-content/uploads/2016/01/1998_DesignCon_Optimized_SI_Methodology.pdf

[45] DesignCon Best Paper: "Signal Integrity Engineering in High-Speed Digital Systems"
http://siguys.com/wp-content/uploads/2019/03/1997_DesignSuperconSI_eng_Telian.pdf,
See also: http://siguys.com/wp-content/uploads/2016/01/1997_DesignCon_HighSpeedDesign.pdf

[46] EDN: "Treat pc-board traces as transmission lines to specify drive buffers"
http://siguys.com/wp-content/uploads/2016/01/1993_EDN_Treat_PCB_traces_as_tlines.pdf

[47] IBIS: "Telian founds IBIS Open Forum"
http://ibis.org/minutes/min1993/M042393.TXT

[48] US Patent 5,028,809: "Computer Bus Structure Permitting Replacement of Modules During Operation"
http://siguys.com/wp-content/uploads/2016/01/1991_USPatent_Computer_bus_structure_permitting_replacement.pdf

Industry References

Links accessed December 2021.

[49] "All Models Are Wrong, but some are useful"
https://en.wikipedia.org/wiki/All_models_are_wrong

[50] Michael Steinberger
https://www.edn.com/designcon-names-mike-steinberger-engineer-of-the-year/

[51] IBIS Open Forum Minutes, June 4 1993
https://ibis.org/minutes/min1993/M060493.TXT

[52] Moore's Law
https://en.wikipedia.org/wiki/Moore%27s_law#/media/File:Moore's_Law_Transistor_Count_1971-2018.png

[53] Jim Pappas on Industry-standard Busses
https://www.eetimes.com/buses-keep-pace-by-switching-serializing/

[54] Eric Bogatin
https://www.colorado.edu/faculty/bogatin/

[55] EEWeb PCB Trace Impedance Solver
https://www.eeweb.com/tools/edge-coupled-stripline-impedance/

[56] Mike Steinberger explains Time Domain Reflectometry (TDR)
http://siguys.com/wp-content/uploads/2016/01/TDR_TeaLeaves.pdf

[57] "When Shorter Isn't Better", Steinberger, Wildes, et. al.
DesignCon 2010

[58] "It's Turtles all the way Down"
https://en.wikipedia.org/wiki/Turtles_all_the_way_down

[59] Eric Bogatin's 20 Rules for Engineering
https://www.signalintegrityjournal.com/blogs/4-eric-bogatin-signal-integrity-journal-technical-editor/post/1539-bogatins-20-rules-for-engineers

[60] "IBIS-AMI: Assumptions, Terminology & Analytical Flows", SiSoft
http://ibis.org/summits/feb17/katz.pdf

[61] About DDR SDRAM
https://en.wikipedia.org/wiki/DDR_SDRAM

[62] "Addressing DDR5 design challenges with IBIS-AMI modeling techniques" Westerhoff et. al.
https://ibis.org/summits/feb18/westerhoff.pdf

[63] EEWeb Crosstalk Calculator
https://www.eeweb.com/tools/stripline/

[64] Seymour Cray, the father of supercomputing
https://en.wikipedia.org/wiki/Seymour_Cray

[65] "Decoupling Capacitor Calculations for CMOS Circuits" Larry D. Smith
http://pdnpowerintegrity.com/wp-content/uploads/2018/05/epep_1994-Decoupling-Capacitor-Calculations-for-CMOS-Circuits.pdf

[66] GigaTest Labs
https://gigatest.com/engineering-services/

[67] "Getting Street-Smart About S Parameters" SiSoft, DesignCon 2015

[68] Frank Burge
https://www.edn.com/frank-burge-who-helped-launch-apple-dead-at-78/

[69] "A Simple Via Experiment" Steinberger et. al., DesignCon 2009

[70] IBIS Open Forum, https://ibis.org/

[71] "Easier Signal Integrity Simulation Setup with IBIS 7.0" Mike LaBonte
https://www.signalintegrityjournal.com/blogs/12-fundamentals/post/1278-coming-up-easier-signal-integrity-simulation-setup-with-ibis-70

[72] "System-level Serial Link Analysis using IBIS-AMI Models" Westerhoff
https://ibis.org/summits/nov08a/westerhoff.pdf

[73] SiSoft QCD (Quantum Channel Designer), DesignCon 2009 Design Vision Award

[74] 802.3 COM and Channel Downloads
http://www.ieee802.org/3/ck/public/tools/index.html