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Santa Clara Convention Center

PCIe Gen5 Signal Integrity Implementation – Issues & Solutions

Donald Telian, SiGuys
Kevin Rowett, Xconn Technologies
Ilya Teplitsky, Hardware Consultant

SPEAKERS

Donald Telian

SI Consultant / Owner, SiGuys

telian@siguys.com | siguys.com

Building on 40 years of SI experience at Intel, Cadence, HP, and others, his focus is helping customers implement today's highest-speed serial links. With tens of thousands of serial links in production spanning all types of electronic standards and products, he consistently helps his customers migrate to next-generation data rates again and again. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. His new book "Signal Integrity, In Practice" brings fresh articulation to the changing practice of SI in the decades ahead.

Kevin Rowett

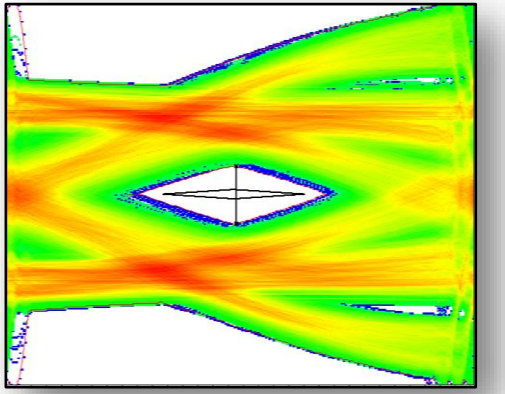
VP Systems Engineering, Xconn Technologies – Owner, Iron Heart Consulting

kevin.rowett@xconn-tech.com | xconn-tech.com

Providing engineering consulting services for technology companies at all stages and sizes, Kevin brings skills in hardware, software, project management, technical communications, and organizational management. Well-known in Silicon Valley, he has worked as an engineering team lead, engineering manager, and executive at many high-tech companies including Tandem, IBM, and Cisco. He has founded six startup high technology companies, including Force10 Networks, Mistletoe Technologies, and Violin Memory.

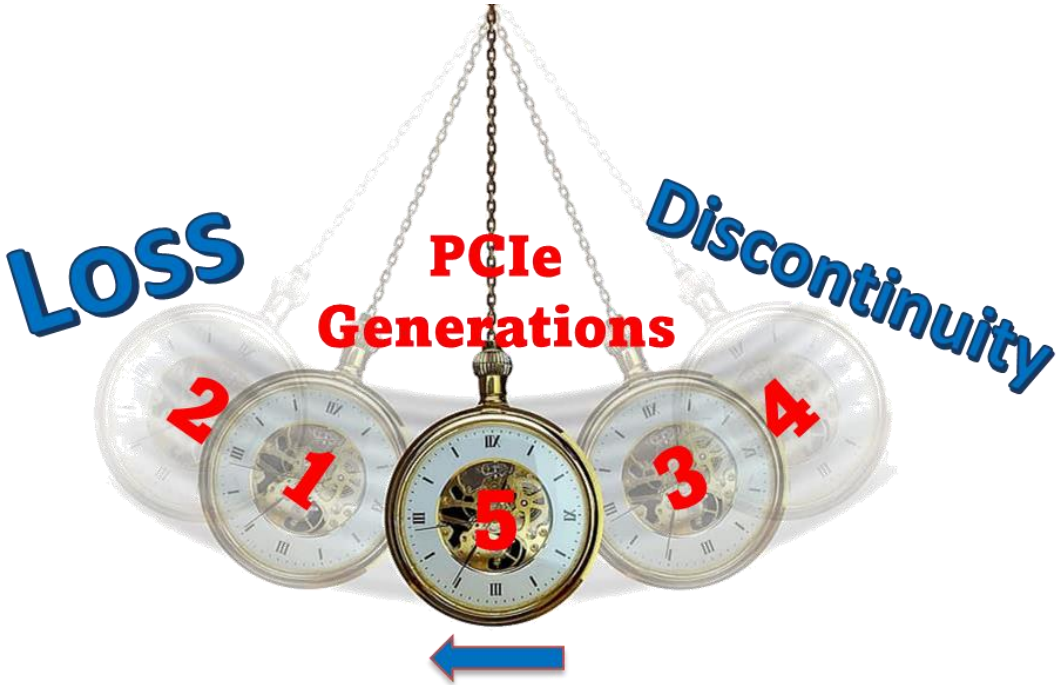
AGENDA: PCIe Gen5 Signal Integrity

- Introduction
- Handling Loss
- Everything is a Discontinuity
- The System Level
- Summary



The PCIe Pendulum Swings

- **Loss at a cross-roads**
  - Measure <-> Simulate
- ***"not yet had a single PCB measurement that confirms IL is as low as we hoped"*** (page 8)
- **Cables to the rescue**
  - PCB loss 10x greater than cable loss
  - 2" route ~= 20" cable



Consequences of Increasing Data Rate

- **36 dB!**
- **Everything is a discontinuity**
- **Stubs are everywhere**
- **SI "Cheat Sheet"**
  - See EDIcon 2022

Feature	4 Gbps	8 Gbps	16 Gbps	32 Gbps	Unit	SIiP Section
Industry/PCIe terminology	Gen2	Gen3	Gen4	Gen5		
Fundamental Frequency	2	4	8	16	GHz	
Relevant Feature Size what's that?	160 traces	80 vias	40 conn pads	20 everything	mils	4.1, 2.1, 4.x 4.2, 4.3, 4.4
Max Stub backdrills	64 none?	32 seq-lam	16 2 layers	8 per-layer	mils	2.5, 1.3.3
P/N Matching, static	10	5	2	1	mils	2.3
P/N Matching, dynamic			10 in 1.5"	5 in 1"	mils	2.3, 2.4
Route Style	45°	45°	curved	curved		2.4
Diff-pair Spacing (XY/Z, min)	25	25	25	30	mils	5.3
Insertion Loss (max)	16	22	28	36	dB	2.2, 3.5
Min EQ: Tx_FFE/Rx_DFE taps, CTLE	1 / 0	2 / 1, C	2 / 2, C	2 / 3, C	#taps	3.3, 3.4, 2.7
Length match method	serpentines		irregular spaced bumps			2.4
Fiberglass weave	spread glass and rotate image 12 degrees on panel					2.6
GND Return Vias (GRVs)	within 30 mils of signal layer transition (see DesCon 2022)					Figure 17
Solid GND reference layers	both sides of trace (don't use microstrips)					2.3, 2.6

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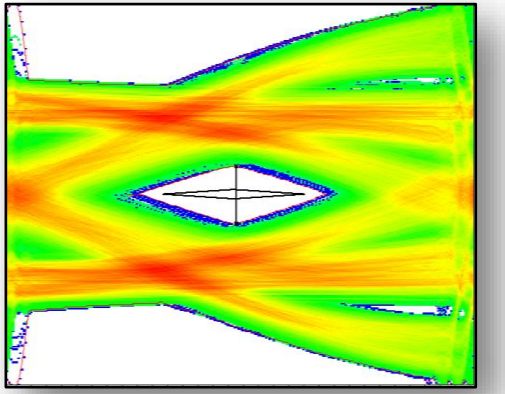


Loss Budgeting: The "Table of Eights"

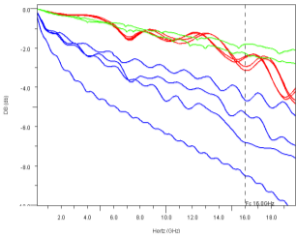
- **Imperative to qualify proposed connection scenarios**

#	System Component	IL (dB)	Notes	MB IC	MB AIC	AIC Cage	SSD Cage	Retimer!	to Rt	from Rt
1	Host/Switch IC	8	8.4 dB, [3] Figure 8-53	8	8	8	8	8	8	
2	Motherboard Route	8	~5" of trace, plus 2 vias	16	16	8	8	16	16	
3	1 Meter Cable	8	Includes mated connectors			8		8		8
4	0.5 Meter Cable	4	Includes mated connectors				4			
5	Adaptor PCB	4	Route conn to SSD/AIC slot			4	8	8		8
6	Non-Root IC	4	4.2 dB, [5] Figure 8-57	4					4	4
7	Add-in Card (AIC)/SSD	8	9.5 dB, [6] section 4.7.11		8	8	8	8		8
			IL Budget Totals (dB):	28	32	36	36	**48**	28	28

- **36 dB is max, and even simplest connection is 28 dB**
- **Scenario over budget? Use retimer to partition path**

Summing works because IL is ~linear

Gen5 PCB IL Challenges & Solutions



Our system context:

- Managing 500+ Gen5 diff-pairs
- Wide array of 30+ dB connection scenarios
- Dozens of 40-67 GHz VNA measurements across numerous PCBs and Cables

Observations:

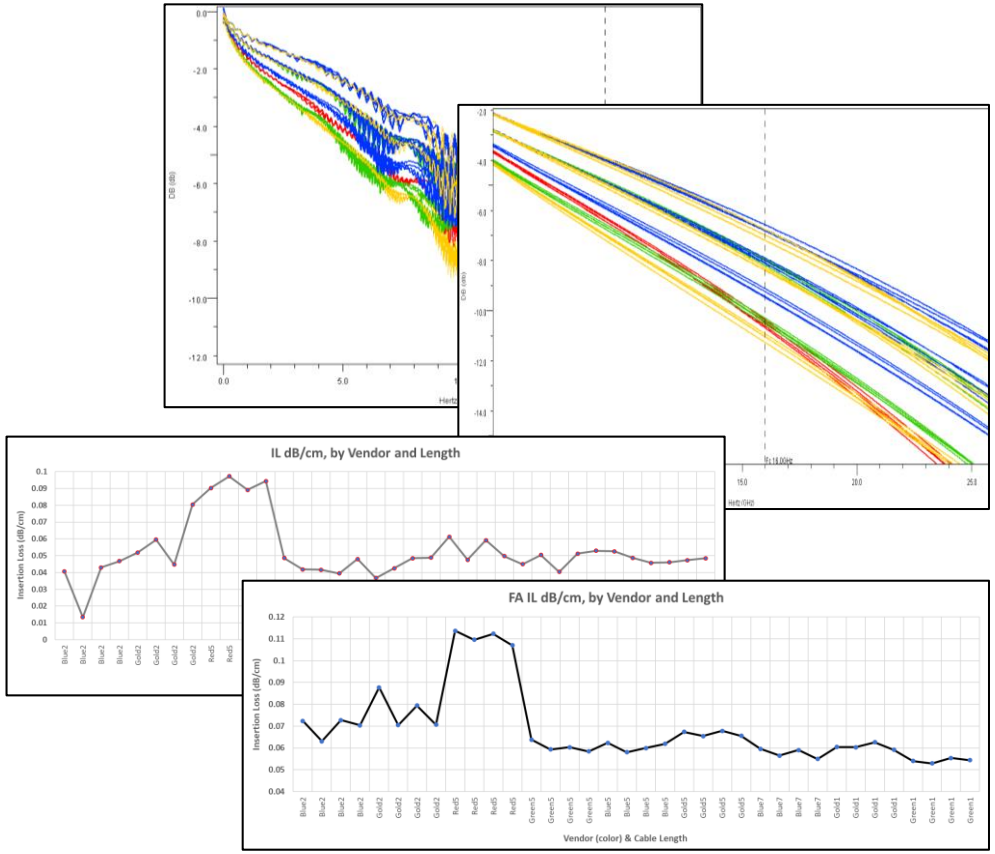
- Measured IL data always higher than plan
- Difficult to achieve less than 1.5 dB/inch
- Problems with simulation, measurement, roughness. Microstrip particularly bad
- Can't solve IL problems with materials

Succeeding with Gen5:

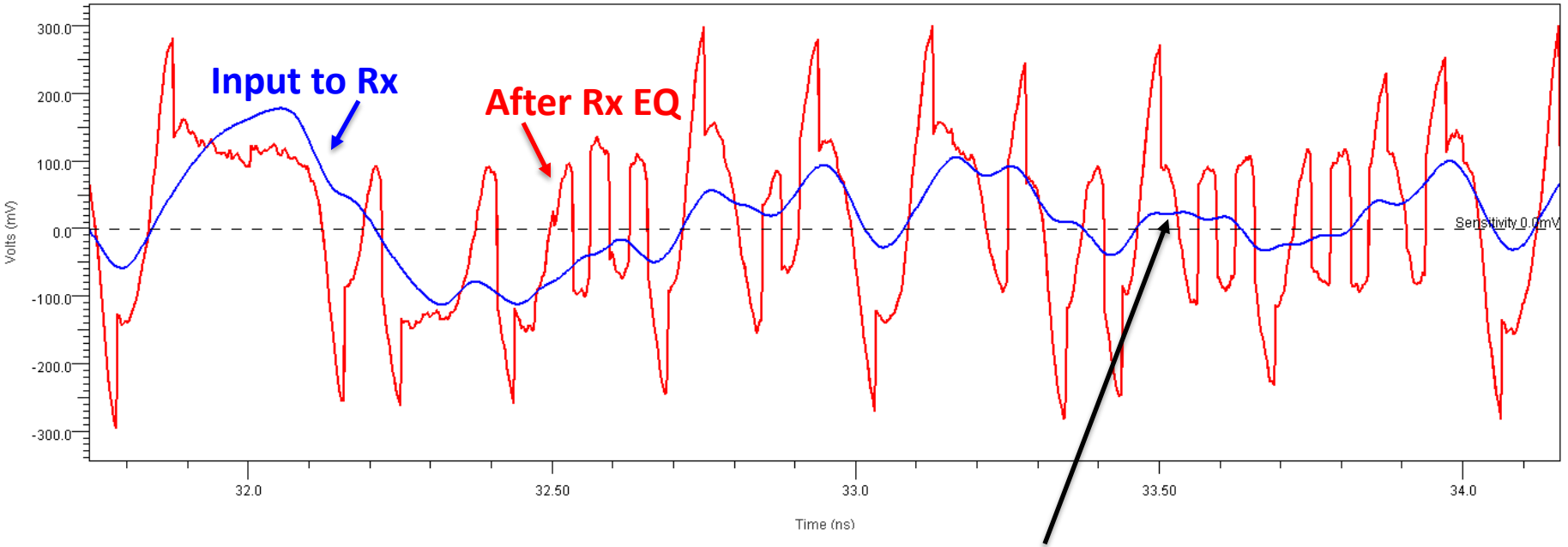
- Keep routes short
- Switch to cables for length
- Avoid microstrip routes (IL 2-3x high)
- Trace width 6+ mils when possible
- Specify and use HVLP2 copper or better
- 0.002 < Df < 0.004 at 16 GHz
- Simulate with correlated table-driven models
- Plan for routed IL of 1.2 to 1.5 dB/inch
- Measure, measure, and then measure again

Cables to the Rescue

- **Measured dozens of MCIO cables across 4 vendors**
- **Data extracted/compared using two algorithms**
- **Good news: Measured IL 10x less than PCB routes**
  - 0.15 dB/in from 3 of 4 vendors
  - 4th vendor's IL is 2x
- **Use cables to achieve length / modularity**
  - But qualify cable vendor's IL!



Gen 5 EQ is Impressive



- EQ perceives slightest change in slope as logic change
- As such, reflections caused by discontinuities must be removed

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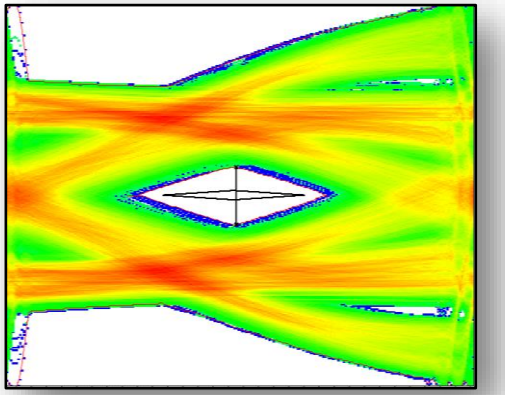
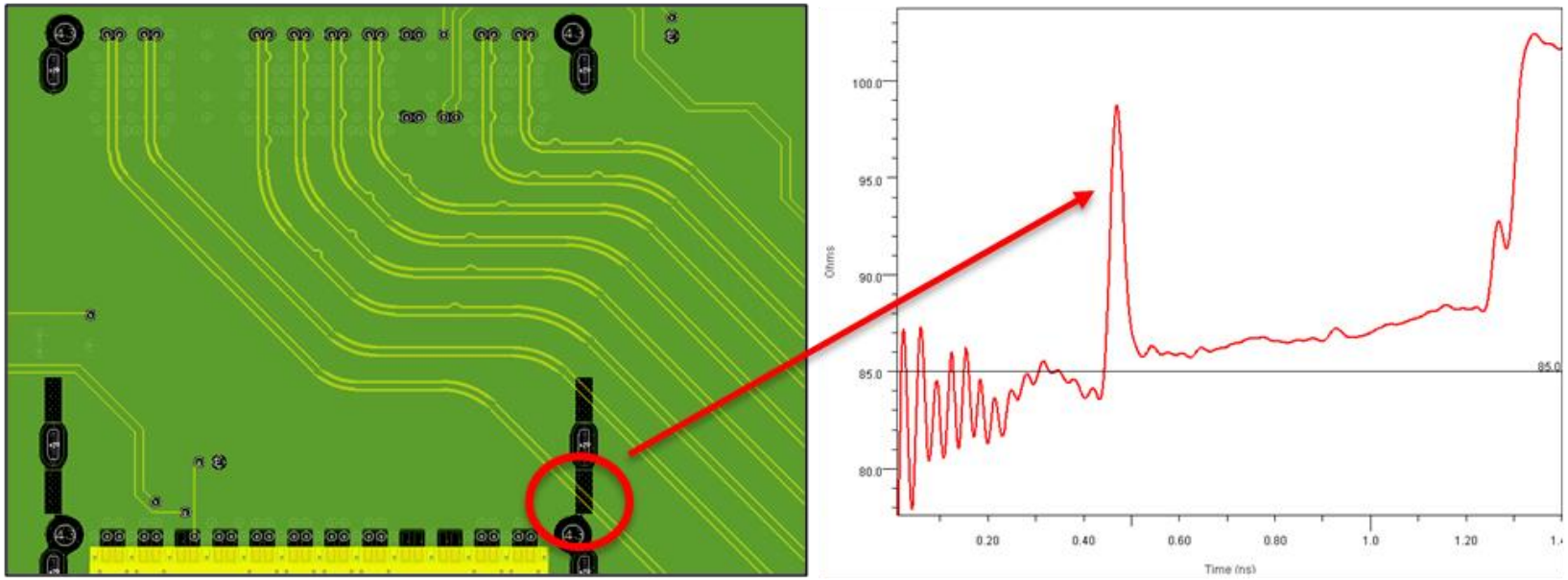


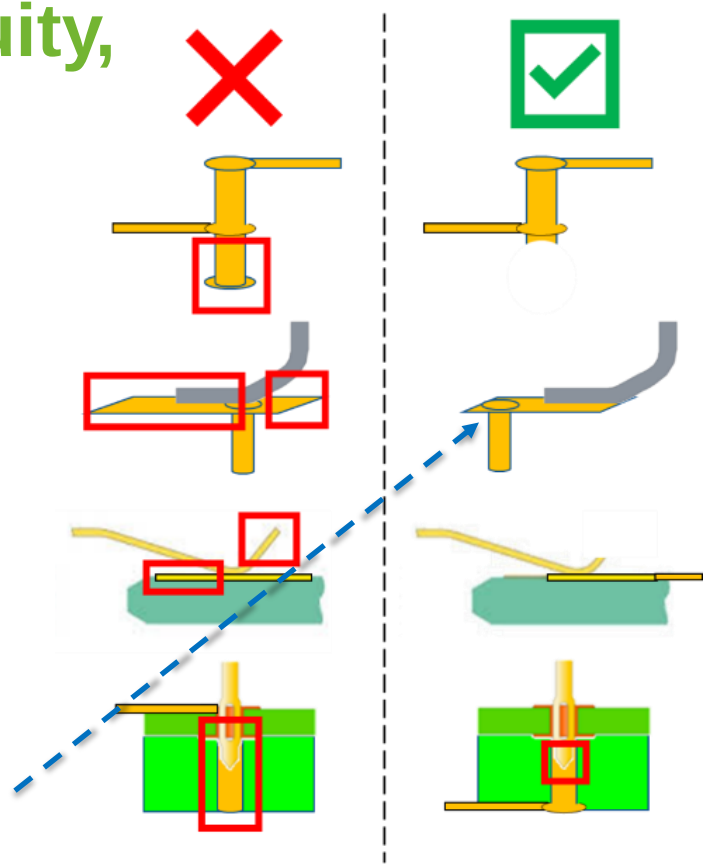
Yes, Everything



- **15 Ohm / 15 ps discontinuity due to small void in GND plane (one side)**

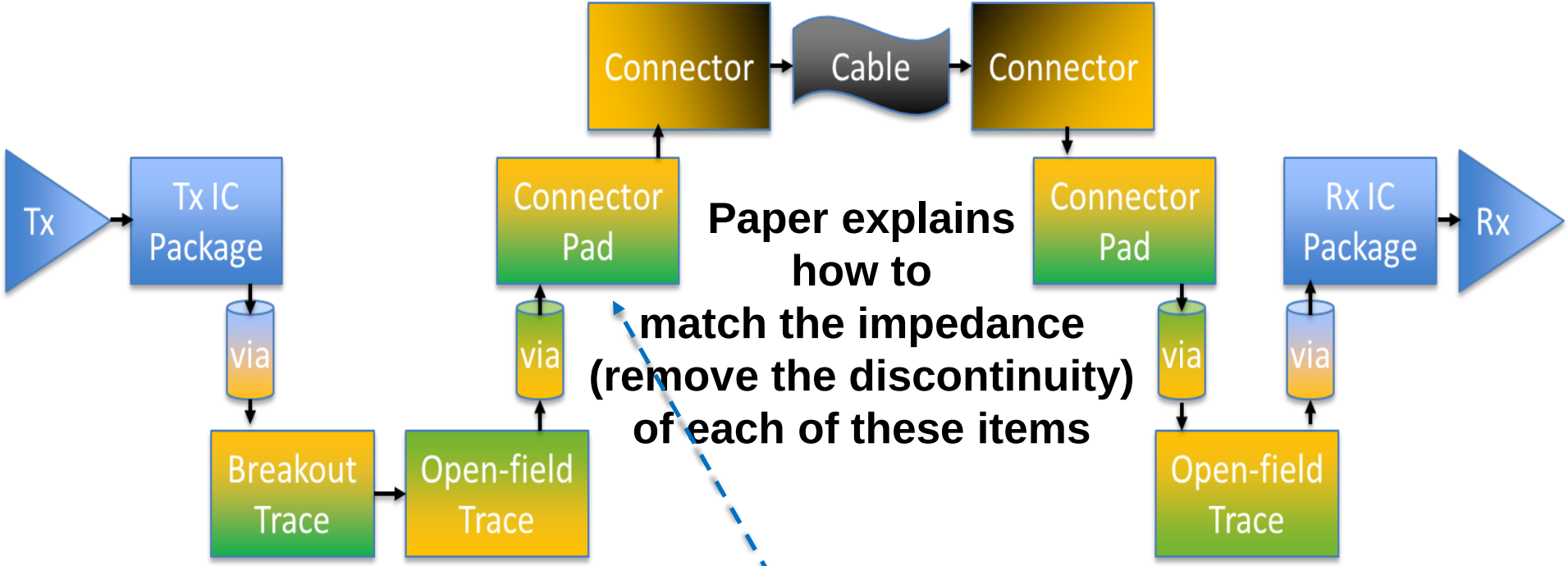
Why Everything is a Discontinuity, and Stubs are Everywhere

- **Relevant Feature Size (RFS):**
  = 0.6*UI(ps) mils ~= 18 mils
  - Pads, vias, etc.
- **Max stub length:**
  = 0.3/Gbps mils ~= 9 mils
  - Per-layer back-drilling
- **What, that's a stub?**
  - Use SI-clean connectors



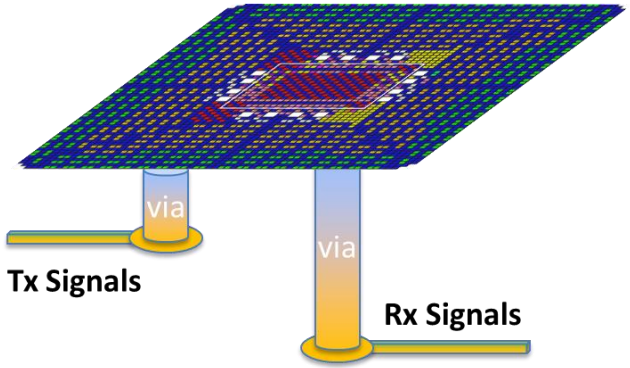
Signals must route into connector pads at the end opposite the connector solder leg exit

Discontinuities in a Gen5 Signal Path



Strategies to Reduce Discontinuities

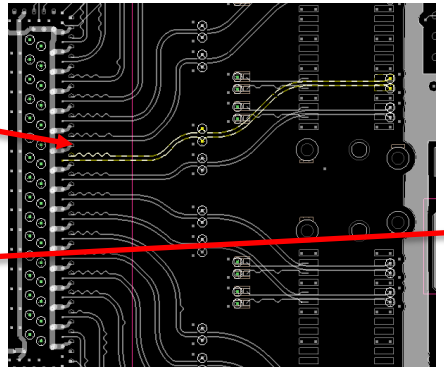
- **Tx at BGA edge with short ViP**
- **Identify/remove p/n skews**
  - In packages, connectors, cables
- **Match vias to trace impedance**
- **Match connector pad impedances**
  - Effective to use 2.5D solver and partial voids
- **Minimize pad sizes**
- **Spread glass with 12º panel rotation**
- **Compensate and/or ~match inflexible impedances**

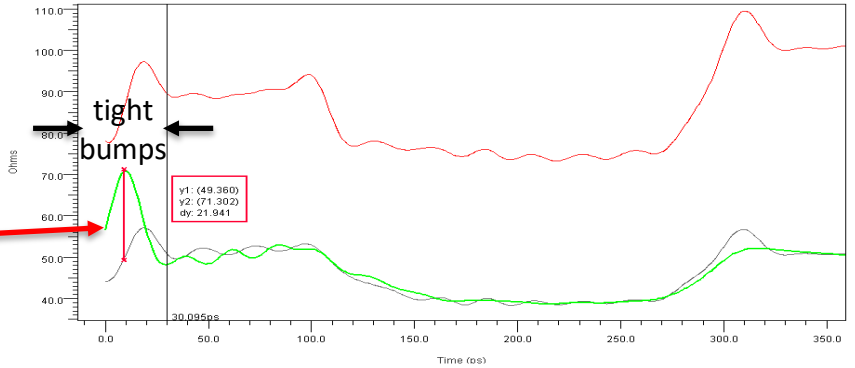


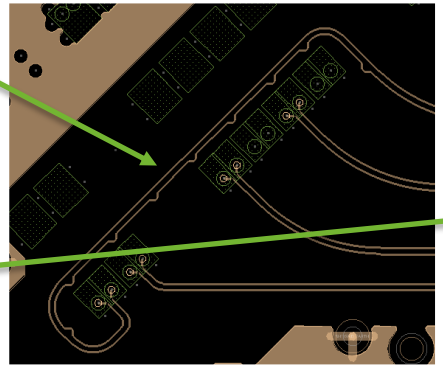
Measure structures to learn and adjust

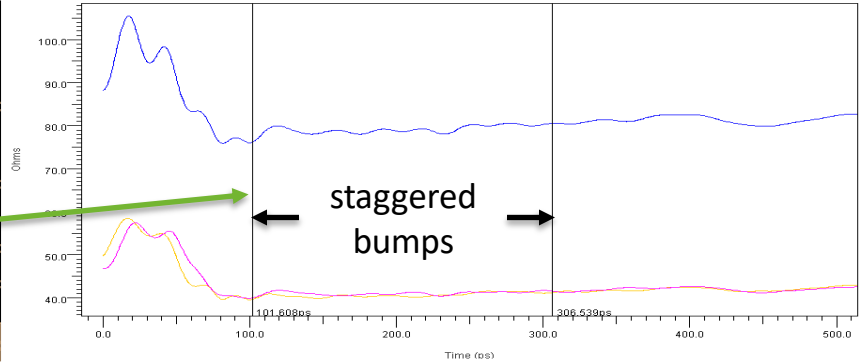
Open Field Routes – Length Match Technique

- **Do not use tight repetitive serpentines**
  - 22 Ohm SE p/n miss-match
- **Stagger bumps irregularly**
- **Length match bumps <= RFS**
- **More bumps, yet less variation**









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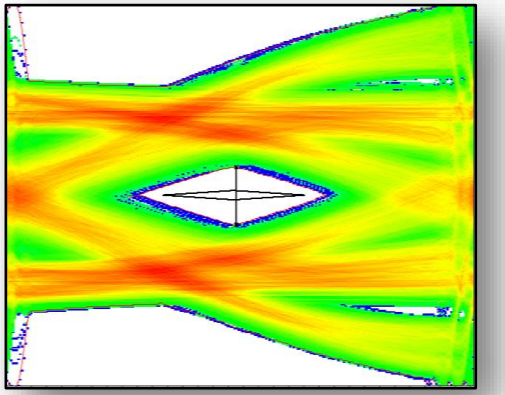
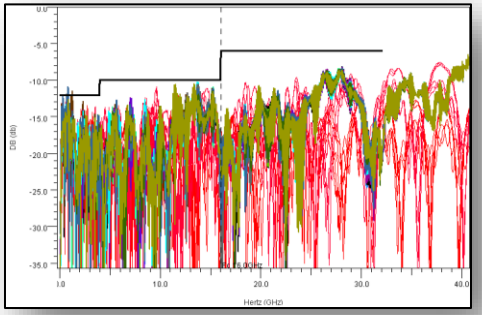
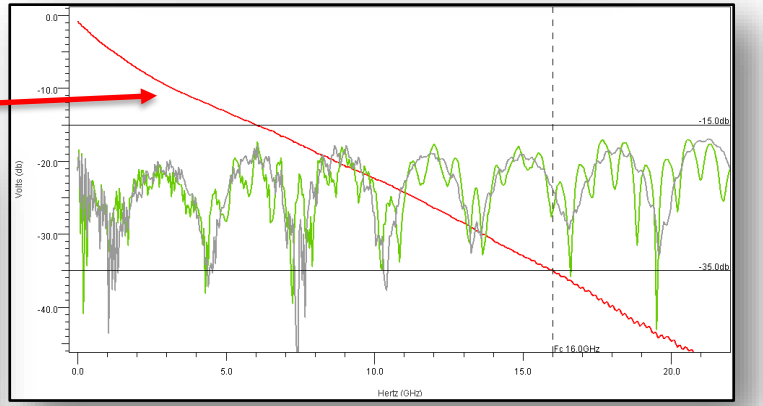
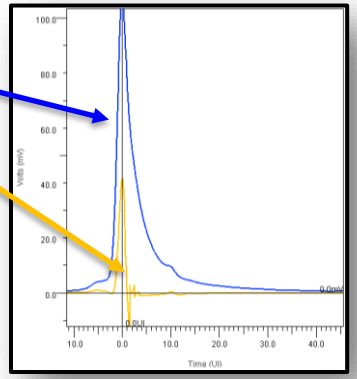


Passive Analysis

- **Min paths for RL, max paths for IL**
- **Min path: non-root IC to connector**
- **Max paths: so many in Gen5**
  - Our paths averaged 31 dB, stdev 6 dB
  - Linear IL, dampens RL
  - ISI to 10 UI pre, 40 UI post
  - Can EQ handle this?

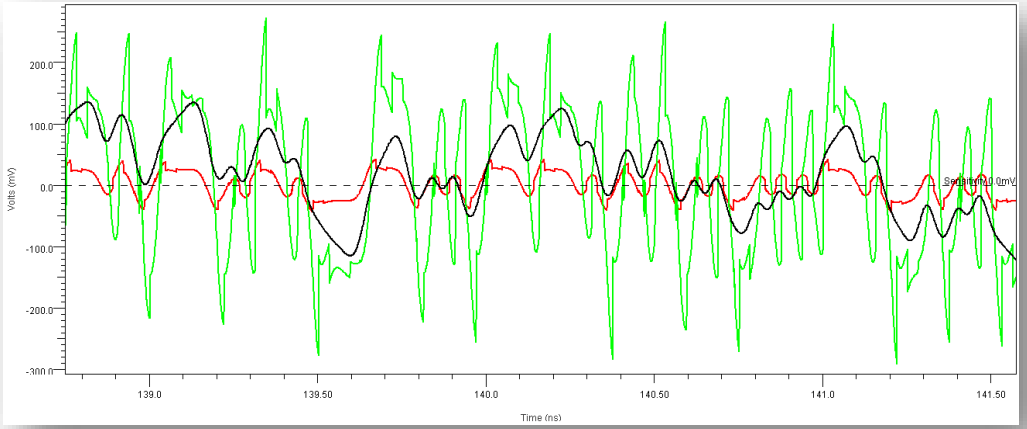


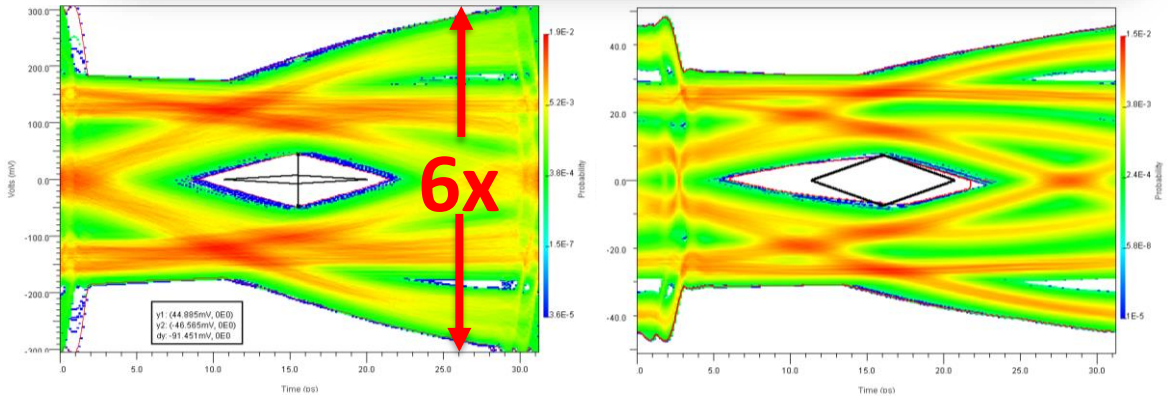




Active Analysis

- **PCIe's primary metric**
- **35 dB channel**
  - **Rx input** applied to:
  - Spec Rx EQ, our EQ
- **Spec eye ~passes**
- **Actual component eye is 6x better**
  - Understand your EQ



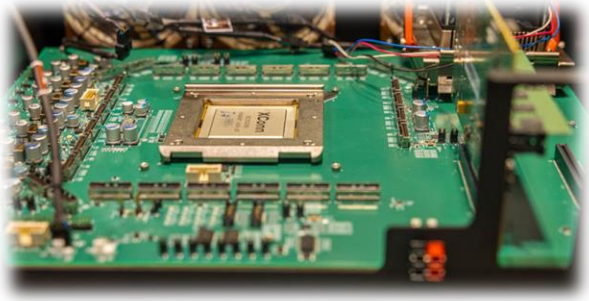


System Component Design Considerations

- **Host/Root IC**
  - Minimize package IL and p/n skews, SerDes should exceed spec's min EQ
- **Motherboard Design**
  - **Shorten routes**, follow our trace guidance, use cables to fan out
- **Add-in Cards**
  - Implement a minimum IL to mitigate connector discontinuities
- **Cables**
  - Work with vendors to confirm cable IL is near 0.15 dB/inch
- **Retimers**
  - Use sparingly, after IL budgets and other options are examined and exhausted

Get IP and chip vendors involved at design start

Lessons from Hardware Bringup



- **Practices shared thus far are imperative to get to the bench**
  - Majority of links worked well – you don't want SI issues post-hardware
- **What we thought would be hard was easy, and vice versa**
- **Good news:**
  - 3rd party AICs work well
  - Protocol Analyzer (kind of)

Bad news:

  - Host connection, BIOS
  - Retimers, and with CXL
- **Do your SI up-front, triple check it, then look elsewhere for problems**
  - Resist the urge to think of SI as "black magic" and the cause of issues

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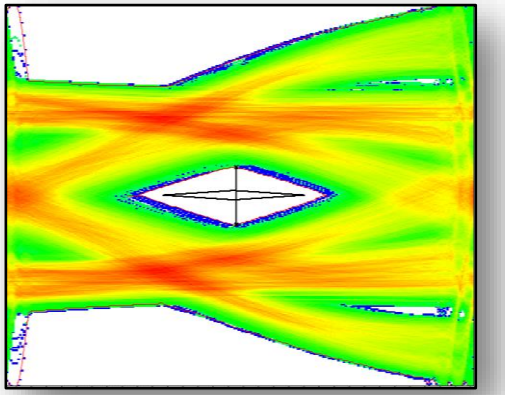

Summary & Conclusions

- **Gen5's 16 GHz significantly changes PCIe implementation**
  - Imperative (once again) to budget, simulate, and measure to manage IL
  - 1" of PCB trace ~= 10" of cable
- **Nearly every feature on a PCB can be a discontinuity**
  - Need to match impedances of increasingly smaller features
- **Measurement of passives is important**
  - Be prepared for surprises/iterations in simulate<->measure correlation
- **Optimal EQ is key, system may not negotiate this automatically**
  - Quantify how component's EQ exceeds PCIe assumptions and manipulate manually

PCIe Gen5 system implementation becomes robust with proper SI

MORE INFORMATION

- Much more in Paper
- SiGuys.com, Xconn-Tech.com
- References at right
- telian@siguys.com

  kevin.rowett@xconn-tech.com

References

1. Donald Telian, "Signal Integrity, In Practice – A Practical Handbook for Hardware, SI, FPGA & Layout Engineers" – book published in 2022 and available at Amazon.
2. Compute Express Link ™ webinars, particularly "CXL 2.0 Specification: Memory Pooling" Airing Date: March 23, 2021
3. EDIcon 2022 on-line conference session presented by Donald Telian "Signal Integrity Cheat Sheet – Data-Rate Driven Design Decisions" recorded October 5 2022.
4. Telian D., Camerlo S., et. al. "Moving Higher Data Rate Serial Links into Production – Issues & Solutions" DesignCon 2014 technical paper.
5. PCI-SIG, "PCI Express® Base Specification" Revision 5.0, Version 1.0, 22 May 2019.
6. PCI-SIG, "PCI Express Card Electromechanical Specification" Revision 5.0, Version 1.0, June 9, 2021.
7. Telian D., "7 Challenging SI/PI Problems That Have NO Existing Solution" presented at SPI 2016 Italy.
8. Beyene W., Hahm YC., et. al., "Lessons learned : How to Make Predictable PCB Interconnects for Data Rates of 50 Gbps and Beyond" published at Signal Integrity Journal, October 2017
9. Isola presentation "PCB Material Selection for High-speed Digital Designs" published at Microwave Journal 26 February 2014
10. Telian D. (2022 July 12). "7 steps to Successful Serial Links" Signal Integrity Journal RSS
11. Telian D. (2022 April 1). 'Which Discontinuities are Small Enough to Ignore?' Signal Integrity Journal RSS
12. Telian D. (2007). "Adapting Signal Integrity Tools and Techniques for 6 Gbps and Beyond" [slides 1-33]. SiGuys, CDNLive! 2007.
13. Telian D. (2022 June 2). 'Understanding Via Impedance.' Signal Integrity Journal RSS.
14. Steinberger M., Telian D., et. al. "Proper Ground Return Via Placement for 40+ Gbps Signaling" DesignCon 2022 best paper
15. Steinberger M., Telian D., et. al. "Managing Differential Via Crosstalk and Ground Via Placement for 40+ Gbps Signaling" DesignCon 2023 technical paper
16. Telian D. (2022 November 1). "Managing PCB Crosstalk" Signal Integrity Journal RSS.
17. Telian D., Steinberger M., Katz B., "New SI Techniques for Large System Performance Tuning" DesignCon 2016 technical paper

Thank you!

QUESTIONS?

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