A SerDes Balancing Act: Co-Optimizing Tx and Rx Equalization Settings to Maximize Margin

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Poll Results: Analyzing Serial Links

How are you analyzing serial links today? (Pick all that apply)

Vendors / consultants do it for us	9%
Measure channels and eyes in the lab	69%
Analyze channel models for mask compliance	52%
AMI-based simulations	53%
Analyze channel TDR/TDT/Pulse responses	51%
In-house tools and processes	36%



AGENDA

- Introduction to Co-Optimization
- Co-Optimization Examples
- How to Co-Optimize
- Summary

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Why Co-Optimization?



time

length

ISI

Rx

Loss

Тх

- Increasing #links, data rates, and protocols
- EQ complexity / importance
 - PAM4, decreasing margin
 - Must balance Tx with Rx
- "Auto-Negotiation/Training" often isn't
 - Good goal, will take time to achieve
- Problems not only loss
 - Traditional EQ targets loss
- Optimal settings: SW-only fix
 - Rescues failing links









• Eye diagram derived from pulse response through recursive convolution



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Unequalized Pulse Response (a.k.a. the Channel Response)

(Relatively) short rise time



• Requires accurate Tx/Rx analog models to correctly predict ringing due to reflections

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The ISI Pulse Response



- Voltage and time scales show ISI contributions
- Useful in evaluating EQ & predicting eye opening

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Equalizing Pulse Responses



- Long channels: pre-cursor & tail ISI is usually the challenge
- Short channels: ringing is usually the challenge





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Poll Results: Analysis Methods

Which of these methods do you currently use to optimize Tx & Rx settings? (Pick all that apply)

Minimize Tx equalization to save cursor amplitude	28%
Evaluate tradeoffs between Tx taps and CTLE	44%
Use TX taps / RX CTLE to bring tail within DFE range	32%
Trade off eye height & width to optimize BER	53%
None of the above	15%
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AGENDA

- Introduction to Co-Optimization
 - **Co-Optimization Examples**
 - Industry Case Study
 - S-Parameter
 - Circuit-based
 - -PAM4
- How to Co-Optimize
- Summary

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Balancing Act

Industry Paper

- Co-Optimization case study
 - 60%+ performance gains
 - Allowed 25% longer links
 - Compared with best-known EQ
 - Removed dozens of components
- Detail on Co-Optimization concepts and techniques
 - Hula-hoop algorithm
 - Equations for reducing ISI
 - System-level Tx/Rx EQ tradeoffs



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This presentation illustrates This presentation illustrates Co-Optimization on a wider array of channels

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Paper: Equations vs Co-Optimization

- Problem:
 - Long/lossy channel
 - 4-tap Tx (1pre, 2post)
 - No Rx EQ



- Hand Calculation (blue)
 - Force zero in all taps
 - 1 hour/tap to solve/iterate
- Co-Optimization (red)
 - Trade amplitude for ISI
 - 15% better eye





Better Result

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- 1 hour, closer result
 - Co-Optimization is 5% wider
- Results:

	Tap-1	Тар0	p0 Tap1 Tap2 Eye		Eye	Time
Hand_Calc	-0.07	0.54	-0.34	0.05	-15%	3 hours
Sweep	-0.08	0.59	-0.33	0.00 -5%		1 hour
Co-Optimize	-0.04	0.61	-0.35	0.00	Best	< 1 sec

- If Rx EQ added
 - complex, less convergence



Faster

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Step 1, Eye Height vs Tx Taps Black=Eve Ht, Red=Tap1, Green=Tap-1, Blue=Tap2

200.0

300.0

00.0

100.0

200.0

-300.0

-400.0

- 600 O

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-200.0

-300.0 🗒

400.0

-500.0

400.

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100.0

80.0

60.0

40.0

20.0

0.0-

100.0

Volts (mV)

Co-Optimization Cockpit

- You can fly this plane
 - Examples that follow will be available as SiSoft QCD Project
- Co-Optimization = SiSoft OptimEye[™] Technology
- All variables adaptable

 UI, EQ (FFE, DFE, CTLE), PCB Parameters, Jitter, Clock Recovery, etc.

Details later in presentation...





S-Parameter Channels



Analysis Setup

- Circuit
 - s4p channels, 10 Gbps



- SerDes EQ
 - 4-taps in Tx FFE and Rx DFE
 - Rx CTLE, 0-15, ~0-15dB boost
- EQ Preset Scenarios
 - 1: Tx taps ~half, CTLE=12
 - 2: Tx taps ~PCIe P7, CTLE=8
 - 3: OptimEye selects Tx / CTLE
 - Rx DFE always "auto"











- 10 Gbps, same EQ options and jitter as S-param channels
- Length: 10" to 42", Lt_cd/bp: 0.015/0.009, ISI & Loss channels
- Permutations: 4 bp_len * 3 rx_len * 2 bp_via * 2 rx_via = 48
- Total Simulations: 48 * 3 EQ options = 144
- Manufacturing tolerances

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Passive Characteristics, 48 Channels



Mix of ISI-Constrained & Loss-Dominated Channels
20 dB Insertion Loss variation at 5 GHz

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Eye Height Results



PAM4

- Co-Optimization • goes center-stage
 - Same OptimEye technology

Complexity

Volts (mV)

- Channels 10"-20" •
- Eye Height vs EQ •
 - PCle P6
 - PCIe_P5
 - OptimEye
- OptimEye ~2x improvement
 - Channel 3 eyes shown



Overall Results

Channel Type	Average Improvement	Standard Deviation	Sample Size	Comparing
ISI	217%	97%	30	OptimEye vs P7
Loss	55%	41%	30	OptimEye vs P7
Industry	166%	42%	7	OptimEye vs P7
PAM4	97%	31%	6	OptimEye vs P5
All	140%	109%	73	OptimEye vs P7/5

- Baseline settings slanted towards loss equalization
 - Which is typical in today's systems
- In general, we expect
 - 100% improvement for ISI-dominated channels
 - 50% improvement for Loss-constrained channels



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Using OptimEye



- "QCD Optimization" attribute on any enabled Tx
- 2 modes Tx & TxRx
- Runtime is longer
 than normal simulation

Channels	Normal (s)	OptimEye™ (s)	x Longer					
20 S-Parameter	38	62	1.6					
48 Circuit-based	94	120	1.3					
running TxRx mode, Statistical Analysis, Quad-core Laptop, Win7								

Answers in seconds instead of weeks



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- Optimization control files let OptimEye predict and verify model settings
- Support for SiSoft models built-in



OptimEye Results

Opt ATX11	-0.225961					0	ria	ino		nd	on	tim	iza	bd			
Opt ATX1.0	0.590481					U	пy	IIId	l d	U IU	υμ	ιΠ	IIZE	JU.			
Opt ATX1.1	0						Sur!										
Opt ATX1.2	-0.183558					Se	ЭШ	ngs	s re	epc	orte	a I	Or	ea	CH 🛛		
Opt ATX1.tx_swing	1																
Opt ARX1.peaking_filter.config	0				I x/Bx model parameter												
Stat ATX1.tap_filter1	-0.225961																
Stat ATX1.tap_filter.0	0-500-44		DU			DV	RI.			80				DC.	DT	DU	
Stat ATX1.tap_filter.1	0	BG	ВН	ы	BJ	BK	BL	BIM	BIN	BO	BP	BQ	BK	BS	BI	BU	BV
Stat ATX1 tap_filter 2	- Stat	Stat ARx.SiSoft	Stat														Opt
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Stat ATV1 normaliza tana	Rx.mod ~	_RX.TX_Tap_ values *	_ Optimizing Rx.tx_ta *	ation	1 Height[0.00	006] (V 👻	009] (V 💌	012] (V 👻	1] (ps) 💌	006] (ps 👻	009] (ps 👻	012] (ps *	Opt ATx. 👻	Opt ATx. 👻	Opt ATx.1 💌	Opt ATx.2 💌	fig 💌
Stat ATX1.normalize_taps	Off	1	ι ο	NRZ	0.532533	0.474033	0.442577	0.421179	74.6094	64.0625	59.7656	57.0313	-0.0476998	0.948184	-0.00411652	0	0
Stat ATX1.number_tx_tap	4 Off	1		NRZ	0.460423	0.390103	0.354113	0.331334	73.8281	62.1094	57.4219	53.9063	-0.0818942	0.915814	-0.00229197	-0 12719	0
Stat ATX1.number precursor tap	1 Off	1	 	NRZ	0.499445	0.4410333	0.415163	0.396053	74.2187	64.0625	59.375	56.25	-0.0640821	0.933004	-5.42101E-20	-0.00291357	0
Stat ATX1 tap max	Off	1		NRZ	0.434893	0.383424	0.355172	0.335223	74.2187	62.8906	58.5937	55.8594	-0.0819756	0.917761	-0.000263023	-4.33681E-19	0
Stat ATV1 tan min	Off	1	 	NRZ	0.46732	0.424751	0.401923	0.385181	73.8281	63.2813	59.375	56.25	-0.0615739	0.936741	0.00168538	0.07302L-15	0
Stat ATA 1.tap_mm	Off	1		NRZ	0.412755	0.361336	0.332669	0.312507	73.4375	62.5	57.8125	54.2969	-0.0976001	0.891354	-8.67362E-19	0.0110462	0
Stat ATX1.tap_step	Off	1) NRZ	0.263167	0.216189	0.19284	0.1/6631 0.133	66.7969	53,9063	51.5625	48.4375	-0.144352	0.849163	-0.00648496	0	0
Stat ARX1.AGC.Mode	Off	1	L C	NRZ	0.274246	0.228107	0.204805	0.188174	69.9219	58.5937	53.5156	49.6094	-0.146933	0.848469	-0.00459776	1.73472E-18	0
Stat ARX1.AGC.Level	Off	1	L C	NRZ NRZ	0.247413	0.202678	0.179685	0.163731 0.0712205	67.5781 55.8594	55.8594	50 40.625	46.0938 37.5	-0.166084	0.827227	-0.00668917	0 -0.226899	0
Stat ARX1 peaking filter config	Off	1	L O	NRZ	0.0960605	0.0754149	0.0646627	0.0570573	57.8125	43.3594	38.6719	35.5469	-0.166734	0.62837	0	-0.204896	4
Stat ADV1 peaking filter mode	f Off	1		NRZ NRZ	0.129846	0.1138/3	0.1054/3	0.0995056	70.3125 60.9375	47.2656	54.2969 41.7969	38.6719	-0.132532	0.862265	0	-0.00520367 -0.163721	5
	Off	1	L C	NRZ	0.397121	0.34599	0.318113	0.298606	74.6094	62.8906	58.5938	55.4688	-0.0640421	0.895245	0	-0.0407134	0
Stat ARX1.peaking_filter.use_new_pole_zero_defaults	Off	1		NRZ	0.27045	0.233186	0.212996	0.199847	73.4375	61.3281	55.0781	51.5625	-0.0861227	0.910919	-0.00295848	0 100893	5
Stat ARX1.peaking_filter.scale_by_design_data_rate	Voff	1	L C	NRZ	0.301033	0.263918	0.24396	0.230696	75.3906	65.2344	60.5469	57.4219	-0.0784638	0.919178	-0.00235777	-0.100855	4
Stat ARX1.peaking_filter.pole_zero_data_rate	6 Off	1		NRZ	0.320367	0.270395	0.243274	0.22422	71.0937	59.7656	55.4687	51.9531	-0.120524	0.874361	-0.00511474	0	0
Stat ARX1.peaking_filter.design_data_rate	off	1		NRZ	0.340023	0.294948	0.269354	0.25107	70.7031	59.7656	55.0781	51.9531	-0.108547	0.88707	-0.00438279	0	0
Stat ARX1.dfe.number_rx_tap	4												1.1				
Stat ARX1.dfe.taps.1	-0.068782			٠	Ρ	ost	:-Dr	'OC	ess	50	utp	ut	to				
Stat ARX1.dfe.taps.2	0.02220)4				-											
Stat ARX1.dfe.taps.3	0.01184	4				C	ont	IUU	re	VO	ur	ent	ire	SV	ster	n	
Stat ARX1.dfe.taps.4	0.00276	64						.90		, .				-)			
Stat ARX1.dfe.mode	auto																



Optimize Routed & Built Systems

- Use OptimEye™
 Pre- or Post-Route
 - Single-board, or System of PCBs

Design

Debug

- Actual routes refine
 design space
- Import / analyze failing channels
- Derive optimal settings
- Software change only



Post-Layout Verification

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Pre-Layout Analysis

Poll Results: SerDes Settings

How long does it take your company to determine SerDes settings during system bring-up? (Pick one)

Not long; we use defaults	11.2%
Not long; the SerDes vendor tells us	6.7%
Days	27.0%
Weeks	28.1%
Months	22.5%
It's too painful to think about	4.5%

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Summary

- Rx eye height should be optimized for the point where the recovered clock samples the data
- "Blind sweeps" consume time and brain cycles
- OptimEye is 3rd generation SiSoft technology
 - Maximizes eye height by co-optimizing Tx/RX settings
 - Does <u>not</u> require changes to vendor AMI models
- Per-channel optimization is now practical at the full system level

See How OptimEye Works for You!

Statistical Eye Diagram

3 4E-2

1.1E-2

1.2E-3

1 4E-44

35

80.0

OptimEye(TN

20.0

40.0 60.0

Time (ns)

 Follow link to "request more information" at the end of this webinar

 Or visit: <u>www.sisoft.com/optimeye</u>

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QUESTIONS ?

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THANK YOU

