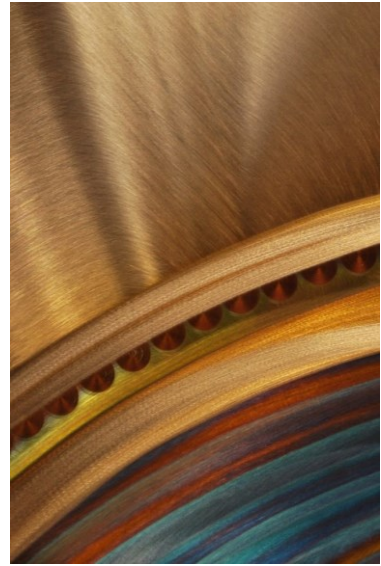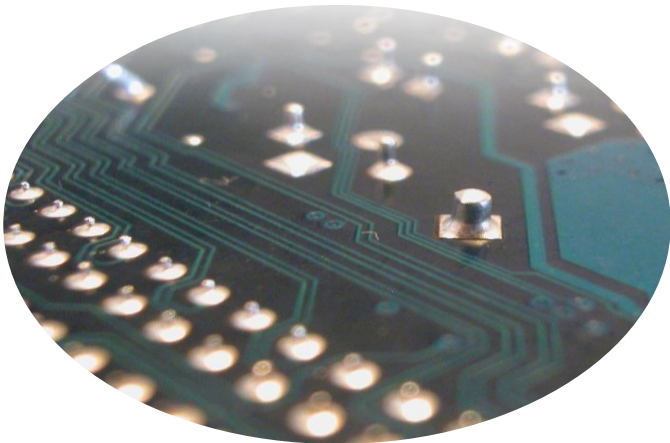# S + I = $

How to Succeed at a Career in Signal Integrity

Donald Telian

telian@siguys.com

SI GUYS

Rev 1.0

S + I = $
How to Succeed at a Career in Signal Integrity

What is the Signal Integrity Engineer's job description? We make electronics work faster. But how do we do that? Interestingly, after doubling data rates more than a dozen times, Donald Telian reveals the answer is always changing. As such, to succeed in Signal Integrity you must learn to creatively adapt – daily. And you must do this both technically and organizationally. This unique talk blends data-rate-dependent SI design guidance with the three keys to succeeding at a career in signal integrity, revealing the answers are less intuitive and more fun than you thought.
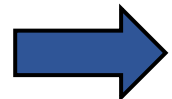
Donald Telian has worked in Signal Integrity for more than 40 years, uniquely positioning him to exposit on a career in SI. He has invented various SI concepts, tools, and quirks engineers use everyday to get their jobs done. He is an SI Coach, the owner of SiGuys.com, and the author of "Signal Integrity, In Practice" – a new book that cuts through the noise to explain how to "do" SI when confronted with the data rates of today.
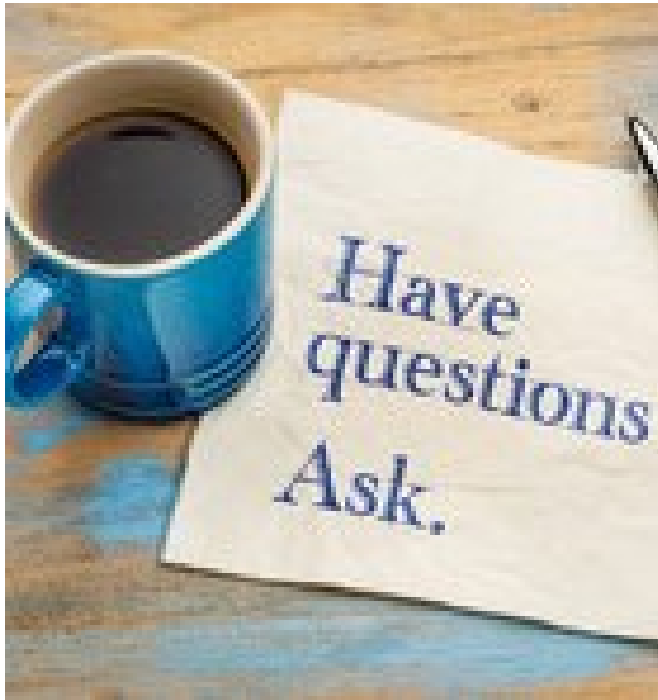
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SI

Signal Integrity, In Practice

AGENDA

- Who Are We?
- How to Go Faster: Technologically
- How to Go Faster: Organizationally
- Summary
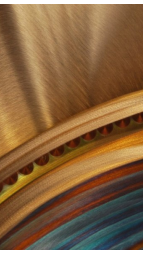
$S + I = \$$
a Career in SI

...how to succeed

Signal Integrity, In Practice

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What do you do for a living?

I'm an Engineer

What kind of engineer?

I design electronics

Signal Integrity, In Practice

What does that mean?

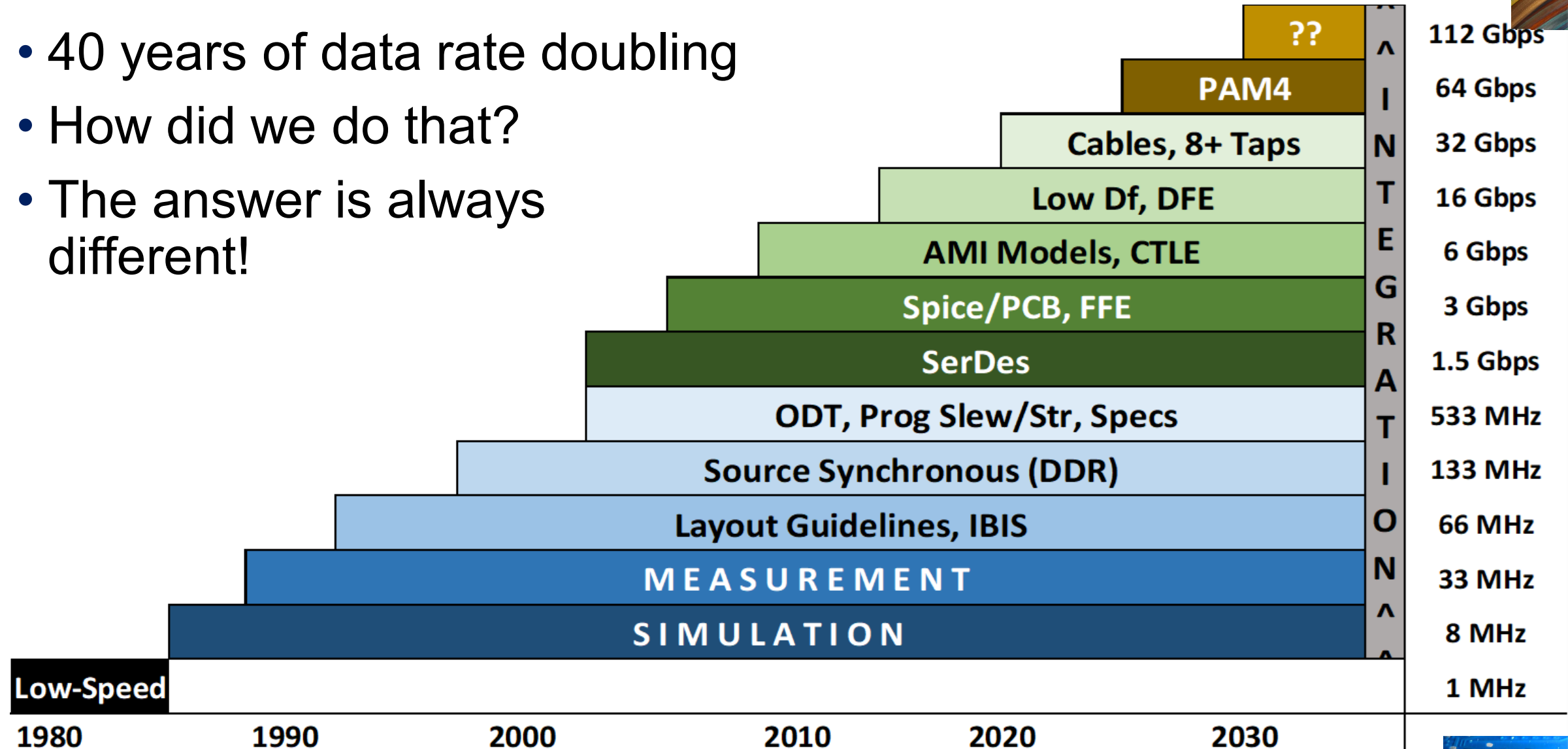*Have you ever owned an electronic device you wanted to work faster?*
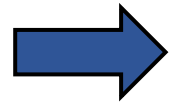
Yes, of course!

I make electronics work faster

Making Things Go Faster

- 40 years of data rate doubling
- How did we do that?
- The answer is always different!

Stack (bottom to top)	Data Rate
??	112 Gbps
PAM4	64 Gbps
Cables, 8+ Taps	32 Gbps
Low Df, DFE	16 Gbps
AMI Models, CTLE	6 Gbps
Spice/PCB, FFE	3 Gbps
SerDes	1.5 Gbps
ODT, Prog Slew/Str, Specs	533 MHz
Source Synchronous (DDR)	133 MHz
Layout Guidelines, IBIS	66 MHz
MEASUREMENT	33 MHz
SIMULATION	8 MHz
Low-Speed	1 MHz

MAINTENANCE ^ INTEGRATION ^

1980   1990   2000   2010   2020   2030

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AGENDA

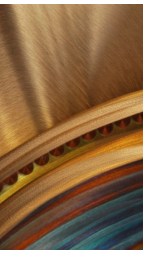- Who Are We?

→ - How to Go Faster: Technologically
  - Data Rate Cheat Sheet
    - Feature Size
    - Stubs
    - Loss

- How to Go Faster: Organizationally

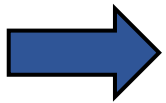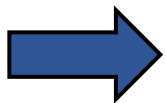- Summary

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Signal Integrity Cheat Sheet

Feature	4 Gbps	8 Gbps	16 Gbps	32 Gbps	Unit	SIiP Section
Industry/PCIe terminology	Gen2	Gen3	Gen4	Gen5		
Fundamental Frequency	2	4	8	16	GHz	
Relevant Feature Size	160	80	40	20	mils	4.1, 2.1, 4.x
what's that?	traces	vias	conn pads	everything		4.2, 4.3, 4.4
Max Stub	64	32	16	8	mils	2.5, 1.3.3
backdrills	none?	seq-lam	2 layers	per-layer		
P/N Matching, static	10	5	2	1	mils	2.3
P/N Matching, dynamic			10 in 1.5"	5 in 1"	mils	2.3, 2.4
Route Style	45°	45°	curved	curved		2.4
Diff-pair Spacing (XY/Z, min)	25	25	25	30	mils	5.3
Insertion Loss (max)	16	22	28	36	dB	2.2, 3.5
Min EQ: Tx_FFE/Rx_DFE taps, CTLE	1 / 0	2 / 1, C	2 / 2, C	2 / 3, C	#taps	3.3, 3.4, 2.7
Length match method	serpentines		irregular spaced bumps			2.4
Fiberglass weave	spread glass and rotate image 12 degrees on panel					2.6
GND Return Vias (GRVs)	within 30 mils of signal layer transition (see DesCon 2022)					Figure 17
Solid GND reference layers	both sides of trace (don't use microstrips)					2.3, 2.6

that's my book →

Relevant Feature Size (RFS)

Figure 2. Relevant Feature Size Versus Data Rate RoT

- What is the smallest structure a signal will "see" at a given data rate
  - As such, need to solve/match impedance to prevent reflection (noise)

- RFS = 0.6 * UI mils (UI in ps)
  - Based on edge-rate/round-trip

- Details at [Signal Integrity Journal]

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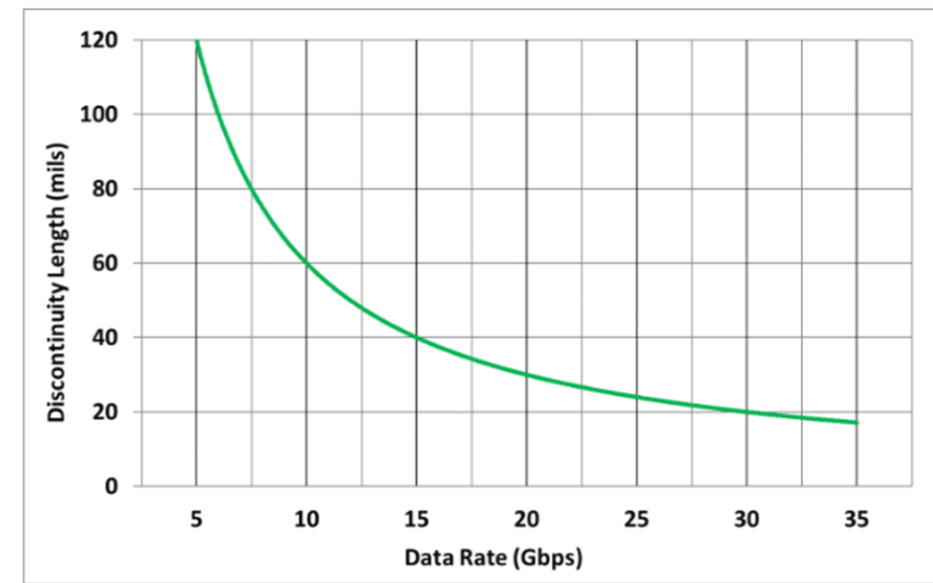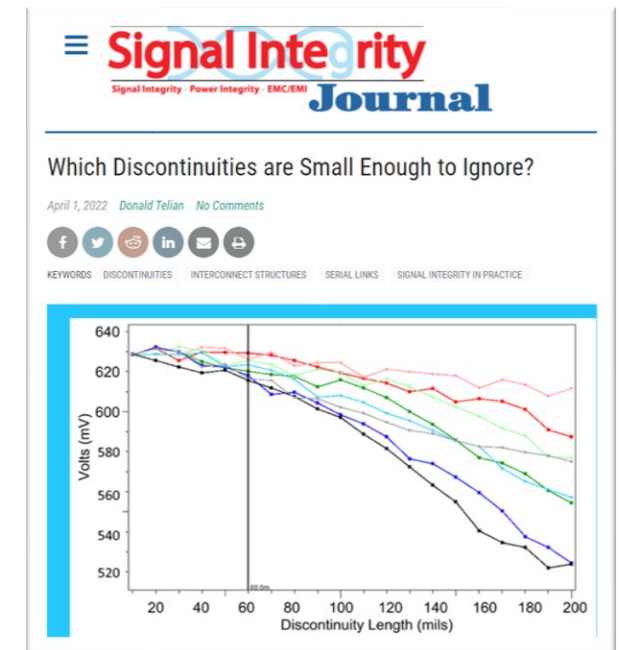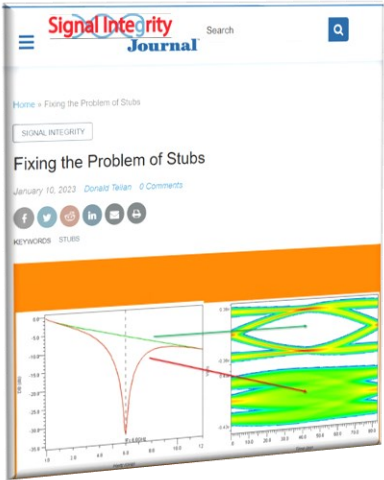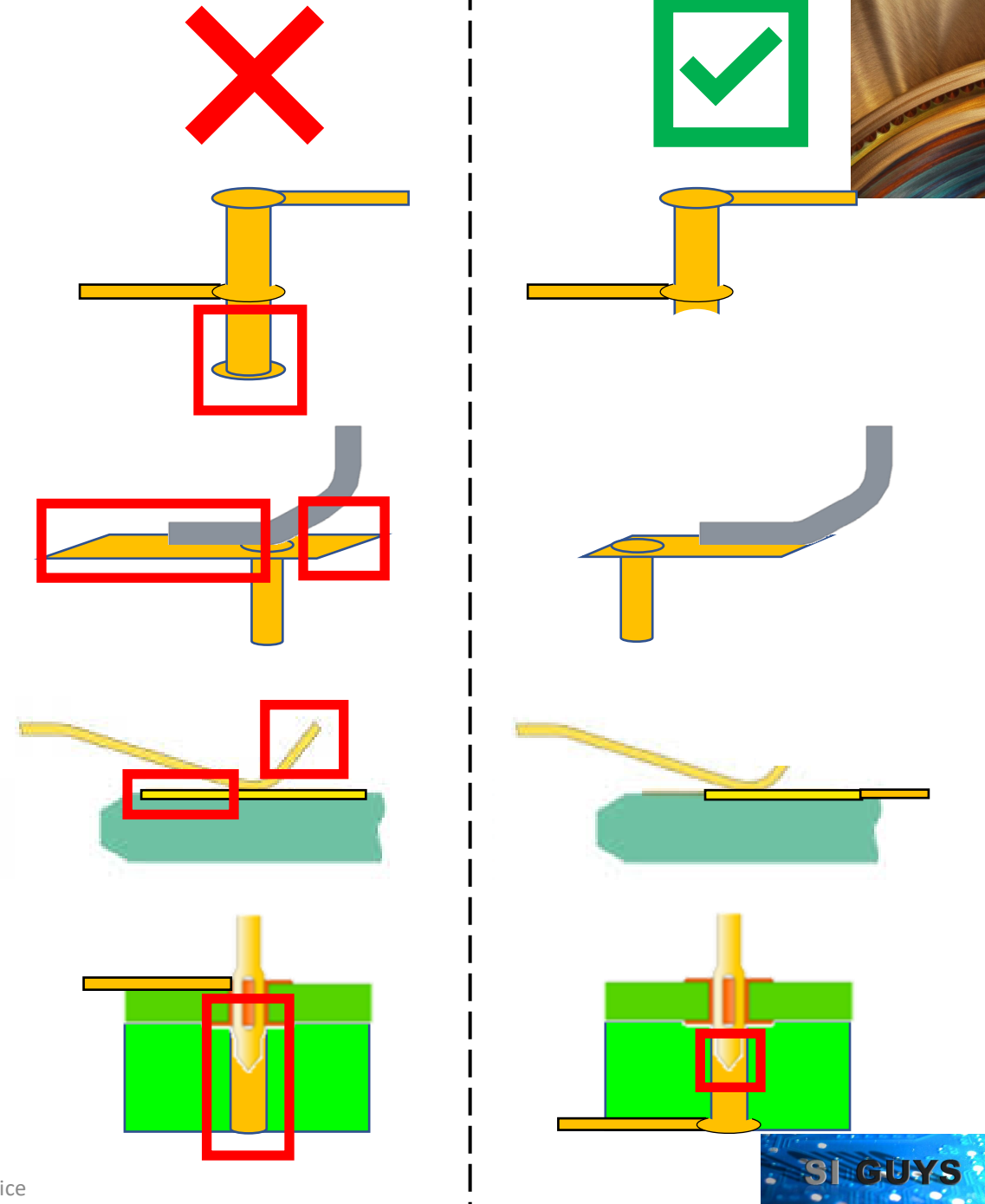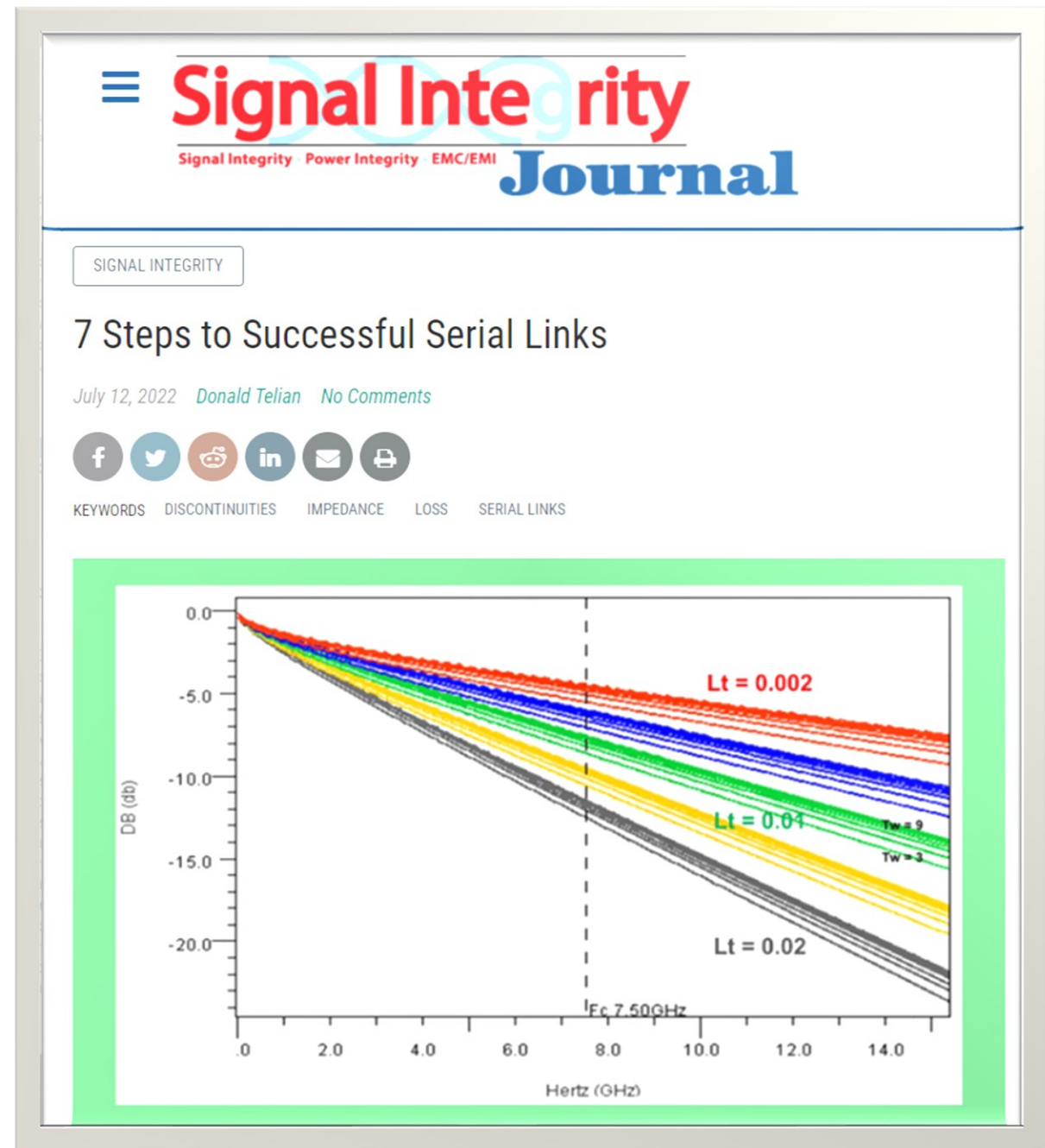
What?! That's a Stub??

- **Backdrill vias**
  - Gen3/4 failures

- **Remove stubs at solder pads**
  - Gen5 failures

- **Minimize stubs at edge fingers**
  - Should be handled by standard

- **Press-fit connectors are messy**
  - No longer used at higher speeds

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Handling Loss

- Can vary 4x in 12" of trace
  - Depending on construction (Lt/Df and Twidth, primarily)
- For many Gens, we've reduced loss by lowering Lt
  - But this is changing!
- Step 2 in the "7 Steps" series

- EQ mainly handles loss

Signal Integrity, In Practice

AGENDA

- Who Are We?

- How to Go Faster: Technologically

➡ - How to Go Faster: Organizationally

  - The 3 Keys to Success

    - Partner Well
    - Be Creative
    - Add Value

- Summary

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a Career in SI
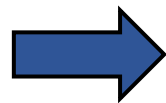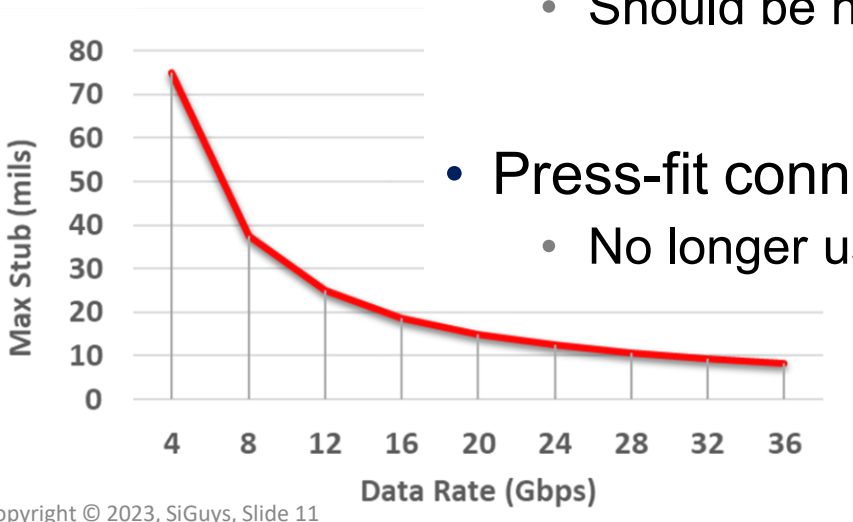
…how to succeed

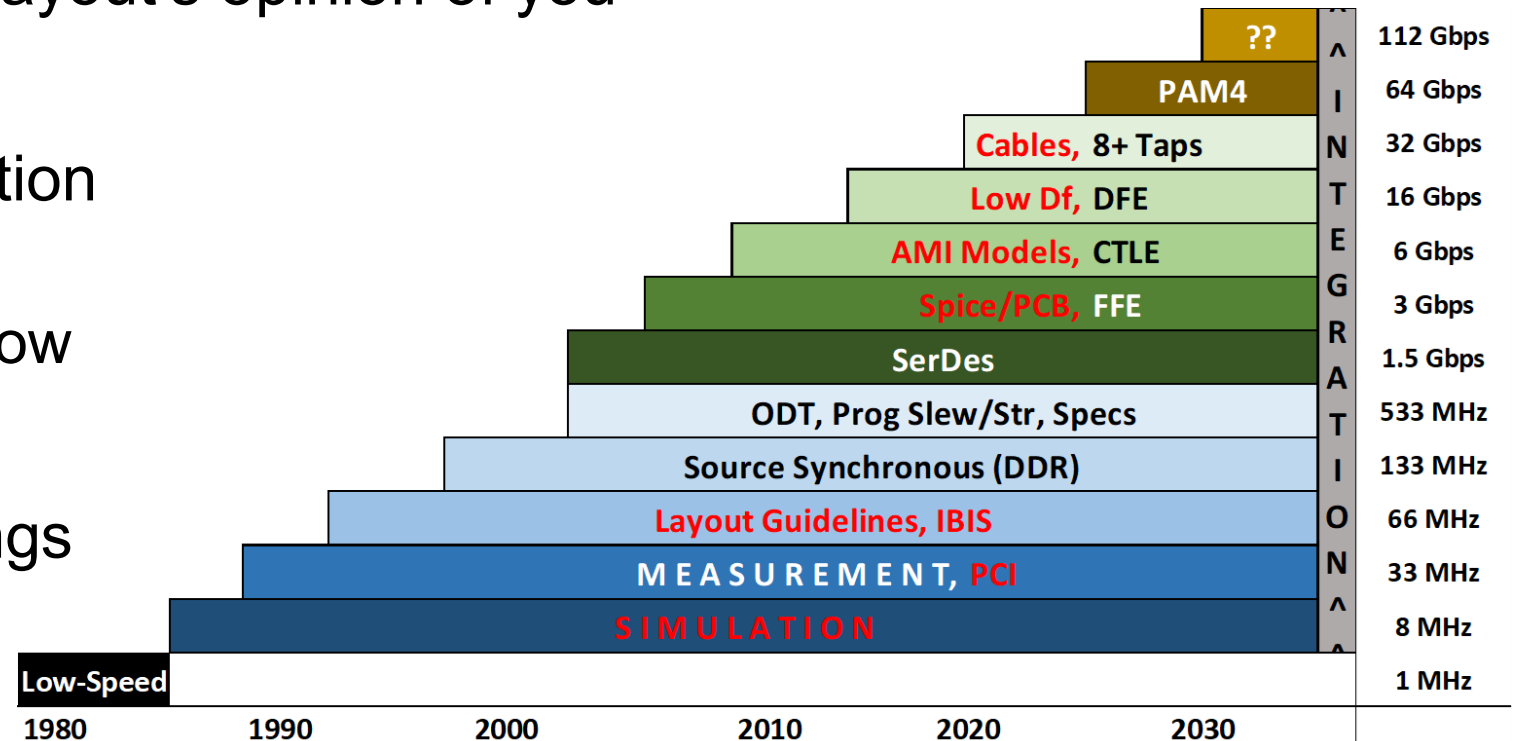SI GUYS

Partner Well

- Layout
  - This is your most important relationship
  - If Layout doesn't implement correctly, you fail
    - Nothing SI needs makes Layout's job simpler
  - Judge your success by Layout's opinion of you

- Hardware Design
  - Clear, timely communication
  - Know what you know
   - And what you don't know

- Industry
  - It's up to us to define things
 - Get on the other side of "Is it hard to keep up?"

??	112 Gbps
PAM4	64 Gbps
Cables, 8+ Taps	32 Gbps
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1980   1990   2000   2010   2020   2030

INTEGRATION

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Be Creative

- ## We make things go faster
  - ### Every speed increase is different!
    - The last 40 years proves that
  - ### The need to go faster will continue
    - What will the next 40 bring?
- ## Think outside the box
  - ### SI's added value is expanding the box
  - ### Simulation's role is not simply verification
- ## Technologically, Organizationally
  - ### How will YOU do that?
  - ### Craftsmanship required

Signal Integrity, In Practice

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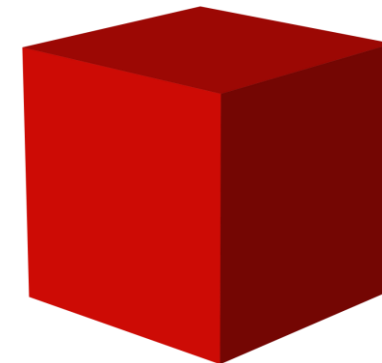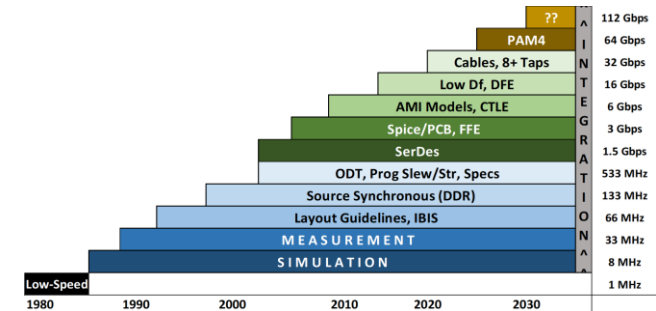
Add Value

- Your job is:
  - NOT to prove something won't work
    …but rather
  - To figure out what WILL make it work

- Leverage what has already been done
  - Component guidelines, company best practices, industry data

- Be data driven
  - Use data to substantiate your guidance
    - Approximate is better than nothing
    - Use/cite published data
    - Make it understandable
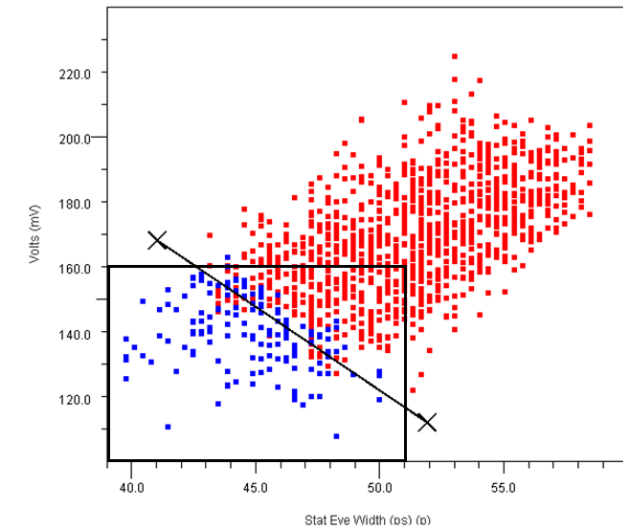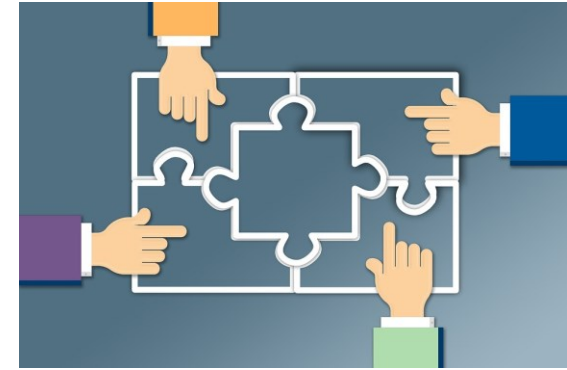
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$S + I = \$$ a Career in SI

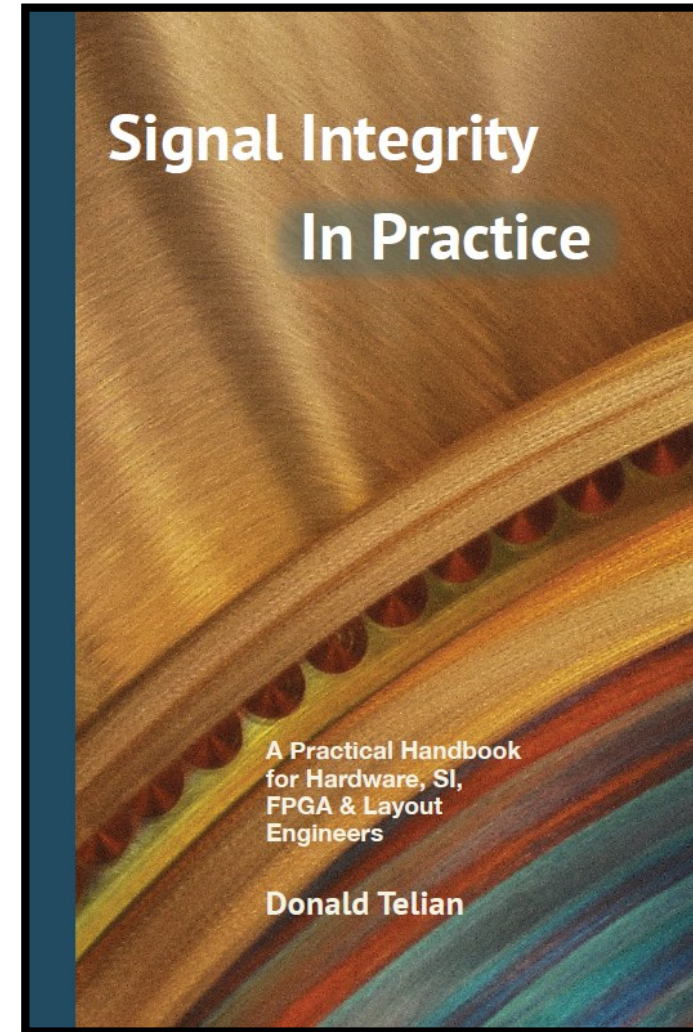*...how to succeed*

SI GUYS
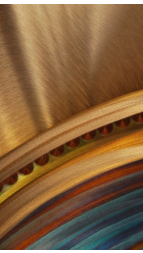
Summary

- SI is a great engineering career
  - Interesting, always changing
  - Lots of longevity
  - Community
- Technical and Organizational skills required
- YOU can succeed – we need you

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How I Can Help:

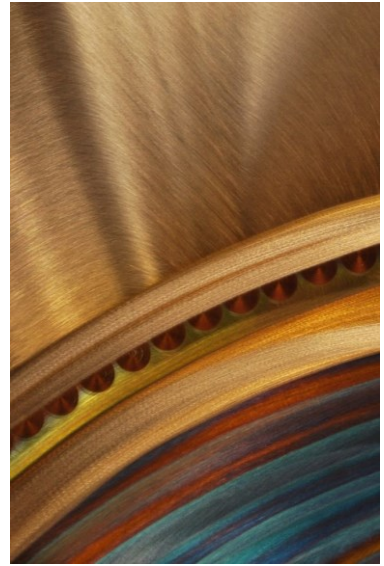https://siguys.com/

[Available at Amazon](#)

Hardcover or Kindle

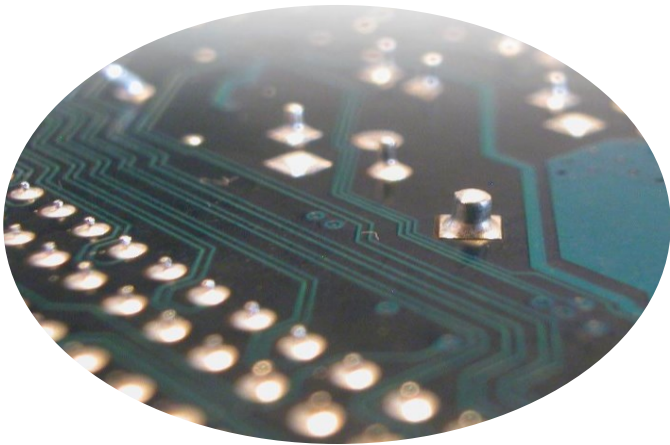# THANK YOU

Questions?

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telian@siguys.com

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7 Steps to Successful Serial Links

1. Minimize Discontinuities
2. Manage Loss
3. Route Using Best Practices
4. Route Using Double-Digit Best Practices
5. Remove Unacceptable Stubs
6. Prevent Fabrication Problems
7. Engage the Firmware Team

Signal Integrity In Practice

A Practical Handbook for Hardware, SI, FPGA & Layout Engineers

Donald Telian

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